WM8788

High Performance 24-bit Stereo ADC

DESCRIPTION

The WM8788 is a high performance 24-bit stereo ADC designed for LCD televisions, DVD, Blu-Ray and set-top box applications.

A stereo pair of analogue inputs is provided; external resistors are used to configure the device for line level inputs at 1Vrms or for higher input signal levels. The hi-fi ADCs output 16, 20 or 24-bit stereo data on the digital audio interface.

ADC sample rates from 8kHz to 192kHz are supported; Master Clock (MCLK) ratios of 128fs up to 768fs are possible (fs = sample rate).

The digital audio interface operates in Master or Slave modes, and supports Right-justified, Left-justified and I2S modes, selectable using hardware control pins.

The WM8788 is powered from a single 3.3V supply rail, connected to the AVDD and REFVDD pins.

A power on reset (POR) circuit ensures correct start-up and shut-down. The device is held in reset when MCLK is not present, offering a low-power standby state.

The WM8788 is supplied in a 16-pin TSSOP package.

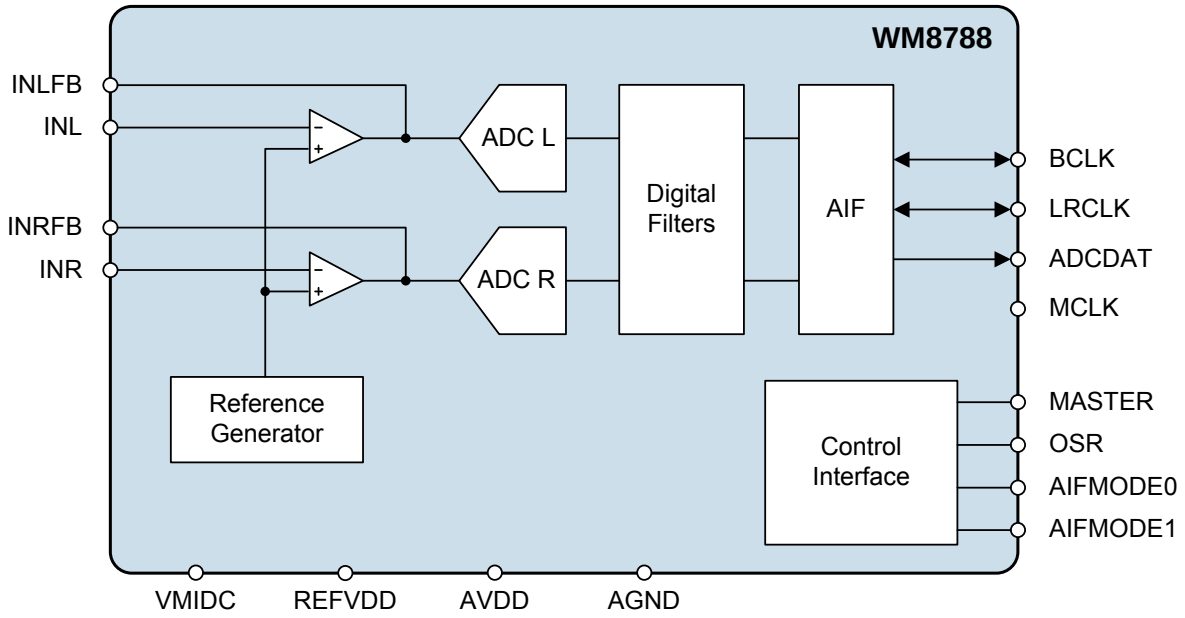
FEATURES

- Hi-fi audio ADC
  - 106dB SNR ('A' weighted
  - -91dB THD (-1dBFS output)
  - Sample rates 8kHz to 192kHz
- 2 analogue audio inputs
  - Support for line level inputs >1Vrms
- Digital audio interface
  - Master or Slave operation
  - 16, 20 or 24-bit data format
  - Right-justified, Left-justified, I2S modes
- Wide range of master clock (MCLK) rates
  - 128fs, 192fs, 256fs, 384fs, 512fs, 768fs support
- Hardware configuration control
- Integrated voltage reference circuits
- Single 3.3V supply
- 16-pin TSSOP package

APPLICATIONS

- LCD televisions
- Set-top boxes (STB)
- Blu-Ray / DVD players and recorders

BLOCK DIAGRAM



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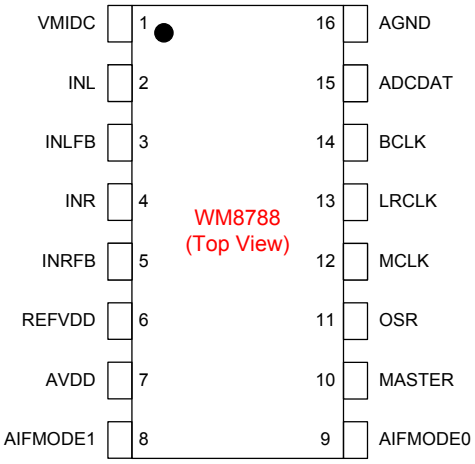
PIN CONFIGURATION

The WM8788 is supplied in a 16-pin TSSOP format. The pin configuration is illustrated below, showing the top-down view from above the chip.



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8788GEDT	-40°C to +85°C	16-pin TSSOP (Pb-free)	MSL1	260°C
WM8788GEDT/R	-40°C to +85°C	16-pin TSSOP (Pb-free, tape and reel)	MSL1	260°C

Note:
Reel quantity = 2,000

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	VMIDC	Analogue Output	Midrail voltage decoupling capacitor
2	INL	Analogue Input	Left channel analogue input
3	INLFB	Analogue Output	Left channel feedback connection
4	INR	Analogue Input	Right channel analogue input
5	INRFB	Analogue Output	Right channel feedback connection
6	REFVDD	Supply	ADC Reference Positive supply
7	AVDD	Supply	Analogue Positive supply
8	AIFMODE1	Digital Tri-state Input	Audio interface configuration pin 1
9	AIFMODE0	Digital Tri-state Input	Audio interface configuration pin 0
10	MASTER	Digital Tri-state Input	Audio interface Master / Slave select
11	OSR	Digital Tri-state Input	ADC oversample rate select
12	MCLK	Digital Input	Master clock
13	LRCLK	Digital Input / Output	Audio interface left / right clock
14	BCLK	Digital Input / Output	Audio interface bit clock
15	ADCDAT	Digital Output	ADC digital audio data
16	AGND	Supply	Ground

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltage (AVDD, REFVDD)	-0.3V	4.5V
Voltage range digital inputs	-0.7V	AVDD +0.7V
Voltage range analogue inputs	-0.7V	AVDD +0.7V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Analogue and digital I/O supplies range	AVDD, REFVDD	2.97	3.3	3.6	V
Ground	GND		0		V

Note:

1. The AVDD and REFVDD pins must both be connected to the same external supply voltage.

THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM8788 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND pin through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below in Figure 1:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package pins to PCB (conduction).

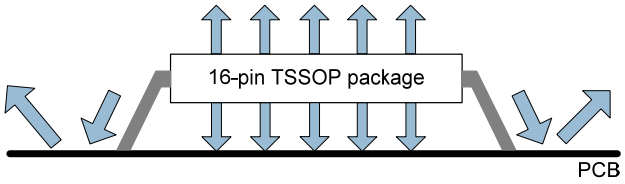


Figure 1 Heat Transfer Paths

The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated in the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air. Θ_{JA} is determined with reference to JEDEC standard JESD51-9.

The junction temperature T_J is given by $T_J = T_A + T_R$, where T_A is the ambient temperature.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating temperature range	T_A	-40		85	°C
Operating junction temperature	T_J	-40		125	°C
Thermal Resistance	Θ_{JA}		95		°C/W

Note:

1. Junction temperature is a function of ambient temperature and of the device operating conditions. The ambient temperature limits and junction temperature limits must both be observed.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = REFVDD = 3.3V, AGND = 0V, T_A = +25°C, 1kHz signal, fs = 48kHz, MCLK = 256fs unless otherwise stated.
Implemented recommended calibration start-up sequence as detailed in Calibrated Start-Up section.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (INL, INR)						
Maximum input signal level		R_{IN} = R_{FB} = 2kΩ		AVDD/3.3		Vrms
Input capacitance				20		pF
ADC Input Path Performance (Analogue Input to ADC)						
Signal to Noise Ratio	SNR	A-weighted, fs = 48kHz		106		dB
		Unweighted, fs = 48kHz		103		
		A-weighted, fs = 96kHz		106		
		Unweighted, fs = 96kHz		103		
Total Harmonic Distortion	THD	-1dBFS input, Master Mode		-91		dB
		-1dBFS input, Slave Mode		-88		
Dynamic range		-60dBFS input		106		dB
Channel separation		20Hz to 20kHz		100		dB
Channel level matching				0.1		dB
Channel phase deviation				0.1		degree
Power Supply Rejection Ratio (with respect to AVDD)	PSRR	1kHz 100mV pk-pk applied to AVDD		50		dB
Digital Inputs / Outputs						
Input high level			0.7 x AVDD			V
Input low level					0.3 x AVDD	V
Output high level		I_{OL} = 1mA	0.9 x AVDD			V
Output low level		I_{OH} = -1mA			0.1 x AVDD	V
Input capacitance				5		pF
Input leakage			-1		1	µA
Clocking						
MCLK frequency			2.048		36.864	MHz
Analogue Reference Levels						
Midrail Reference Voltage	VMID		-4%	AVDD/2	+4%	V
VMID resistance to Ground	R_{VMID}			35		kΩ
Current Consumption						
AVDD current consumption	I_{AVDD}	Quiescent fs = 48kHz, MCLK = 256fs		84		mA
		Quiescent fs = 96kHz, MCLK = 256fs		88		
		Quiescent No clocks applied		1		

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is the difference in level between a full scale output signal and the device output noise with no signal applied, measured over a bandwidth of 20Hz to 20kHz. This ratio is also called idle channel noise. (No Auto-zero or Mute function is employed).
2. Total Harmonic Distortion (dB) – THD is the difference in level between a 1kHz reference sine wave output signal and the first seven harmonics of the output signal. The amplitude of the fundamental frequency of the output signal is compared to the RMS value of the next seven harmonics and expressed as a ratio.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the difference in level between a 1kHz reference sine wave output signal and all noise and distortion products in the audio band. The amplitude of the fundamental reference frequency of the output signal is compared to the RMS value of all other noise and distortion products and expressed as a ratio.
4. Channel Separation (L/R) (dB) – is a measure of the coupling between left and right channels. A full scale signal is applied to the left channel only, and the right channel amplitude is measured. Next, a full scale signal is applied to the right channel only, and the left channel amplitude is measured. The worst case channel separation is quoted; this is the difference in level between the full-scale output and the cross-channel output signal level, expressed as a ratio.
5. Power Supply Rejection Ratio (dB) – PSRR is a measure of ripple attenuation between a power supply rail and a signal output path. With the signal path idle, a small sine wave ripple is applied to power supply rail. The amplitude of the supply ripple is compared to the amplitude of the output signal generated and is expressed as a ratio.
6. All performance measurements are carried out with 20kHz AES17 low pass filter for distortion measurements, and an A-weighted filter for noise measurement. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out-of-band noise; although it is not audible, it may affect dynamic specification values.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

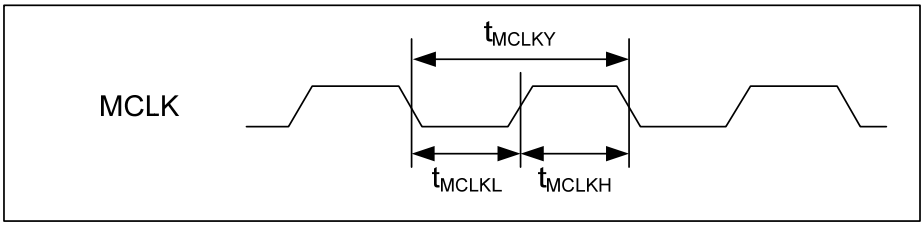


Figure 2 Master Clock Timing

Test Conditions

AVDD = REFVDD = 3.3V, AGND = 0V, T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing						
MCLK frequency	1 / T_{MCLKY}		2.048		36.864	MHz
MCLK duty cycle (= T_{MCLKH} : T_{MCLKL})			60:40		40:60	

AUDIO INTERFACE TIMING

MASTER MODE

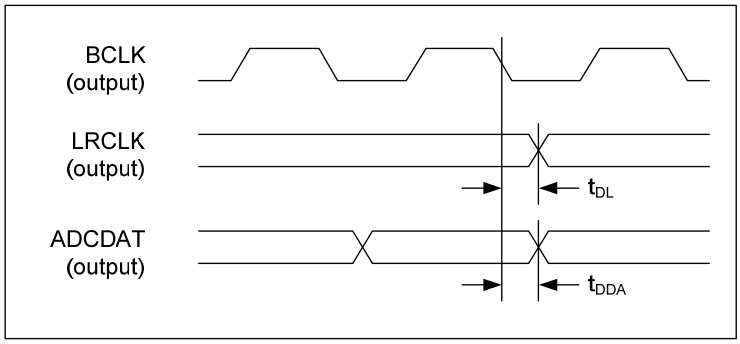


Figure 3 Audio Interface Timing - Master Mode

Test Conditions

AVDD = REFVDD = 3.3V, AGND = 0V,

T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
LRCLK propagation delay from BCLK falling edge	t_{DL}			20	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			20	ns

SLAVE MODE

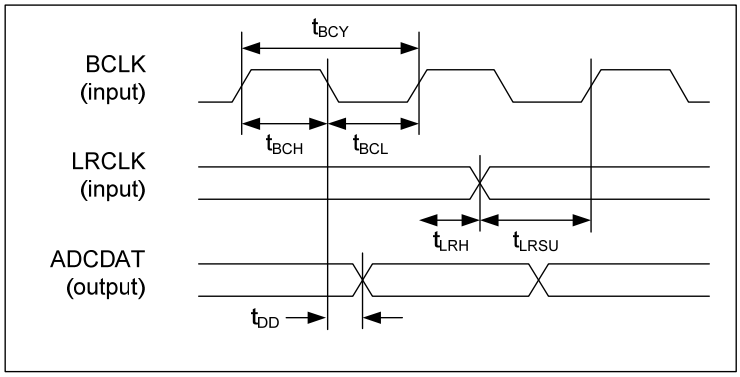


Figure 4 Audio Interface Timing - Slave Mode

Test Conditions

AVDD = REFVDD = 3.3V, AGND = 0V,

T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	20			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	20			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			20	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8788 is a high-performance 24-bit stereo ADC designed for LCD televisions, DVD, Blu-Ray and set-top box applications. It is packaged in a 16-pin TSSOP.

The device comprises two analogue input channels. External resistors are used to configure the device for line level inputs at 1Vrms or for higher input signal levels.

The stereo hi-fi ADCs operate at sample rates from 8kHz to 192kHz. A high pass filter is provided in the ADC path for removing DC offsets and suppressing low frequency noise.

The digital audio interface can operate in Master or Slave mode and supports the ADC output in Right-justified, Left-justified or I2S format. The data word size is selectable between 16, 20 or 24 bits. The device configuration is selected using hardware control inputs. The digital control inputs use tri-state logic in order to support many different configuration selections.

The WM8788 incorporates an internal voltage reference and LDO regulator for power-efficient operation from a single power supply. External clocking is required via the MCLK pin.

A power on reset (PoR) circuit ensures correct start-up and shut-down. The WM8788 is held in reset when MCLK is not present, offering a low-power standby state.

CALIBRATED START-UP

SLAVE MODE

The WM8788 chip has a phase calibration circuit that is active in slave mode. This circuit detects incoming clock phase relationship and configures the device automatically to ensure best performance of the device.

Phase calibration starts as soon as the device comes out of reset, and takes 64 BCLK periods from Power on Reset to complete. Note that once the clock signals are calibrated and in phase, no further calibration will take place until the device next comes out of reset.

For the phase calibration to work effectively, the calibration must take place when the MCLK and the BCLK signals are stable with a fixed phase relationship and running at the frequency which the device will eventually operate. There are three different sequences that allow the system designer to ensure that this can happen:

1. Ensure that MCLK and BCLK have a fixed phase relationship before LRCLK is applied
2. After power-up, pause LRCLK for a minimum of 1 period
3. After power-up, stop MCLK for a minimum of 20 periods. Then re-start MCLK in a fixed phase and frequency relationship to BCLK

In option (1), the device will be held in reset if no LRCLK is applied. MCLK and BLCK must be in a fixed and final operation phase relationship and frequency before LRCLK is applied. Options (2) and (3) both digitally reset the device, and can be used if the clock relationship changes during operation to allow re-calibration to the new relationship.

If sample rate is changed, it is recommended that either Option 2 or Option 3 above is carried out once the sample rate change is complete.

After the calibrated start-up sequence has completed, the phase relationship between MCLK and BCLK must remain static to within 0.6ns. If there is a movement in the MCLK/BCLK phase relationship of 0.6ns or over, performance degradation in SNR and THD+N of up to 6dB from the figures stated in the electrical characteristics can occur.

Note that phase calibration only takes place in Slave Mode. In Master Mode, the phase calibration circuit is not required and is disabled.

MASTER MODE

In Master Mode operation, the device requires a reset operation after power-up to guarantee SNR performance meets the performance stated in the electrical characteristics. To reset the device after power-up, stop MCLK for a minimum of 20 periods then re-start MCLK.

INPUT SIGNAL PATH

The WM8788 supports two analogue input channels. The recommended input circuit configuration for the left input channel is illustrated in Figure 5. This is suitable for single-ended connection to line level input signals.

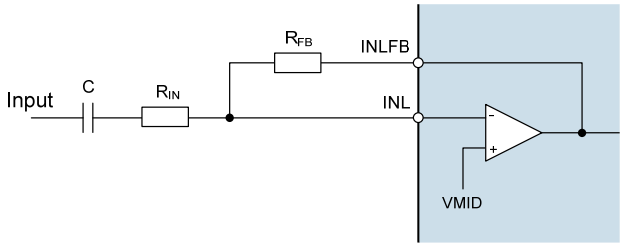


Figure 5 Input Signal Path Configuration

The right input channel is identical to the left input channel. The feedback input pins INLFB and INRFB are used to provide an adjustable gain in the input circuit, enabling input signals greater than 1Vrms to be supported.

The maximum analogue input signal level varies with AVDD and with the input circuit configuration, as described in the following equation:

$$\text{Maximum Input } (V_{RMS}) = \frac{R_{IN}}{R_{FB}} \times \frac{AVDD}{3.3}$$

See “Applications Information” for details of the recommended external components.

ANALOGUE-TO-DIGITAL CONVERTER (ADC)

The WM8788 uses two 24-bit sigma-delta ADCs. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. All common sample rates from 8kHz to 192kHz are supported; these are selected as described in the “Digital Audio Interface” section.

Digital filters are also incorporated on the ADC output signal path to remove DC offsets and other unwanted noise. The cut-off frequency of the ADC high-pass filter varies with the ADC sample rate (fs), but is typically 4Hz when fs = 48kHz.

Filter response plots for the ADC high-pass filter are shown in “Digital Filter Characteristics”.

DIGITAL AUDIO INTERFACE

The digital audio interface is used for outputting ADC data from the WM8788. It uses three pins:

- ADCDAT - ADC data output
- LRCLK - Left / Right data alignment clock
- BCLK - Bit clock, for synchronisation

The configuration of the digital audio interface is determined by the logic levels on the following hardware control pins:

- MASTER - Master / Slave mode select
- OSR - ADC Oversample rate select
- AIFMODE0 - Audio Interface configuration select 0
- AIFMODE1 - Audio Interface configuration select 1

The digital audio interface supports Right-justified, Left-justified and I2S formats. The data word size can be 16, 20 or 24-bits.

Audio sample rates (fs) from 8kHz to 192kHz are supported. A master clock (MCLK) is required at one of the typical clocking ratios 128fs, 192fs, 256fs, 384fs, 512fs and 768fs.

The WM8788 can operate in master mode or in slave mode. In master mode, LRCLK and BCLK are generated by the WM8788. In slave mode, LRCLK and BCLK are inputs to the WM8788.

The digital audio interface is configured using the hardware control pins MASTER, OSR, AIFMODE0 and AIFMODE1. Note that these pins are tri-state digital inputs. The logic 1 and logic 0 voltage levels are referenced to the AVDD power domain. A logic ‘Z’ is a high-impedance condition which is selected when the pin is floating and not connected.

A description of the hardware control pins is provided in the “Digital Audio Interface Control” section below.

The digital audio interface protocols are described in the “Master and Slave Mode Operation” and “Audio Data Formats” sections.

DIGITAL AUDIO INTERFACE CONTROL

The digital audio interface protocol is selected using the control pins AIFMODE0 and AIFMODE1, as described in Table 1.

AIFMODE1	AIFMODE0	FORMAT
0	0	16-bit Right-justified
0	1	20-bit Right-justified
0	Z	24-bit Right-justified
1	0	16-bit Left-justified
1	1	20-bit Left-justified
1	Z	24-bit Left-justified
Z	0	16-bit I2S
Z	1	20-bit I2S
Z	Z	24-bit I2S

Table 1 Digital Audio Interface Mode Select

For Slave Mode, set MASTER = 0 and set OSR according to the applicable sample rate.

MASTER	OSR	SAMPLE RATE
0	0	8, 16, 32, 44.1, 48kHz
0	1	88.2, 96kHz
0	Z	176.4, 192kHz

Table 2 Slave Mode Configuration

In Slave Mode, the MCLK and LRCLK inputs must conform to a valid clocking ratio, as noted below.

The LRCLK frequency is the same as the sample rate, fs. MCLK frequencies of 128fs, 192fs, 256fs, 384fs, 512fs and 768fs can be supported, depending on the sample rate.

The BCLK signal is an input to the WM8788 in slave mode. A range of BCLK frequencies can be supported, provided there are sufficient BCLK cycles for the selected data word length. The BCLK frequency must not be higher than the MCLK frequency, and must not be higher than 12.288MHz.

SAMPLE RATE	MCLK FREQUENCY (MHz)					
	128fs	192fs	256fs	384fs	512fs	768fs
8kHz	n/a	n/a	2.048	3.072	4.096	6.144
16kHz	n/a	n/a	4.096	6.144	8.192	12.288
32kHz	n/a	n/a	8.192	12.288	16.384	24.576
44.1kHz	n/a	n/a	11.2896	16.9344	22.5792	33.8688
48kHz	n/a	n/a	12.288	18.432	24.576	36.864
88.2kHz	11.2896	16.9344	22.5792	33.8688	n/a	n/a
96kHz	12.288	18.432	24.576	36.864	n/a	n/a
176.4kHz	22.5792	33.8688	n/a	n/a	n/a	n/a
192kHz	24.576	36.864	n/a	n/a	n/a	n/a

Table 3 MCLK Frequency in Slave Mode

For Master Mode, set MASTER and OSR according to the applicable sample rate and clocking ratio.

MASTER	OSR	CLOCKING RATIO	SAMPLE RATE
1	0	384fs	8, 16, 32, 44.1, 48kHz
1	1	384fs	88.2, 96kHz
Z	0	256fs	8, 16, 32, 44.1, 48kHz
Z	1	256fs	88.2, 96kHz

Table 4 Master Mode Configuration

In Master Mode, the sample rate (fs) is determined by the MCLK frequency and by the selected clocking ratio. The LRCLK frequency is the same as the sample rate, and is output by the WM8788 in master mode.

The BCLK signal is output by the WM8788 in master mode. The BCLK frequency is LRCLK x 64.

MASTER AND SLAVE MODE OPERATION

The digital audio interface can be configured as a Master or a Slave interface, depending on the state of the MASTER control pin described earlier. The two modes are illustrated in Figure 6 and Figure 7.

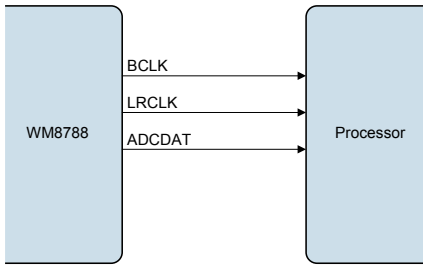


Figure 6 Master Mode

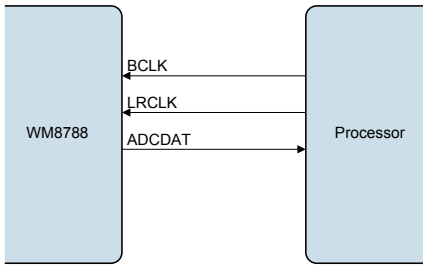


Figure 7 Slave Mode

In Master mode, LRCLK and BCLK are configured as outputs, and the WM8788 controls the timing of the data transfer on the ADCDAT pin.

In Master mode, the LRCLK frequency is determined automatically according to the MCLK frequency and the selected clocking ratio. The BCLK frequency is LRCLK x 64.

In Slave mode, LRCLK and BCLK are configured as inputs, and the data timing is controlled by an external master.

AUDIO DATA FORMATS

Three audio data formats are supported by the digital audio interface:

- Right-justified
- Left-justified
- I^2S

All of these modes are MSB first, and are illustrated below. Refer to the “Signal Timing Requirements” section for timing information.

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.

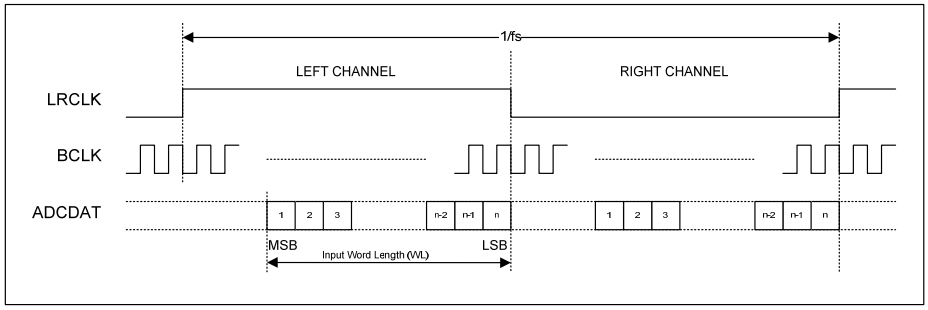


Figure 8 Right Justified Audio Interface (assuming n-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

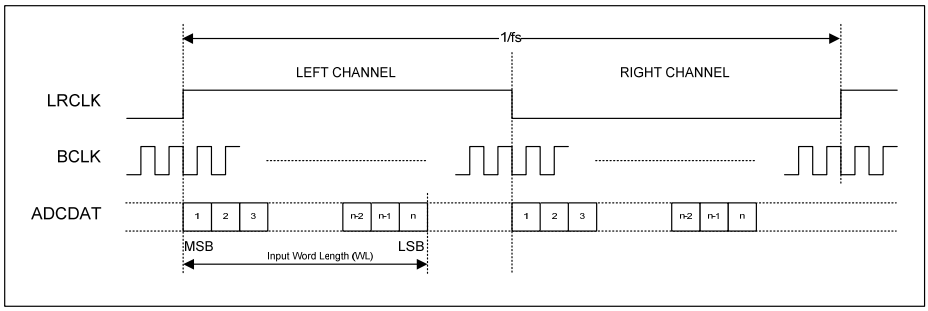


Figure 9 Left Justified Audio Interface (assuming n-bit word length)

In I^{2}S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

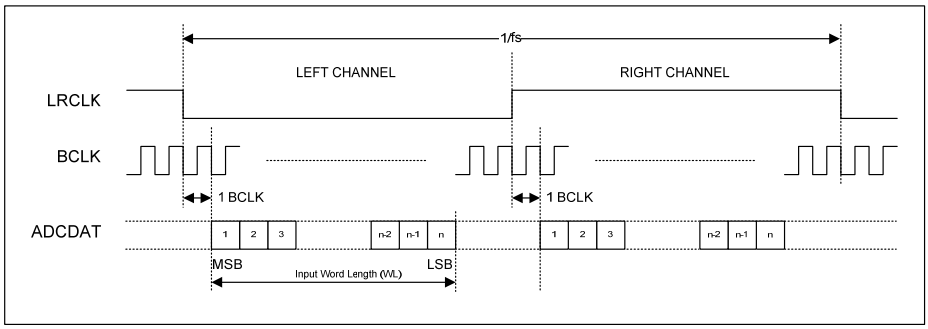


Figure 10 I^{2}S Justified Audio Interface (assuming n-bit word length)

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband	+/- 0.1dB	0		0.454 fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.1	dB
Stopband		0.546s			
Stopband Attenuation	f > 0.546 fs	-60			dB
Group Delay			16.5 / fs		s

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

ADC FILTER RESPONSE

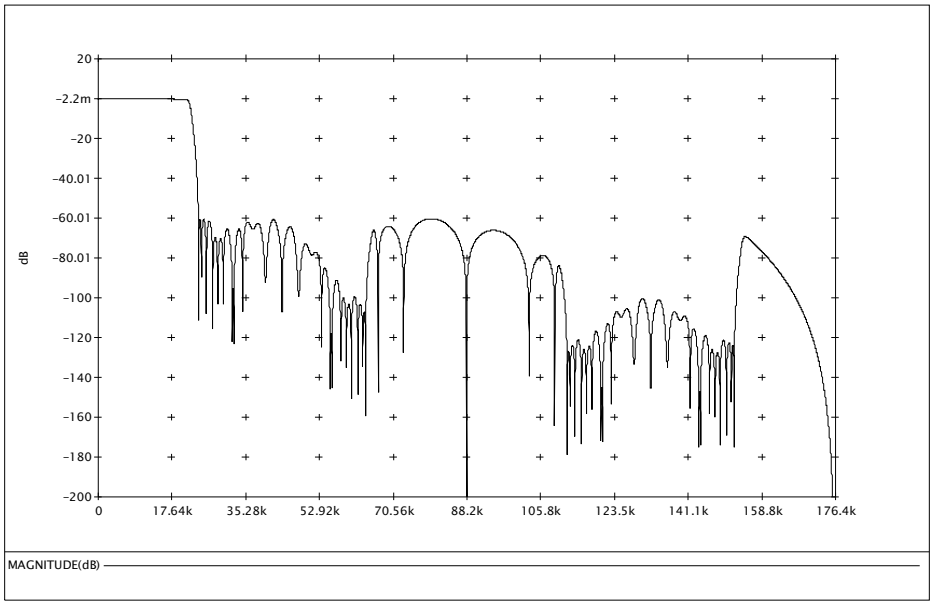


Figure 11 ADC Frequency Response up to 4 x fs (Sample rate, fs = 48kHz)

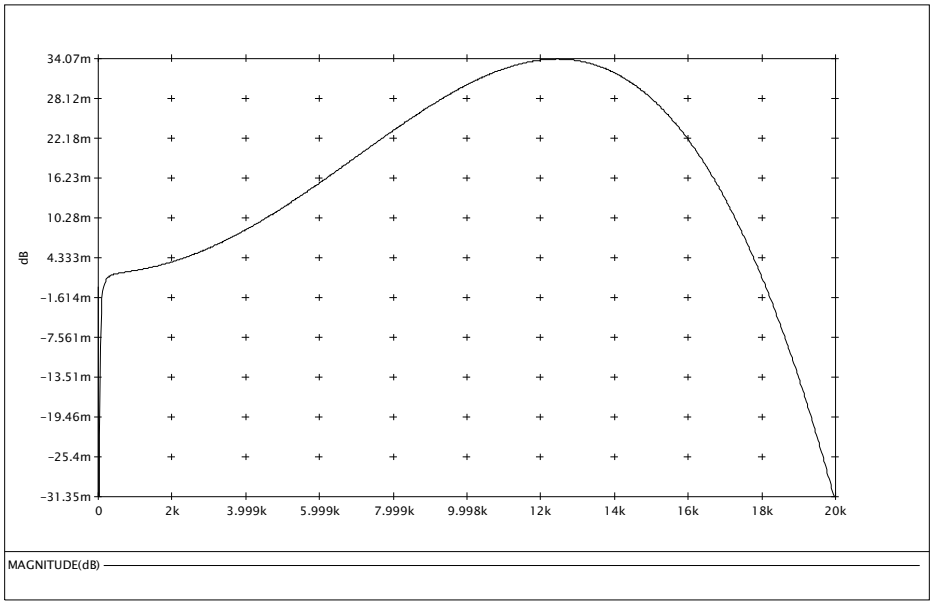


Figure 12 ADC Pass Band Frequency Response up to fs/2 (Sample rate, fs = 48kHz)

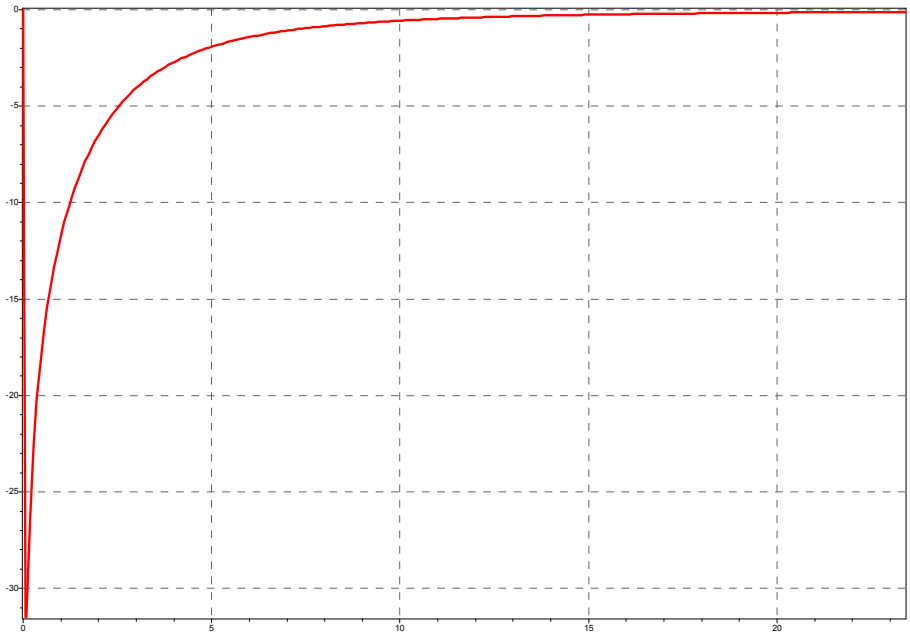


Figure 13 ADC High Pass Filter Frequency Response (Sample rate, fs = 48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

AUDIO INPUT PATHS

The WM8788 provides 2 analogue audio inputs. The maximum analogue input signal level varies with AVDD and with the input circuit configuration, as described in the following equation:

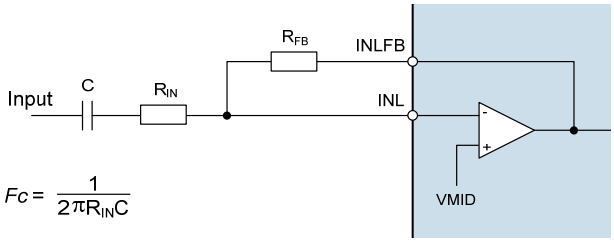
$$\text{Maximum Input } (V_{RMS}) = \frac{R_{IN}}{R_{FB}} \times \frac{AVDD}{3.3}$$

It is recommended that the resistors R_{IN} and R_{FB} should not exceed 10kΩ.

For 1Vrms (0dBV) maximum input signal level when AVDD = 3.3V, the recommended input components are R_{IN} = 2kΩ, R_{FB} = 2kΩ.

For 2Vrms (6dBV) maximum input signal level when AVDD = 3.3V, the recommended input components are R_{IN} = 2kΩ, R_{FB} = 1kΩ.

The input pins INL and INR are referenced to the internal DC reference, VMID. A DC blocking capacitor is required for each input. The choice of capacitor is determined by the filter that is formed between that capacitor and the input resistor, R_{IN}. The circuit is illustrated in Figure 14.



Fc = high pass 3dB cut-off frequency

Figure 14 Input Signal Path External Components

It is recommended that an input capacitor is selected such that the Fc cut-off frequency is less than 20Hz. It is recommended that a 4.7μF capacitance is used for all WM8788 input connections. Tantalum electrolytic capacitors are particularly suitable as they offer high stability in a small package size.

See Wolfson Applications Note WAN_0176 for further guidance on the choice of capacitor types.

POWER SUPPLY DECOUPLING

Electrical coupling exists particularly in digital logic systems where switching in one sub-system causes fluctuations on the power supply. This effect occurs because the inductance of the power supply acts in opposition to the changes in current flow that are caused by the logic switching. The resultant variations (or 'spikes') in the power supply voltage can cause malfunctions and unintentional behavior in other components. A decoupling (or 'bypass') capacitor can be used as an energy storage component which will provide power to the decoupled circuit for the duration of these power supply variations, protecting it from malfunctions that could otherwise arise.

Coupling also occurs in a lower frequency form when ripple is present on the power supply rail caused by changes in the load current or by limitations of the power supply regulation method. In audio components such as the WM8788, these variations can alter the performance of the signal path, leading to degradation in signal quality. A decoupling (or 'bypass') capacitor can be used to filter these effects, by presenting the ripple voltage with a low impedance path that does not affect the circuit to be decoupled.

These coupling effects are addressed by placing a capacitor between the supply rail and the corresponding ground reference. In the case of systems comprising multiple power supply rails, decoupling should be provided on each rail.

The recommended power supply decoupling capacitors for WM8788 are listed below in Table 5.

POWER SUPPLY	DECOUPLING CAPACITOR
AVDD	4.7μF ceramic
REFVDD	4.7μF ceramic
VMIDC	4.7μF ceramic

Table 5 Power Supply Decoupling Capacitors

All decoupling capacitors should be placed as close as possible to the WM8788 device.

The VMIDC capacitor is not, technically, a decoupling capacitor. However, it does serve a similar purpose in filtering noise on the VMID reference. The connection between GND, the VMID decoupling capacitor and the main system ground should be made at a single point as close as possible to the GND pin of the WM8788.

Due to the wide tolerance of many types of ceramic capacitors, care must be taken to ensure that the selected components provide the required capacitance across the required temperature and voltage ranges in the intended application. For most application the use of ceramic capacitors with capacitor dielectric X5R is recommended.

See Wolfson Applications Note WAN_0176 for further guidance on the choice of capacitor types.

RECOMMENDED EXTERNAL COMPONENTS DIAGRAM

Figure 15 provides a summary of recommended external components for WM8788. Note that the actual requirements may differ according to the specific target application.

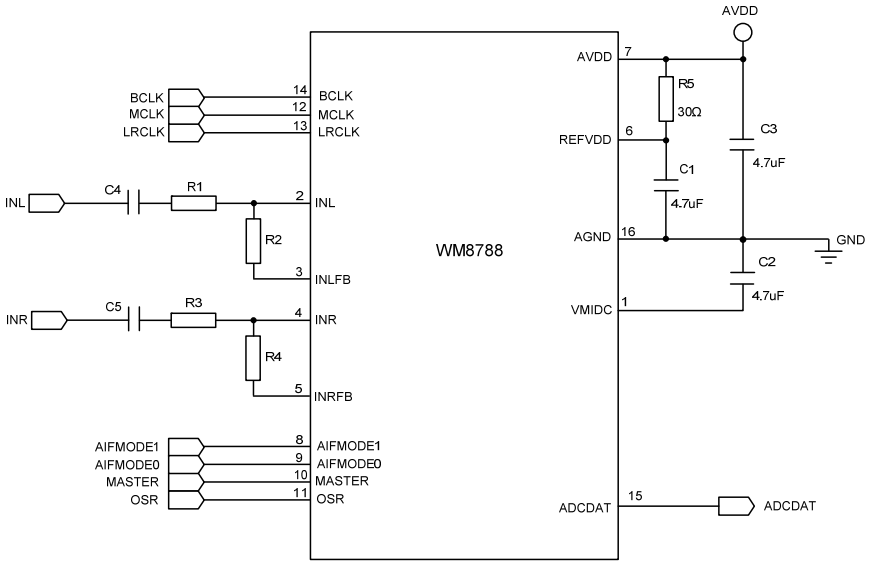


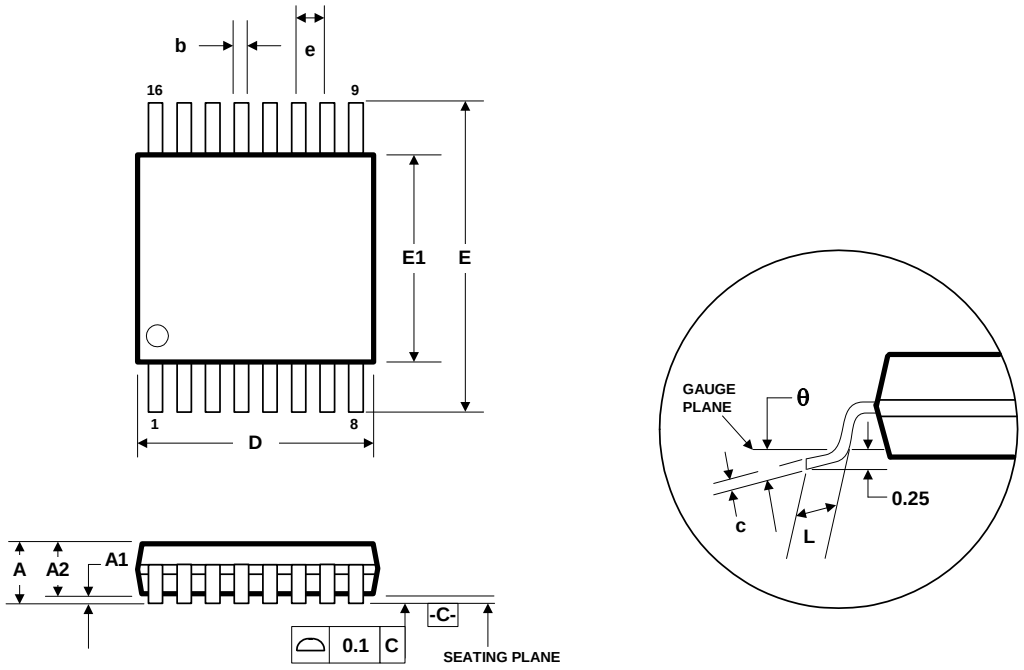
Figure 15 WM8788 Recommended External Components Diagram

PCB LAYOUT CONSIDERATIONS

Poor PCB layout will degrade the performance and be a contributory factor in EMI, ground bounce and resistive voltage losses. All external components should be placed as close to the WM8788 device as possible, with current loop areas kept as small as possible.

PACKAGE DIMENSIONS

DT: 16 PIN TSSOP (5.0 x 4.4 x 1.0 mm) **DM013.B**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.80	1.00	1.05
b	0.19	-----	0.30
c	0.09	-----	0.20
D	4.90	5.00	5.10
e	0.65 BSC		
E	6.4 BSC		
E_1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ	0^o	-----	8^o
REF:	JEDEC.95, MO-153		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MO-153, VARIATION = AB. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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ADDRESS:

Wolfson Microelectronics plc

26 Westfield Road

Edinburgh

EH11 2QB

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com

REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES
01/12/11	2.3	BT	Added 0.6ns Phase variation restriction and 6dB Performance degradation to calibrated start-up sequence
01/12/11	2.3	BT	Added Master Mode reset requirement after power up