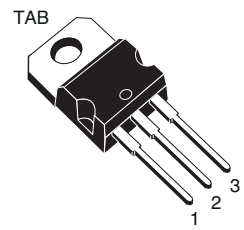
STP180NS04ZC

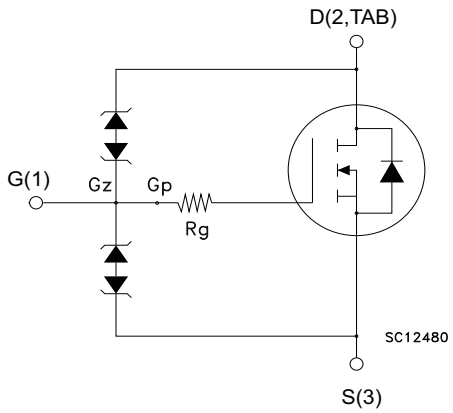
N-channel 40 V clamped 3.6 mΩ typ., 120 A fully protected SAFeFET™ Power MOSFET in a TO-220 package

Datasheet - production data



TO-220

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STP180NS04ZC	40 V clamped	4.2 mΩ	120 A

- Low capacitance and gate charge
- 100% avalanche tested
- 175 °C maximum junction temperature

Applications

- Switching and linear applications

Description

This fully clamped Power MOSFET is manufactured using an advanced mesh overlay process which is based on an innovative strip layout. The benefits of this technology, coupled with the extra clamping capabilities render this device particularly suitable for the harshest operating conditions, such as those associated with the automotive environment. The device is also suitable for other applications that require a high degree of ruggedness.

Table 1. Device summary

Order code	Marking	Package	Packaging
STP180NS04ZC	P180NS04ZC	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	41(1)	V
V_{DG}	Drain-gate voltage	33(1)	V
V_{GS}	Gate-source voltage	± 20(1)	V
I_D (2)	Drain current (continuous) at T_C = 25 °C	120	A
I_D (2)	Drain current (continuous) at T_C=100 °C	120	A
I_{DG}	Drain gate current (continuous)	±50	mA
I_{GS}	Gate-source current (continuous)	±50	mA
I_{DM} (3)	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at T_C = 25 °C	330	W
	Derating factor	2.2	W/°C
ESD	Gate-source human body model (C = 100 pF, R = 1.5 kΩ)	± 8	kV
ESD	Gate-drain human body model (C = 100 pF, R = 1.5 kΩ)	± 8	kV
ESD	Drain-source human body model (C = 100 pF, R = 1.5 kΩ)	± 8	kV
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Voltage is limited by Zener diodes
2. Current limited by wire bonding
3. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.45	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not repetitive (pulse width limited by Tjmax $\delta < 1\%$)	80	A
E_{AS}	Single pulse avalanche energy (starting Tj=25 °C, $I_D=I_{AS}$, V_{DD}=21 V) *(see Figure 17, Figure 14.)*	1000	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DG}$	Clamped voltage	I_D = 1 mA, V_{GS} = 0 -40 < Tj < 175 °C	33		41	V
$V_{DSR(CL)}$	Drain-source clamping voltage (DC)	$I_{GS(CL)}$ = -2 mA, I_D = 1 A		41		V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 16 V V_{DS} = 16 V, T_j = 150 °C V_{DS} = 16 V, T_j = 175 °C			1 50 100	µA µA µA
I_{GSS} (1)	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±10 V V_{GS} = ±10 V,T_j = 175 °C V_{GS} = ±16 V,T_j = 175 °C			±2 ±50 ±150	µA µA µA
V_{GSS}	Gate-source breakdown voltage	I_{GS} = ±100 µA	18		25	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 40 A		3.6	4.2	mΩ
R_G	Internal gate resistor			14		Ω

1. Gate Oxide, without zener diodes, tested at wafer sorting (I_{GSS} < ± 100 nA @ ± 20 V Tj=25 °C).
Figure 17: Unclamped inductive load test circuit for electrical schematics

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	4500	-	pF
C_{oss}	Output capacitance		-	1700	-	pF
C_{rss}	Reverse transfer capacitance		-	500	-	pF
$t_{r(Voff)}$	Off voltage rise time	V_{CLAMP}=30 V, I_D=80 A, V_{GS}=10 V, R_G=4.7 Ω *(see Figure 14)*	-	250	-	ns
t_f	Fall time		-	115	-	ns
t_c	Cross-over time		-	290	-	ns
Q_g	Total gate charge	V_{DD}=20 V, I_D = 120 A V_{GS} =10 V *(see Figure 15)*	-	110	-	nC
Q_{gs}	Gate-source charge		-	25	-	nC
Q_{gd}	Gate-drain charge		-	45	-	nC

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		120	A
I_{SDM} (1)	Source-drain current (pulsed)				480	A
V_{SD} (2)	Forward on voltage	I_{SD}=120 A, V_{GS}=0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD}=120 A, di/dt = 100 A/µs, V_{DD}= 32 V, Tj=150 °C (see Figure 16)	-	56		ns
Q_{rr}	Reverse recovery charge		-	70		nC
I_{RRM}	Reverse recovery current		-	12		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

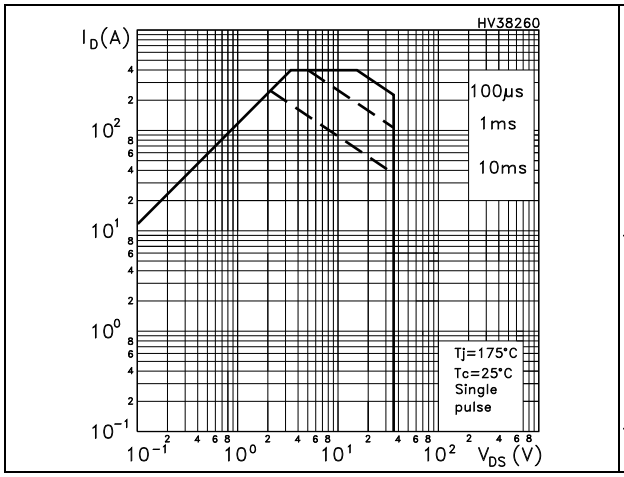


Figure 3. Thermal impedance

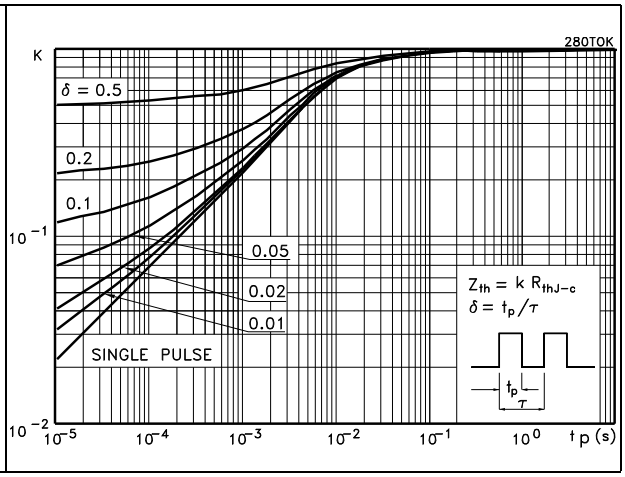


Figure 4. Output characteristics

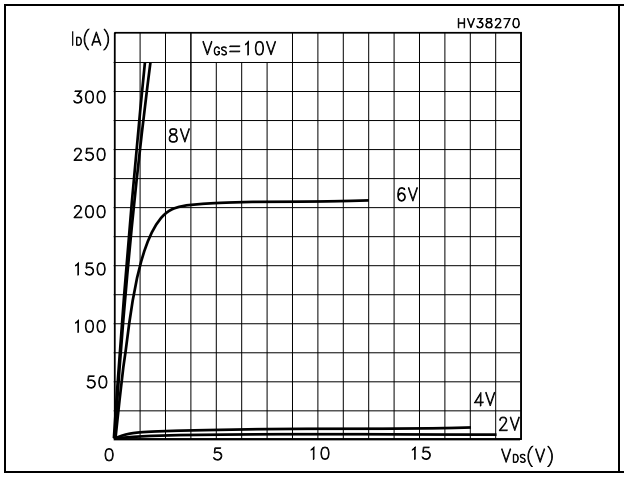


Figure 5. Transfer characteristics

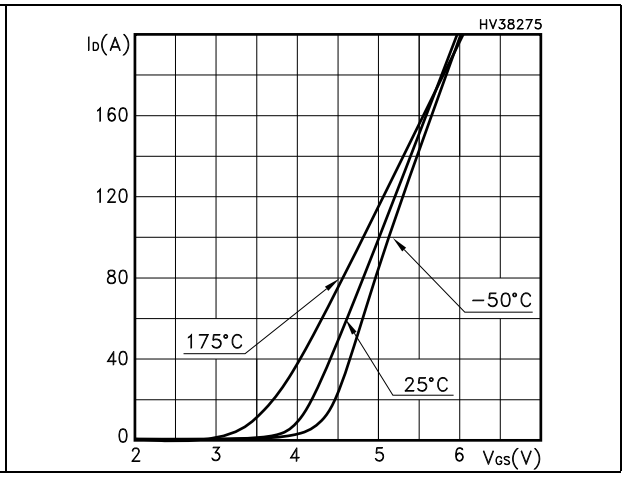


Figure 6.Transconductance

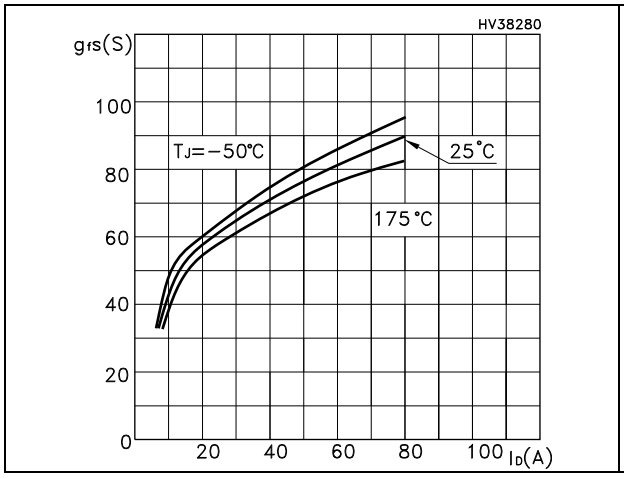


Figure 7.Static drain-source on-resistance

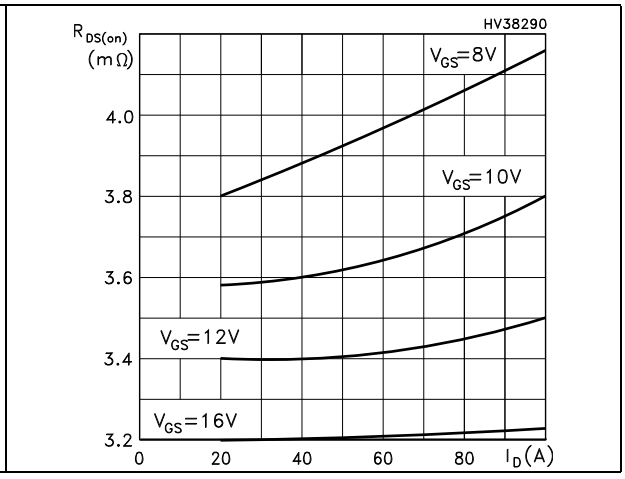


Figure 8. Gate charge vs gate-source voltage

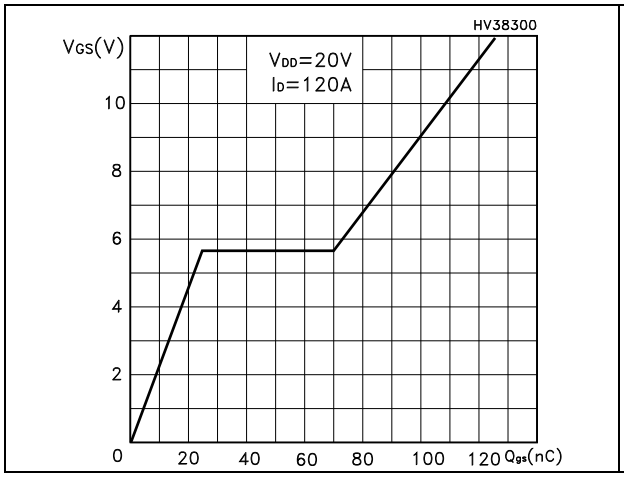


Figure 9. Capacitance variations

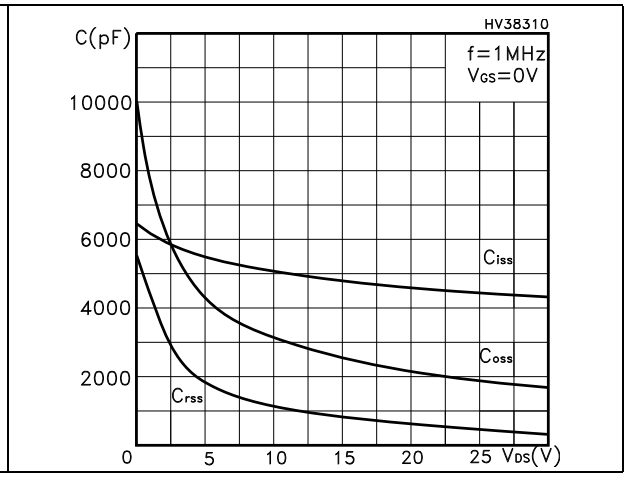


Figure 10. Normalized gate threshold voltage vs temperature

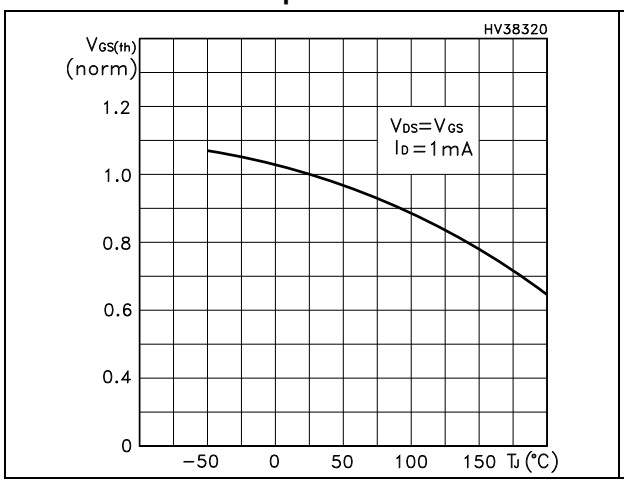


Figure 11. Normalized on-resistance vs temperature

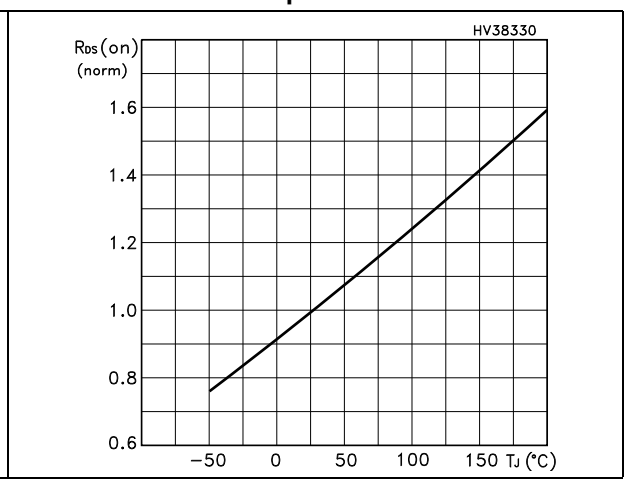


Figure 12.Source-drain diode forward characteristics

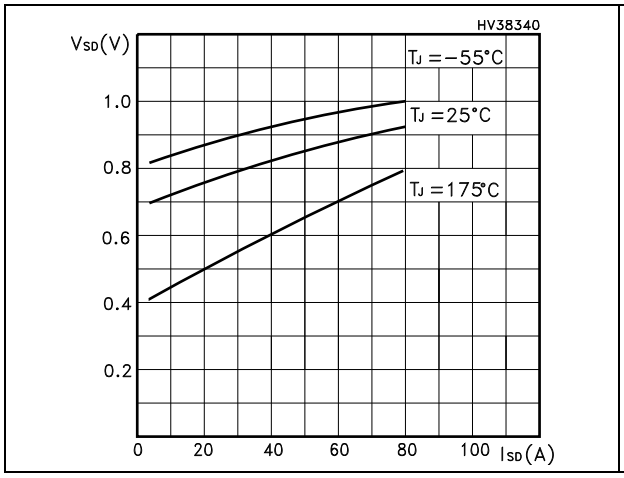
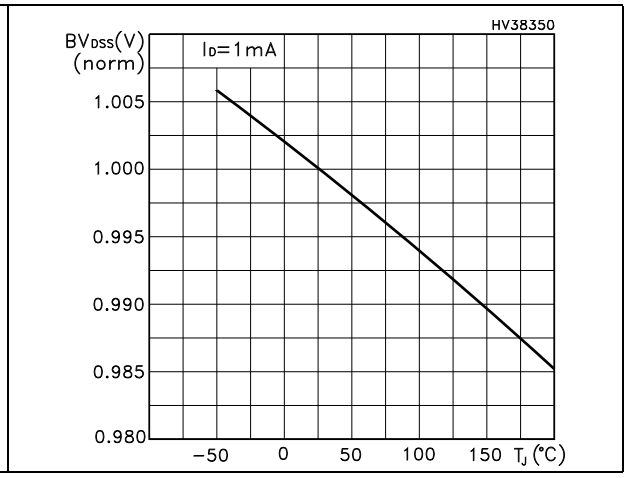


Figure 13.Normalized BV_{DSS} vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

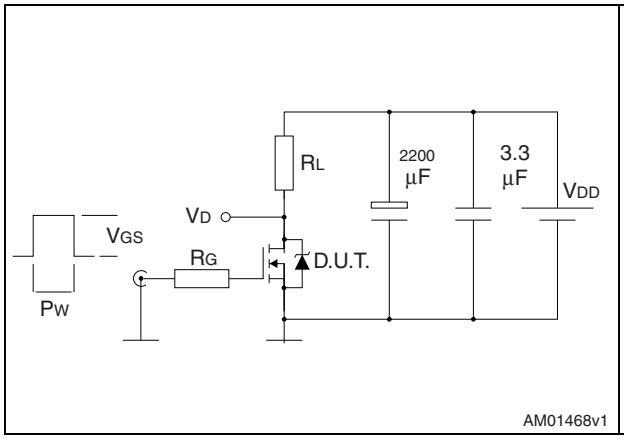


Figure 15. Gate charge test circuit

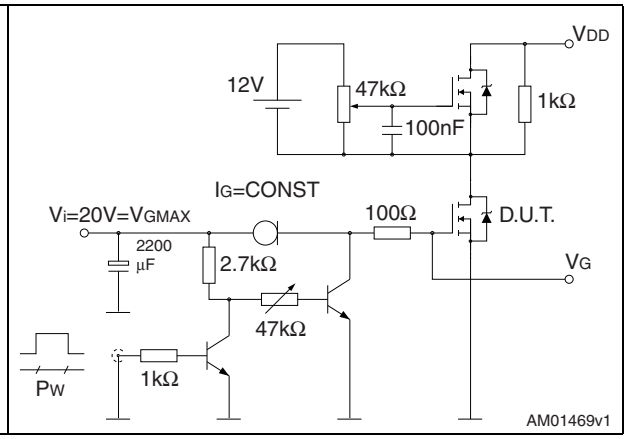


Figure 16. Test circuit for inductive load switching and diode recovery times

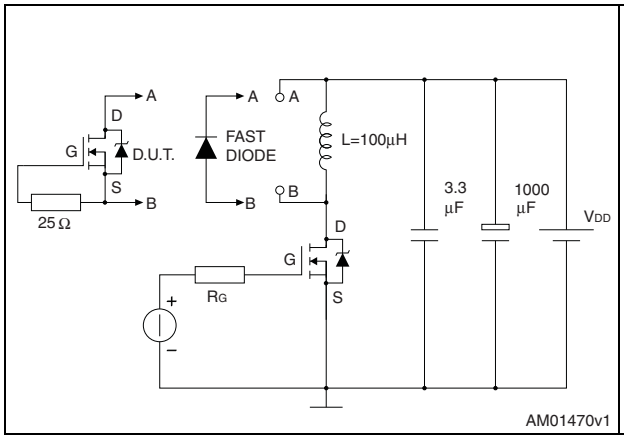


Figure 17. Unclamped inductive load test circuit

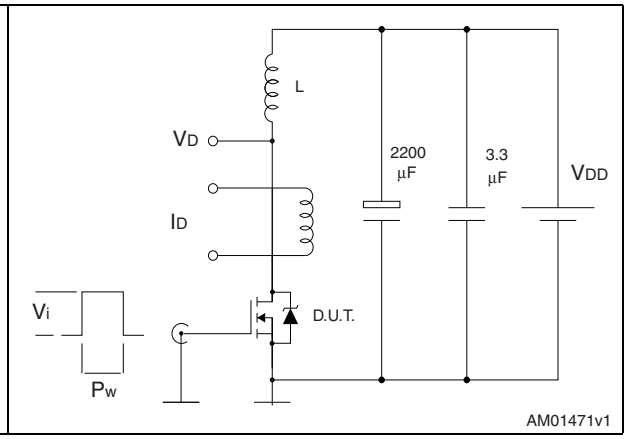


Figure 18. Unclamped inductive waveform

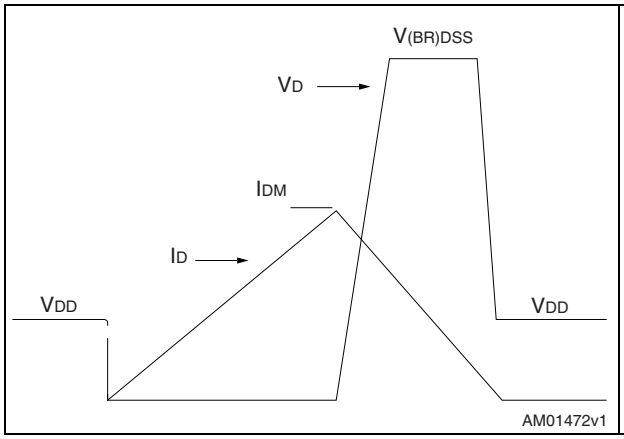
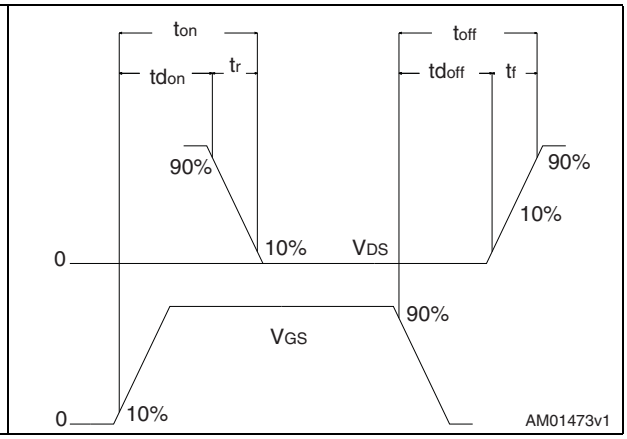


Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
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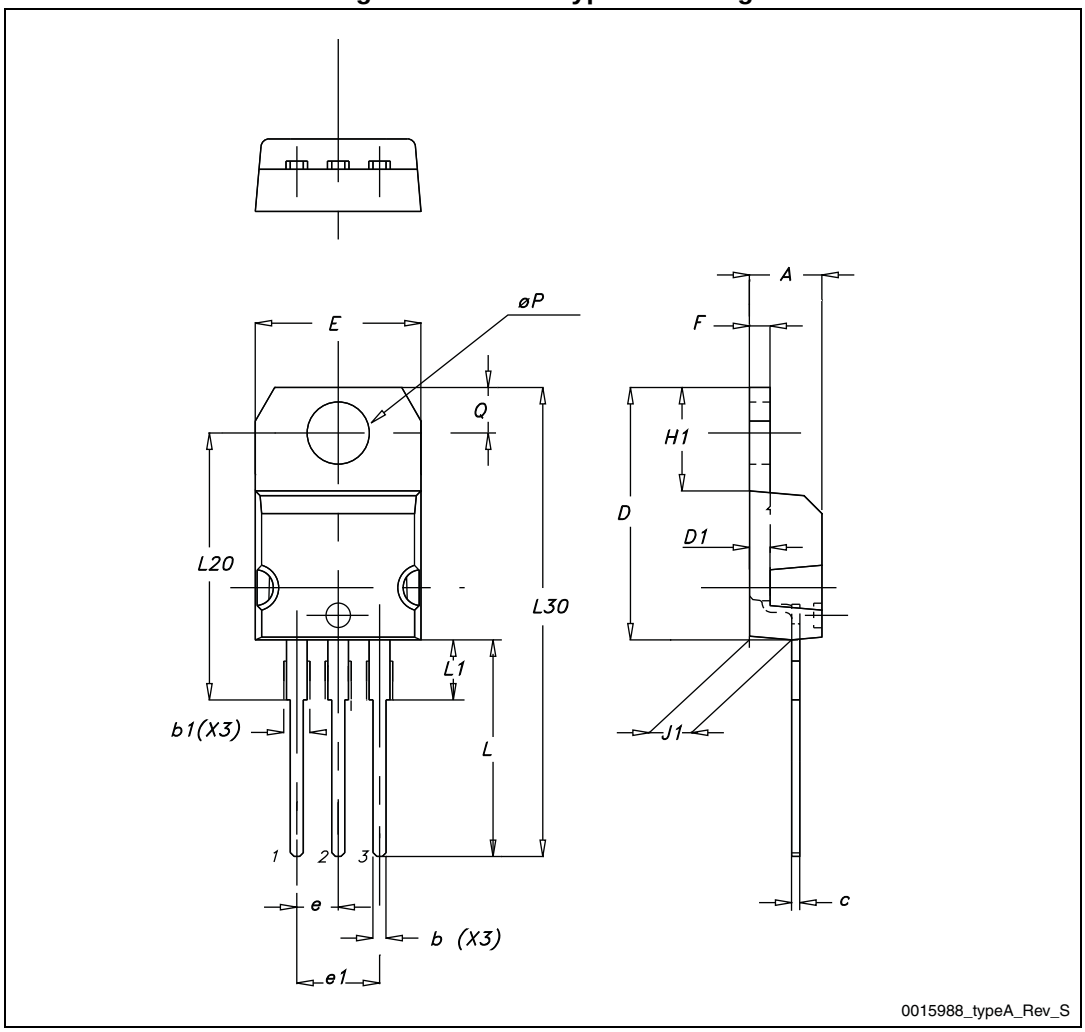
Table 8. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

Figure 20. TO-220 type A drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Apr-2008	1	First release.
21-Mar-2013	2	– *Table 1: Device summary*, *Table 2: Absolute maximum ratings*, *Table 3: Thermal data*, *Table 6: Dynamic* have been corrected. – Minor text changes. – Modified: *Applications* section on the cover page.

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