NGD18N45CLB

Ignition IGBT
18 Amps, 450 Volts

N−Channel DPAK

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This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over−Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

Features

- Ideal for Coil−on−Plug Applications
- DPAK Package Offers Smaller Footprint for Increased Board Space
- Gate−Emitter ESD Protection
- Temperature Compensated Gate−Collector Voltage Clamp Limits Stress Applied to Load
- Low Threshold Voltage Interfaces Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Emitter Ballasting for Short−Circuit Capability
- This is a Pb−Free Device

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CES}	500	V_{DC}
Collector−Gate Voltage	V_{CER}	500	V_{DC}
Gate−Emitter Voltage	V_{GE}	18	V_{DC}
Collector Current−Continuous @ T_C = 25°C − Pulsed	I_C	18 50	A_{DC} A_{AC}
ESD (Human Body Model) R = 1500 Ω, C = 100 pF	ESD	8.0	kV
ESD (Machine Model) R = 0 Ω, C = 200 pF	ESD	400	V
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.77	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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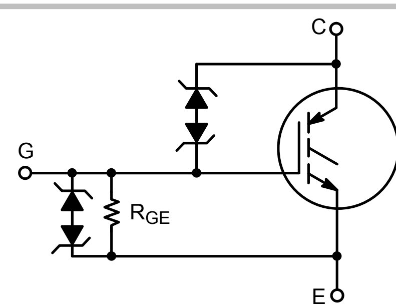
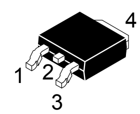
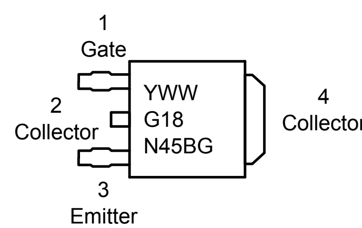
18 AMPS
450 VOLTS
$V_{CE(on)}$ ≤ 2.1 V @
I_C = 10 A, V_{GE} ≥ 4.5 V





DPAK
CASE 369C
STYLE 7

MARKING DIAGRAM



G18N45B = Device Code
Y = Year
WW = Work Week
G = Pb−Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NGD18N45CLBT4G	DPAK (Pb−Free)	2500/Tape & Reel

UNCLAMPED COLLECTOR−TO−EMITTER AVALANCHE CHARACTERISTICS (Note 2)

Characteristic	Symbol	Value	Unit
Single Pulse Collector−to−Emitter Avalanche Energy	E_{AS}		mJ
V_{CC} = 50 V, V_{GE} = 5.0 V, Pk I_L = 26.0 A, R_G = 1000 Ω, L = 1.0 mH, Starting T_J = 25°C		338	
V_{CC} = 50 V, V_{GE} = 5.0 V, Pk I_L = 10.0 A, R_G = 1000 Ω, L = 8.4 mH, Starting T_J = 25°C		420	
V_{CC} = 50 V, V_{GE} = 5.0 V, Pk I_L = 15.4 A, R_G = 1000 Ω, L = 2.0 mH, Starting T_J = 150°C		237	
V_{CC} = 50 V, V_{GE} = 5.0 V, Pk I_L = 5.7 A, R_G = 1000 Ω, L = 15.2 mH, Starting T_J = 150°C		247	

MAXIMUM SHORT−CIRCUIT TIMES

Short Circuit Withstand Time – Test 1 (See Figure 17, 3 Pulses with 10 ms Period, T_a = 105°C)	t_{sc1-1}	1000	μS
Short Circuit Withstand Time – Test 1 (See Figure 17, 3 Pulses with 10 ms Period, T_a = 150°C)	t_{sc1-2}	800	μS
Short Circuit Withstand Time – Test 2 (See Figure 18, 3 Pulses with 10 ms Period, T_a = 105°C)	t_{sc2-1}	5	ms
Short Circuit Withstand Time – Test 2 (See Figure 18, 3 Pulses with 10 ms Period, T_a = 150°C)	t_{sc2-2}	1	ms

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.3	°C/W
Thermal Resistance, Junction to Ambient — DPAK (Note 1)	$R_{\theta JA}$	95	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 2)							
Collector−Emitter Clamp Voltage	BV_{CES}	I_C = 2.0 mA	T_J = −40°C to 150°C	430	455	470	V_{DC}
		I_C = 10 mA	T_J = −40°C to 150°C	440	475	500	
Zero Gate Voltage Collector Current	I_{CES}	V_{CE} = 350 V, V_{GE} = 0 V	T_J = 25°C	−	0.5	20	μA_{DC}
			T_J = 150°C	−	75	250	
			T_J = −40°C	−	0.2	10	
		V_{CE} = 15 V, V_{GE} = 0 V	T_J = 25°C	−	−	2.0	
Reverse Collector−Emitter Leakage Current	I_{ECS}	V_{CE} = −24 V	T_J = 25°C	−	0.7	1.0	mA
			T_J = 150°C	−	12	25	
			T_J = −40°C	−	0.1	1.0	
Reverse Collector−Emitter Clamp Voltage	$B_{VCES(R)}$	I_C = −75 mA	T_J = 25°C	24	27	30	V_{DC}
			T_J = 150°C	26	29	33	
			T_J = −40°C	23	26	29	
Gate−Emitter Clamp Voltage	BV_{GES}	I_G = 5.0 mA	T_J = −40°C to 150°C	11	13	15	V_{DC}
Gate−Emitter Leakage Current	I_{GES}	V_{GE} = 10 V	T_J = −40°C to 150°C	384	590	700	μA_{DC}
Gate Emitter Resistor	R_{GE}	−	T_J = −40°C to 150°C	10	16	26	kΩ

1. When surface mounted to an FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GE(th)}$	I_C = 1.0 mA, $V_{GE} = V_{CE}$	T_J = 25°C	1.1	1.56	1.9	V_{DC}
			T_J = 150°C	0.75	1.08	1.4	
			T_J = −40°C	1.2	1.75	2.1	
Collector−to−Emitter On−Voltage	$V_{CE(on)}$	I_C = 7 A, V_{GE} = 4.5 V	T_J = −40°C to 150°C	1.10	1.84	2.30	V
		I_C = 7 A, V_{GE} = 4.0 V	T_J = −40°C to 150°C	1.15	1.89	2.35	
		I_C = 7 A, V_{GE} = 3.7 V	T_J = −40°C to 150°C	1.20	1.93	2.50	
		I_C = 10 A, V_{GE} = 4.5 V	T_J = −40°C to 150°C	1.45	2.07	2.65	
		I_C = 10 A, V_{GE} = 4.0 V	T_J = −40°C to 150°C	1.50	2.13	2.80	
		I_C = 10 A, V_{GE} = 3.7 V	T_J = −40°C to 150°C	1.55	2.19	2.85	
		I_C = 10 mA, V_{GE} = 4.5 V	T_J = −40°C to 150°C	−	0.65	1.00	
Threshold Temperature Coefficient (Negative)	−	−	−	−	3.5	−	mV/°C
Forward Transconductance	gfs	V_{CE} = 5.0 V, I_C = 6.0 A	T_J = −40°C to 150°C	6.0	14	25	Mhos
DYNAMIC CHARACTERISTICS (Note 2)							
Input Capacitance	C_{ISS}	V_{CC} = 25 V, V_{GE} = 0 V f = 1.0 MHz	T_J = −40°C to 150°C	400	780	1000	pF
Output Capacitance	C_{OSS}			50	72	100	
Transfer Capacitance	C_{RSS}			4.0	6	10	
SWITCHING CHARACTERISTICS (Note 2)							
Turn−Off Delay Time	$t_{d(off)}$	V_{CC} = 300 V, V_{GE} = 5 V R_G = 1.0 kΩ, R_L = 46 Ω,	T_J = 25°C	1.0	2.9	12	μSec
Fall Time	t_f	V_{CC} = 300 V, V_{GE} = 5 V R_G = 1.0 kΩ, R_L = 46 Ω,	T_J = 25°C	1.0	2.5	7.0	
Turn−On Delay Time	$t_{d(on)}$	V_{CC} = 14 V, V_{GE} = 5 V R_G = 1.0 kΩ, R_L = 1 Ω	T_J = 25°C	0.1	0.42	1.4	μSec
Rise Time	t_r	V_{CC} = 14 V, V_{GE} = 5 V R_G = 1.0 kΩ, R_L = 1 Ω	T_J = 25°C	1.0	2.5	9.0	

2. Electrical Characteristics at temperature other than 25°C, Dynamic and Switching characteristics are not subject to production testing. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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Publication Order Number:
NGD18N45CLB/D

TYPICAL ELECTRICAL CHARACTERISTICS (unless otherwise noted)

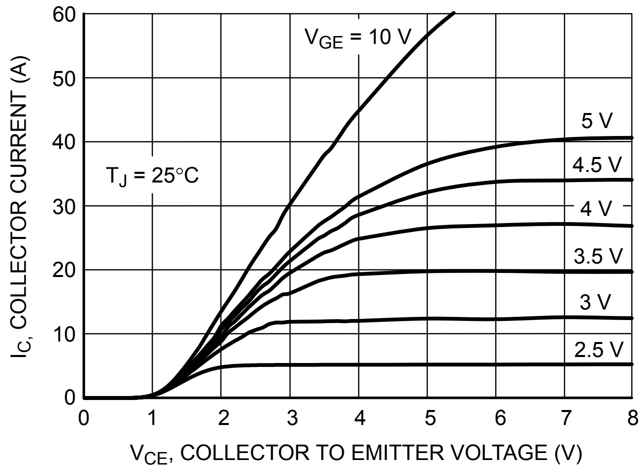


Figure 1. Output Characteristics

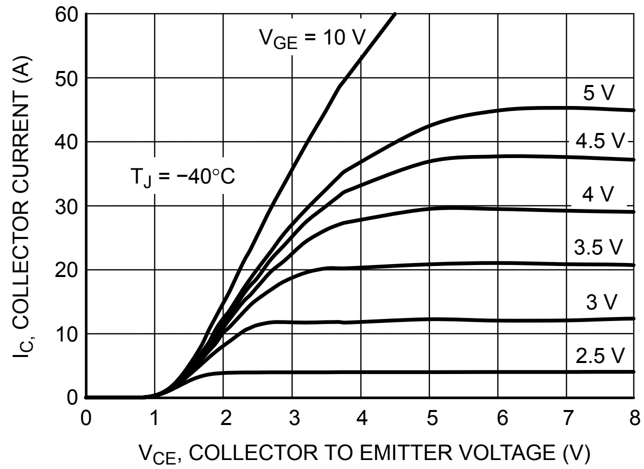


Figure 2. Output Characteristics

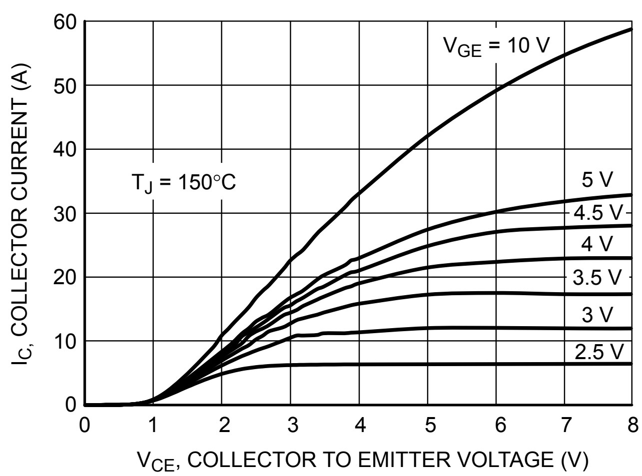


Figure 3. Output Characteristics

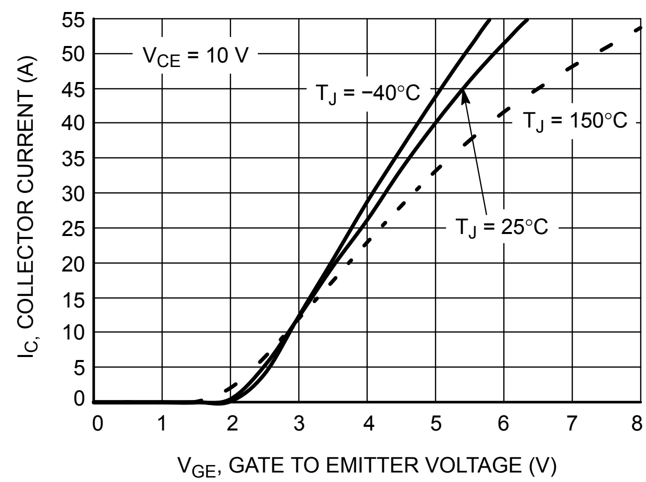


Figure 4. Transfer Characteristics

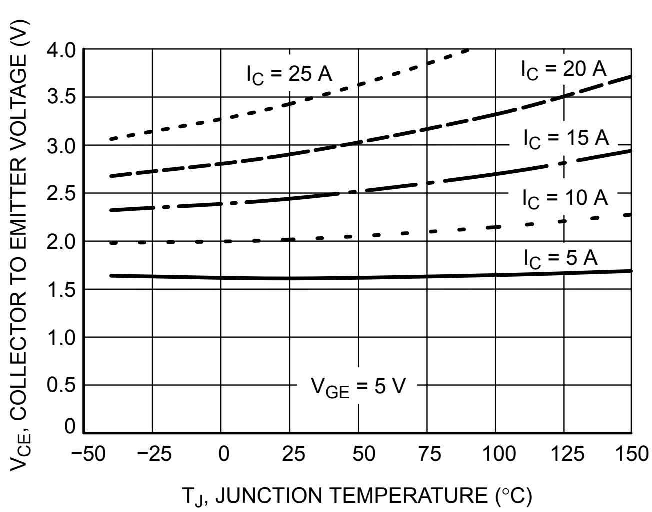


Figure 5. Collector−to−Emitter Saturation Voltage vs. Junction Temperature

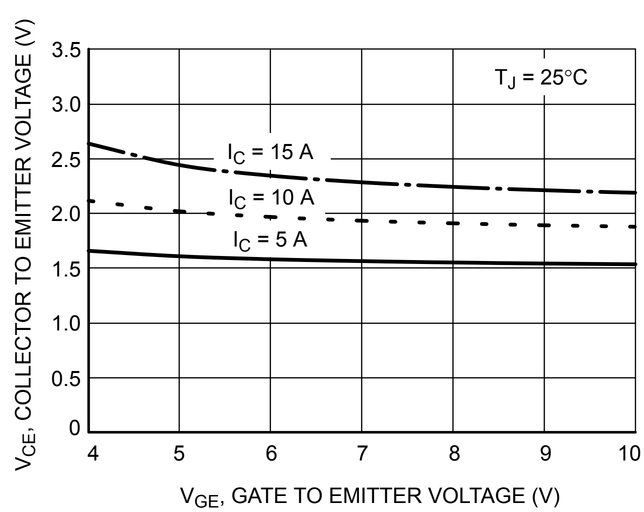


Figure 6. Collector−to−Emitter Voltage vs. Gate−to−Emitter Voltage

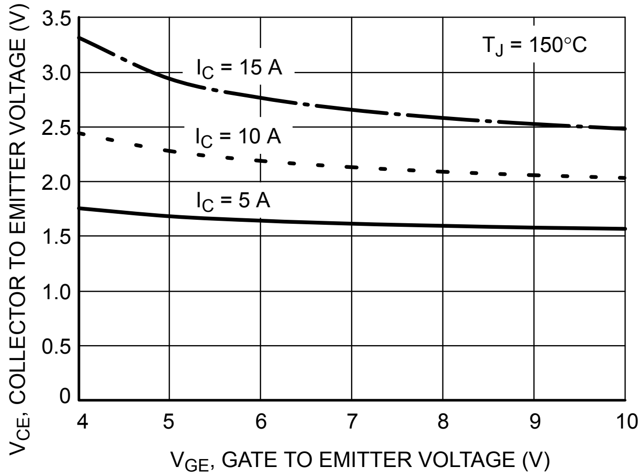


Figure 7. Collector−to−Emitter Voltage vs. Gate−to−Emitter Voltage

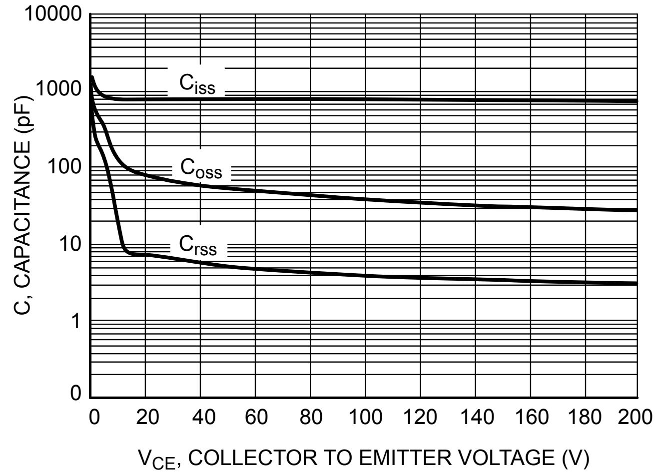


Figure 8. Capacitance Variation

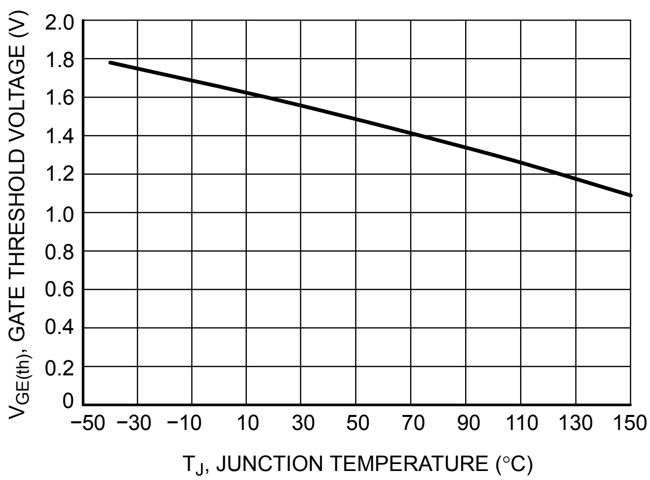


Figure 9. Gate Threshold Voltage vs. Junction Temperature

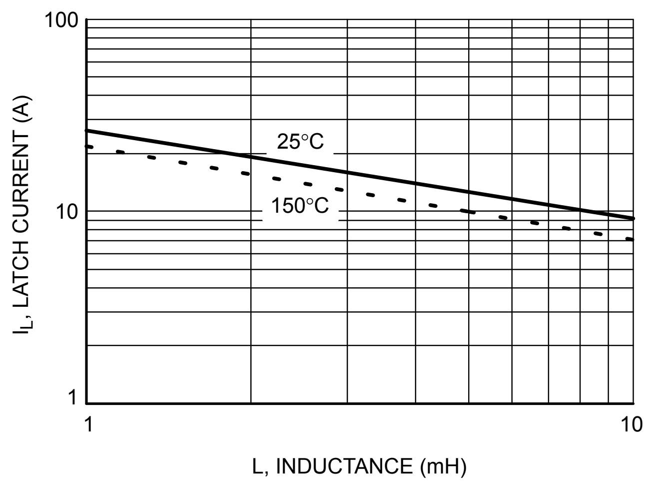


Figure 10. Minimum Open Secondary Latch Current vs. Inductance

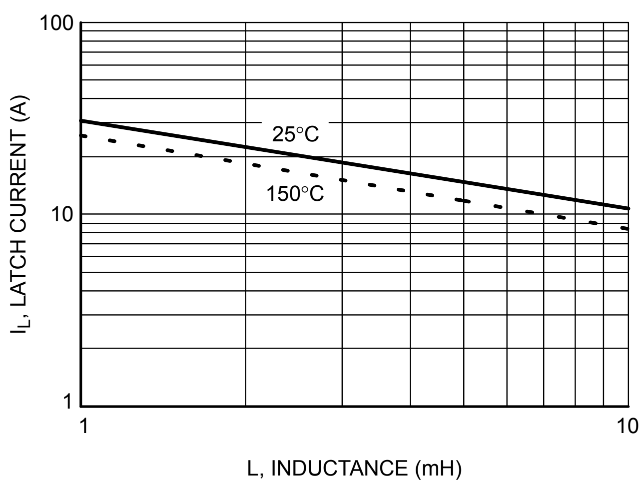


Figure 11. Typical Open Secondary Latch Current vs. Inductance

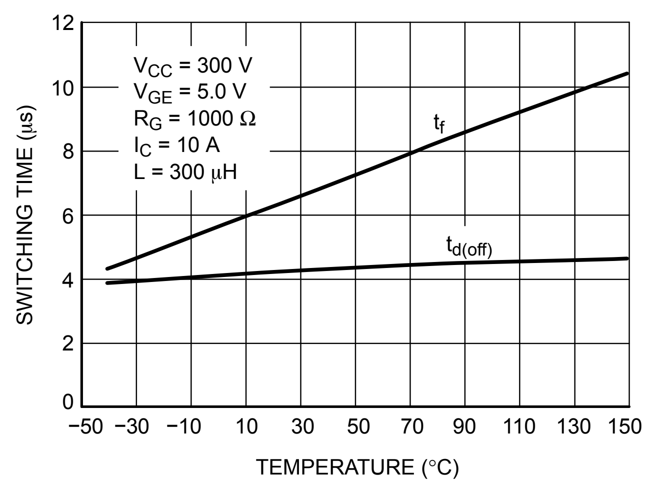


Figure 12. Inductive Switching Fall Time vs. Temperature

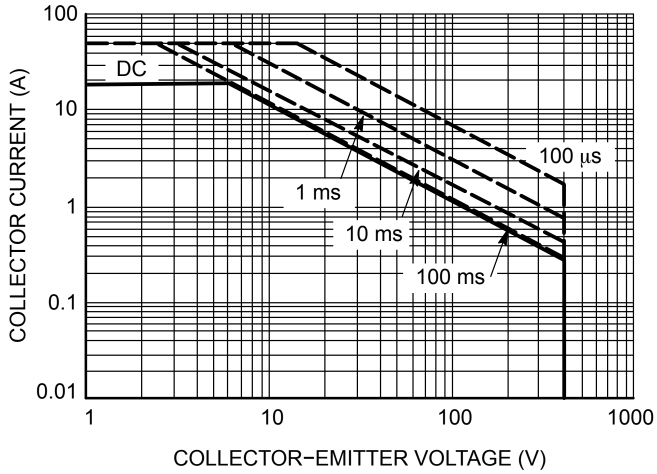


Figure 13. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at T_A = 25°C)

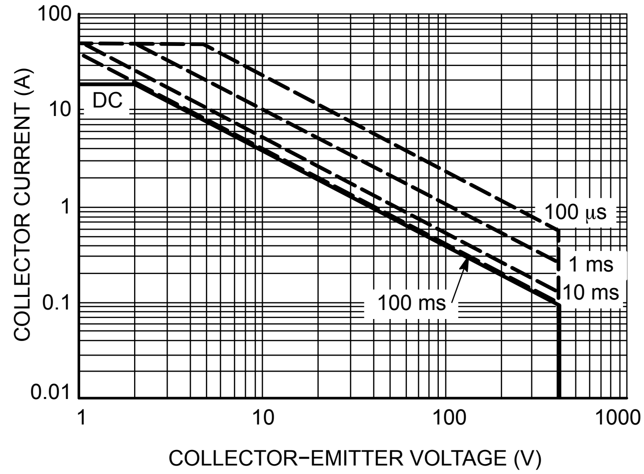


Figure 14. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at T_A = 125°C)

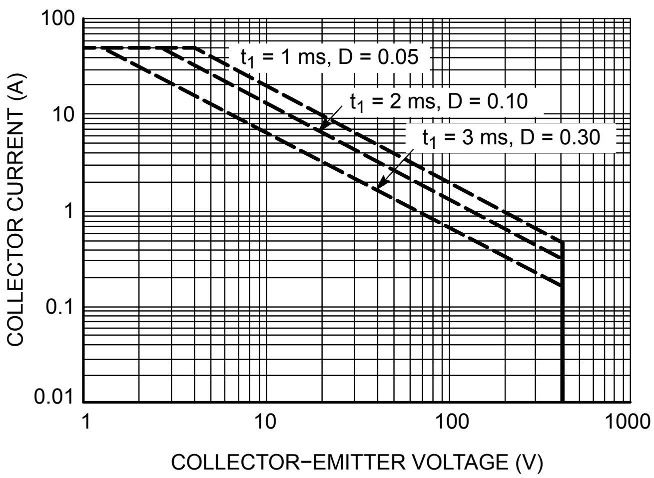


Figure 15. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at T_C = 25°C)

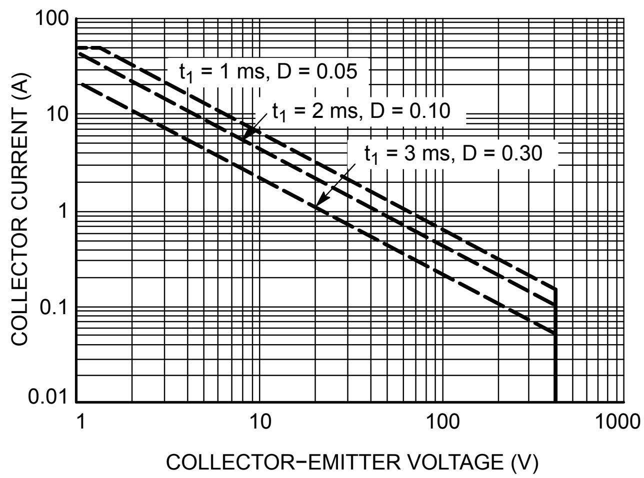


Figure 16. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at T_C = 125°C)

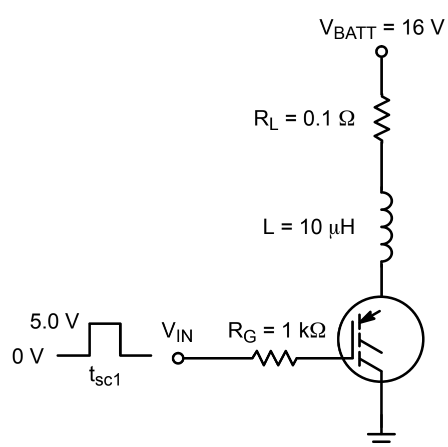


Figure 17. Circuit Configuration for Short Circuit Test #1

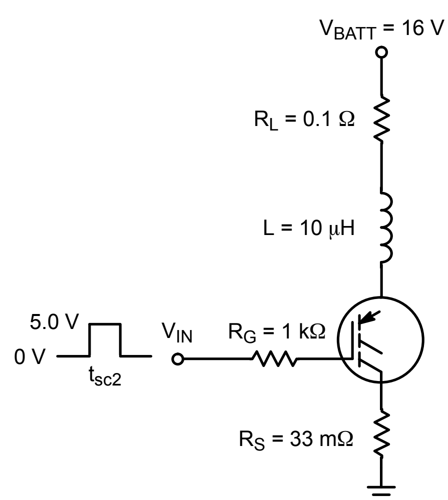


Figure 18. Circuit Configuration for Short Circuit Test #2

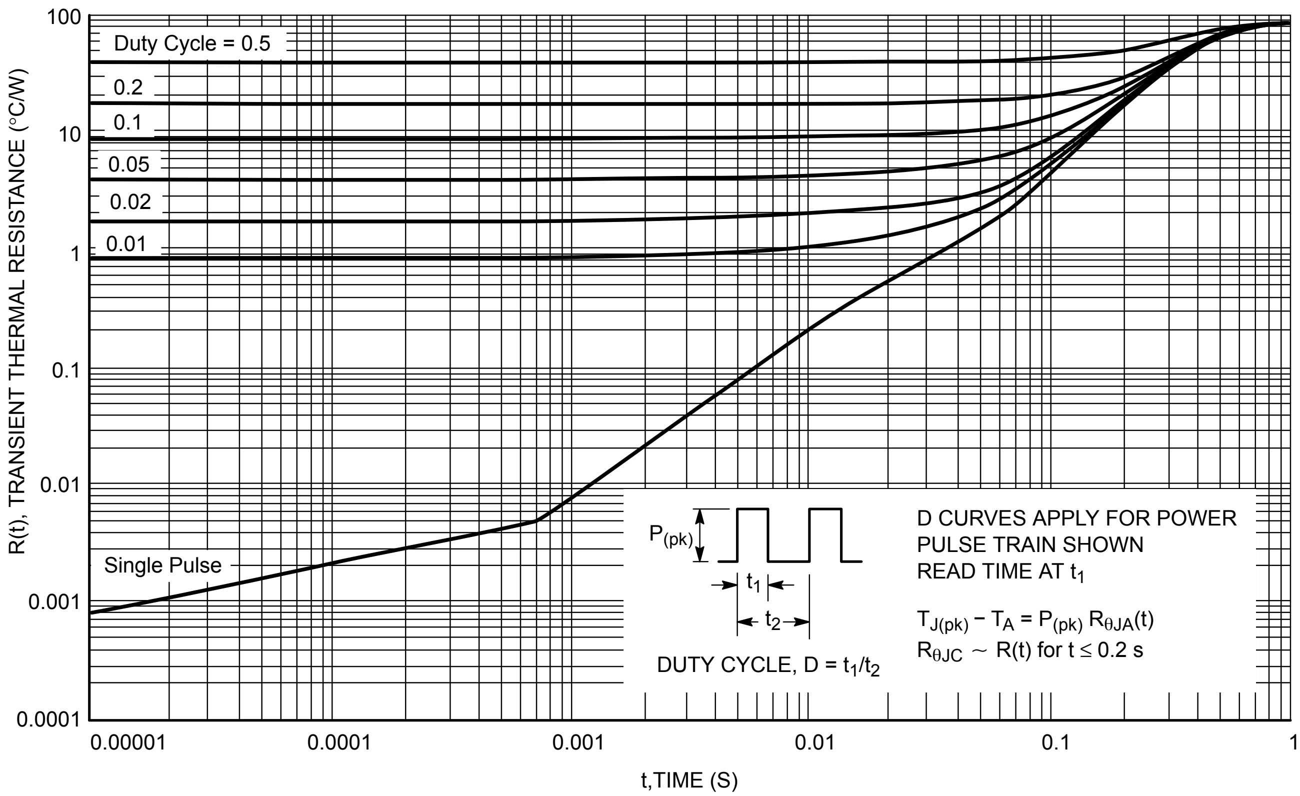
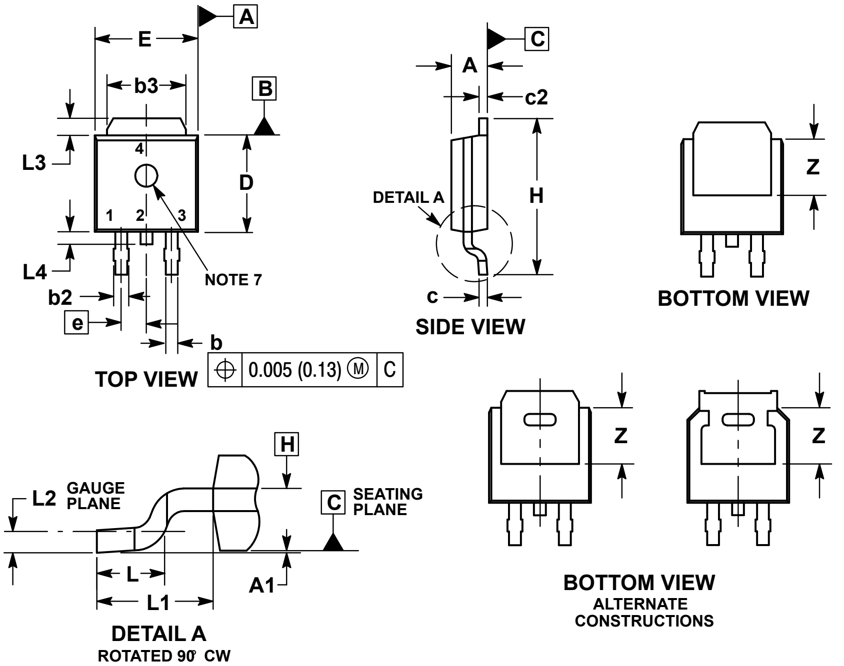


Figure 19. Transient Thermal Resistance
(Non−normalized Junction−to−Ambient mounted on minimum pad area)

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

SOLDERING FOOTPRINT*