



# DIFFERENTIAL-TO-3.3V, 2.5V LVPECL BUFFER/ DIVIDER W/INTERNAL TERMINATION

**ICS889871**

## GENERAL DESCRIPTION

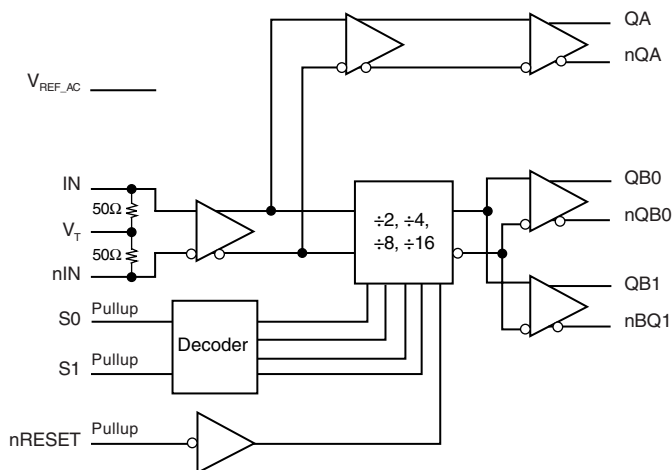


The ICS889871 is a high speed Differential-to-3.3V, 2.5V LVPECL Buffer/Divider w/Internal Termination and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. The ICS889871 has a selectable  $\div 2$ ,  $\div 4$ ,  $\div 8$ ,  $\div 16$  output dividers. The clock input has internal termination resistors, allowing it to interface with several differential signal types while minimizing the number of required external components. The device is packaged in a small, 3mm x 3mm VFQFN package, making it ideal for use on space-constrained boards.

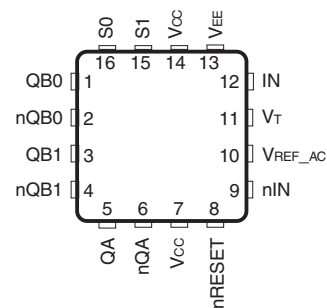
## FEATURES

- Three LVPECL outputs
- Frequency divide select options:  $\div 2$ ,  $\div 4$ ,  $\div 8$ ,  $\div 16$
- IN, nIN input can accept the following differential input levels: LVPECL, LVDS, CML
- Output frequency: 2GHz (typical)
- Additive phase jitter, RMS: 0.26ps (typical)
- Output skew: 7ps (typical), QB outputs
- Part-to-part skew: 250ps (maximum)
- Propagation Delay: 535ps (typical), QA/nQA outputs
- Supply voltage range: (LVPECL), 2.375V to 3.465V  
Supply voltage range: (ECL), -3.465V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) compliant packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**ICS889871**  
**16-Lead VFQFN**  
 3mm x 3mm x 0.95 package body  
**K Package**  
 Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	QB0, nQB0	Output		Differential output pair. LVPECL / ECL interface levels.
3, 4	QB1, nQB1	Output		Differential output pair. LVPECL / ECL interface levels.
5, 6	QA, nQA	Output		Differential output pair. LVPECL / ECL interface levels.
7, 14	$V_{CC}$	Power		Positive supply pins.
8	nRESET	Input	Pullup	Synchronizing enable/disable pin. When LOW, resets the divider. When HIGH, unconnected. Input threshold is $V_{CC}/2V$ . Includes a 37k $\Omega$ pull-up resistor. See Table 3A. LVTTTL / LVCMOS interface levels.
9	nIN	Input		Inverting differential clock input. 50 $\Omega$ internal input termination to $V_T$ .
10	$V_{REF\_AC}$	Output		Reference voltage for AC-coupled applications.
11	$V_T$	Input		Termination input.
12	IN	Input		Non-inverting differential clock input. 50 $\Omega$ internal input termination to $V_T$ .
13	$V_{EE}$	Power		Negative supply pin.
15, 16	S1, S0	Input	Pullup	Output divider select pins. See Table 3B. LVCMOS/LVTTTL interface levels.

NOTE: *Pullup* refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLUP}$	Input Pullup Resistor			37		k $\Omega$

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Input	Outputs	
nRESET	QB0, QB1	nQB0, nQB1
0	Disabled; LOW	Disabled; HIGH
1	Enabled	Enabled

NOTE: After nRESET switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in Figure 1.

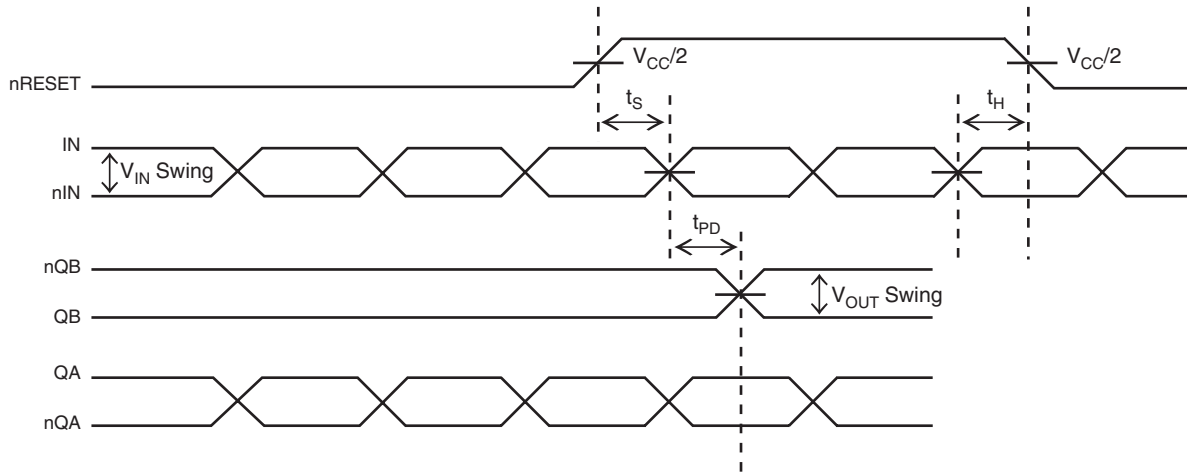


FIGURE 1. nRESET TIMING DIAGRAM

TABLE 3B. TRUTH TABLE

Inputs			Outputs	
nRESET	S1	S0	Bank A	Bank B
1	0	0	Input Clock	Input Clock ÷2
1	0	1	Input Clock	Input Clock ÷4
1	1	0	Input Clock	Input Clock ÷8
1	1	1	Input Clock	Input Clock ÷16
0	X	X	Input Clock	QB = LOW, nQB = HIGH

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{CC}$	-0.5V to +4.0V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5$ V
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Input Current $I_N$ , $nIN$	$\pm 50$ mA
$V_T$ Current, $I_{VT}$	$\pm 100$ mA
$V_{REF\_AC}$ Sink/Source, $I_{VREF\_AC}$	$\pm 0.5$ mA
Operating Temperature Range, $T_A$	-40°C to +85°C
Storage Temperature, $T_{STG}$	-65°C to 150°C
Package Thermal Impedance, $\theta_{JA}$ (Junction-to-Ambient)	51.5°C/W (0 lfpm)

**NOTE:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 10\%$  OR  $2.5V \pm 5\%$ ;  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Positive Supply Voltage		2.375	3.3	3.63	V
$I_{EE}$	Power Supply Current				60	mA
$R_{IN}$	Differential Input Resistance	( $I_N$ , $nIN$ )	40	50	60	$\Omega$
$V_{IH}$	Input High Voltage	( $I_N$ , $nIN$ )	1.2		$V_{CC}$	V
$V_{IL}$	Input Low Voltage	( $I_N$ , $nIN$ )	0		$V_{CC} - 0.15$	V
$V_{IN}$	Input Voltage Swing		0.15		2.8	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing		0.3			V
$I_{IN}$	Input Current	( $I_N$ , $nIN$ )			45	mA
$V_{REF\_AC}$	Bias Voltage			$V_{CC} - 1.35$		V

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 10\%$  OR  $2.5V \pm 5\%$ ;  $T_A = -40^\circ\text{C}$  TO  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{CC} = 3.3V$	2		$V_{CC} + 0.3$	V
		$V_{CC} = 2.5V$	1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{CC} = 3.3V$	0		0.8	V
		$V_{CC} = 2.5V$	0		0.7	V
$I_{IH}$	Input High Current	$V_{CC} = V_{IN} = 3.63V$ or $2.625V$	-125		20	$\mu\text{A}$
$I_{IL}$	Input Low Current	$V_{CC} = 3.63V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu\text{A}$

TABLE 4C. LVPECL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 10\%$  OR  $2.5V \pm 5\%$ ;  $T_A = -40^\circ C$  TO  $85^\circ C$ 

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.125$	$V_{CC} - 1.005$	$V_{CC} - 0.935$	mV
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 1.895$	$V_{CC} - 1.78$	$V_{CC} - 1.67$	mV
$V_{OUT}$	Output Voltage Swing		0.6		1.0	mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing		1.2		2.0	V

Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.925V to -0.5V.

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .

TABLE 5. AC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 10\%$  OR  $2.5V \pm 5\%$ ;  $T_A = -40^\circ C$  TO  $85^\circ C$ 

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
$f_{MAX}$	Maximum Output Frequency	Output Swing $\geq 450mV$		2.0		GHz
	Maximum Input Frequency	$\div 2, \div 4, \div 8, \div 16$		2.5		GHz
$t_{PD}$	Propagation Delay, (Differential); NOTE 1	QA/nQA	300	535	800	ps
		QB/nQB	450	700	975	ps
$tsk(o)$	Output Skew; NOTE 2, 3	QB0-to-QB1		7	21	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 3, 5				250	ps
$t_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	155.25MHz, Integration Range: 12kHz-20MHz		0.26		ps
$t_R/t_F$	Output Rise/Fall Time	20% - 80%	100		380	ps
$t_S/t_H$	Clock Enable Setup/Hold Time	nRESET to IN/nIN	300			ps
odc	Output Duty Cycle	QA/nQA	48		52	%
		QB/nQB	47		53	%

All parameters characterized at  $\leq 1GHz$  unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

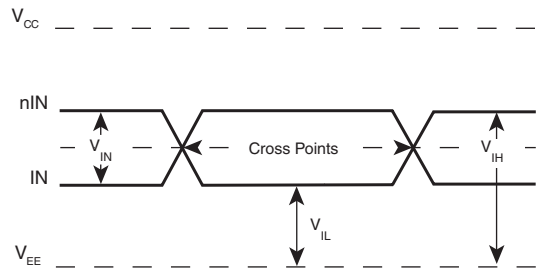
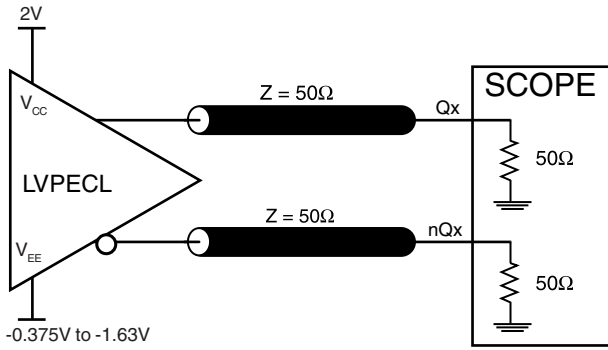
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

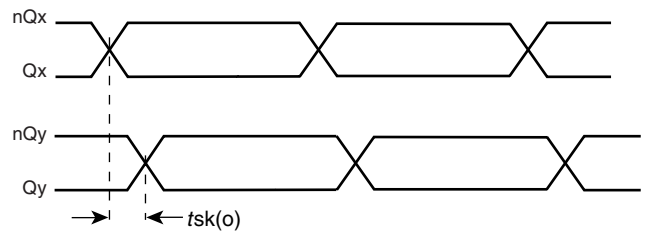
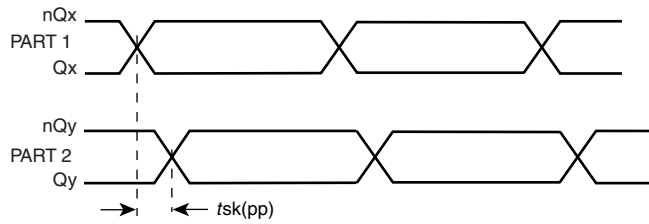
NOTE 5: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

# PARAMETER MEASUREMENT INFORMATION



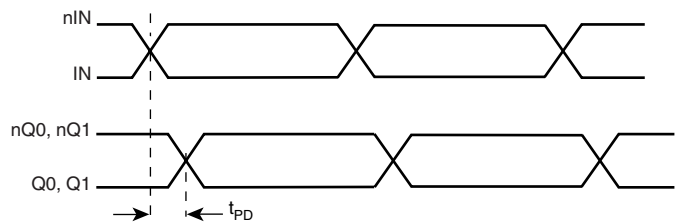
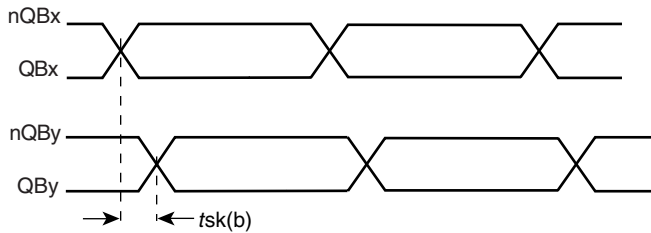
**OUTPUT LOAD AC TEST CIRCUIT**

**DIFFERENTIAL INPUT LEVEL**



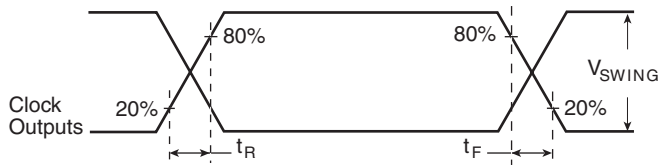
**PART-TO-PART SKEW**

**OUTPUT SKEW**



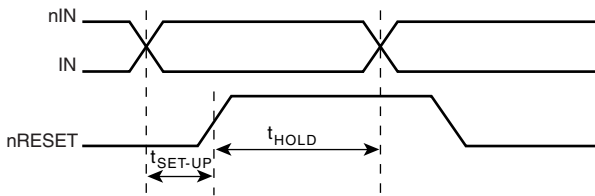
**BANK SKEW**

**PROPAGATION DELAY**



OUTPUT RISE/FALL TIME

SINGLE ENDED & DIFFERENTIAL INPUT VOLTAGE SWING



SETUP & HOLD TIME

## APPLICATION INFORMATION

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### SELECT PINS:

All select pins have internal pull-ups and pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

#### OUTPUTS:

##### LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

### 3.3V LVPECL INPUT WITH BUILT-IN 50 $\Omega$ TERMINATIONS INTERFACE

The IN/nIN with built-in 50 $\Omega$  terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 2A to 2E show interface examples for the HiPerClockS IN/nIN input with built-in 50 $\Omega$  terminations driven by the most common

driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

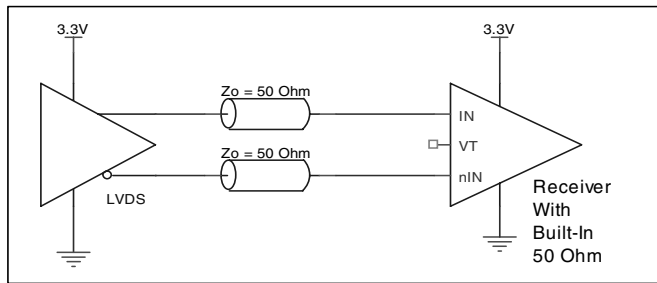


FIGURE 2A. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50 $\Omega$  DRIVEN BY AN LVDS DRIVER

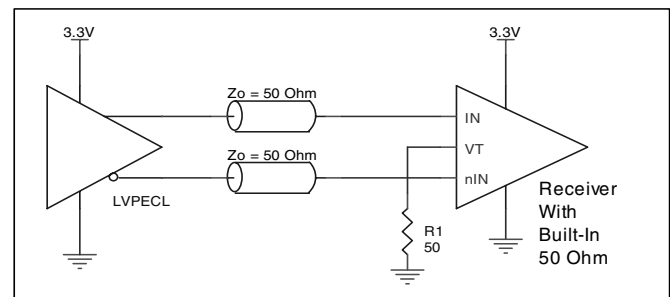


FIGURE 2B. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50 $\Omega$  DRIVEN BY AN LVPECL DRIVER

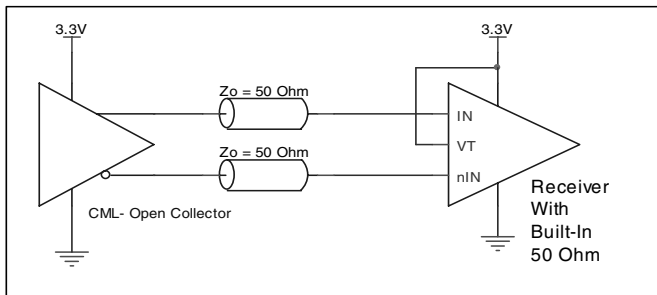


FIGURE 2C. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50 $\Omega$  DRIVEN BY A CML DRIVER WITH OPEN COLLECTOR

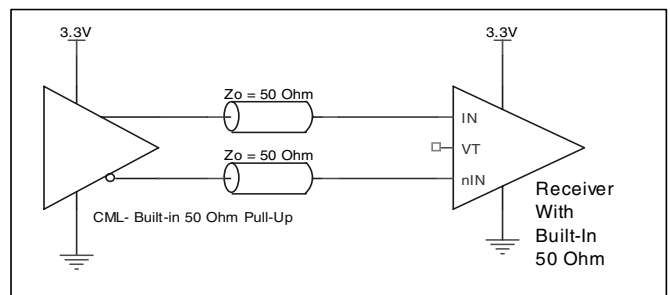


FIGURE 2D. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50 $\Omega$  DRIVEN BY A CML DRIVER WITH BUILT-IN 50 $\Omega$  PULLUP

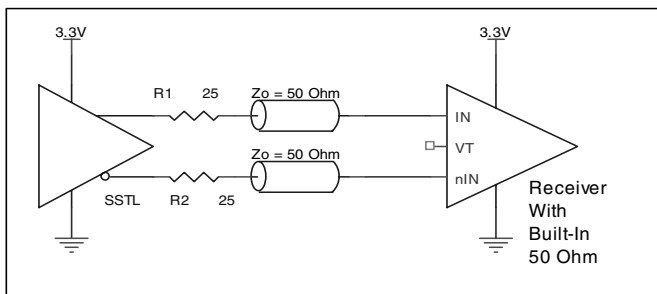


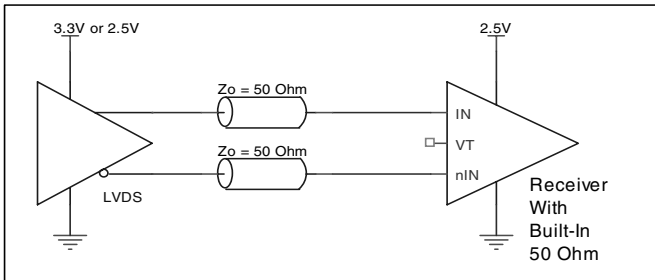
FIGURE 2E. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50 $\Omega$  DRIVEN BY AN SSTL DRIVER



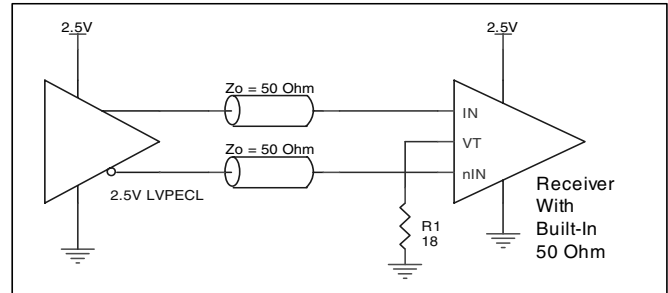
## 2.5V LVPECL INPUT WITH BUILT-IN 50Ω TERMINATIONS INTERFACE

The IN/nIN with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both  $V_{\text{SWING}}$  and  $V_{\text{OH}}$  must meet the  $V_{\text{PP}}$  and  $V_{\text{CMR}}$  input requirements. Figures 3A to 3E show interface examples for the HiPerClockS IN/nIN input with built-in 50Ω terminations driven by the most

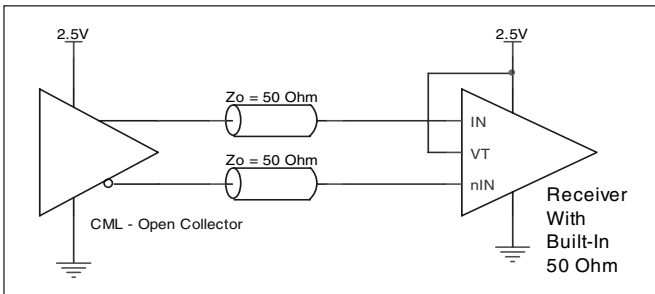
common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



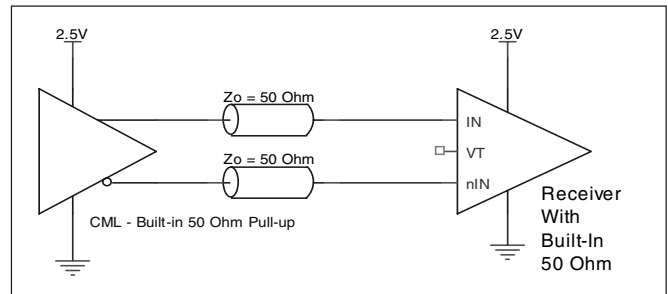
**FIGURE 3A. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER**



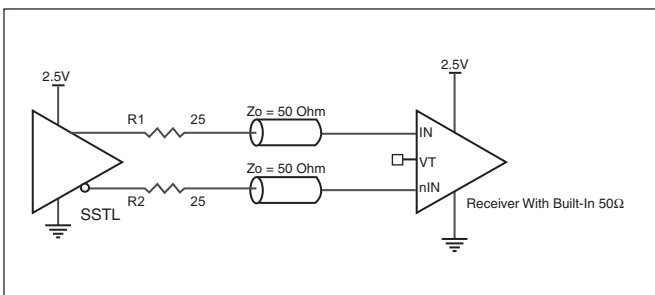
**FIGURE 3B. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER**



**FIGURE 3C. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN OPEN COLLECTOR CML DRIVER**



**FIGURE 3D. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP**



**FIGURE 3E. HiPerClockS IN/nIN INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER**

### TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

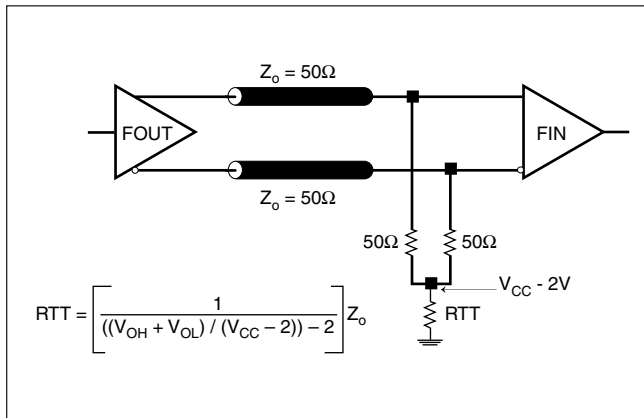


FIGURE 4A. LVPECL OUTPUT TERMINATION

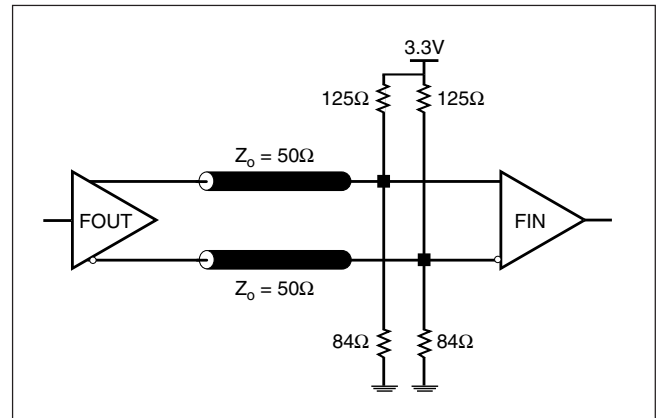
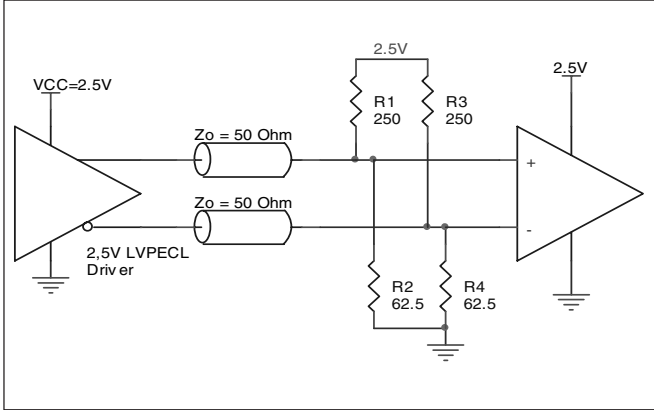


FIGURE 4B. LVPECL OUTPUT TERMINATION

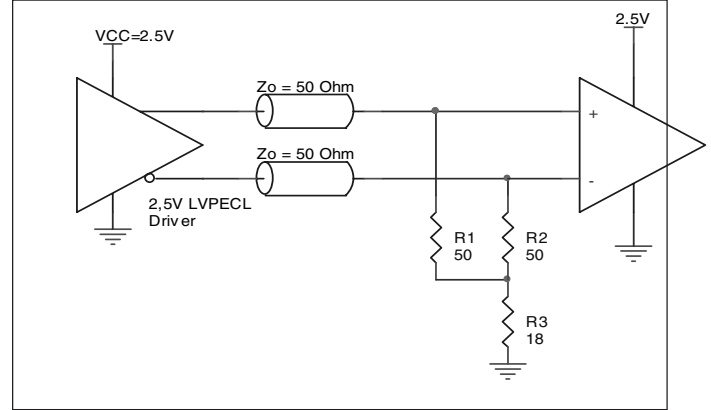
**TERMINATION FOR 2.5V LVPECL OUTPUT**

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{cc} - 2V$ . For  $V_{cc} = 2.5V$ , the  $V_{cc} - 2V$  is very close to ground

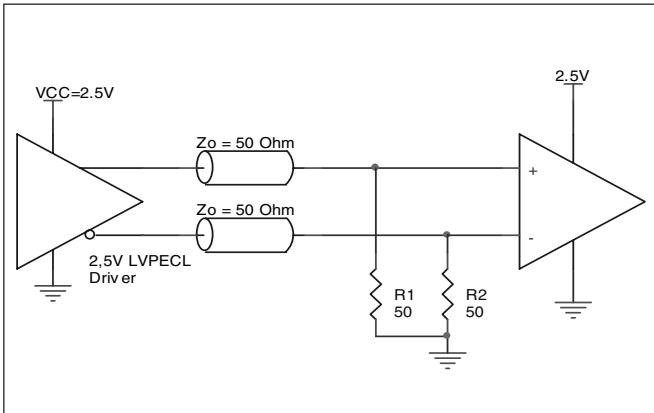
level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.



**FIGURE 5A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**



**FIGURE 5B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE**



**FIGURE 5C. 2.5V LVPECL TERMINATION EXAMPLE**

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS889871. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS889871 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V \pm 10\% = 3.63V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.63V * 55mA = 199.65mW$
- Power (outputs)<sub>MAX</sub> = **30.94mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $3 * 30.94mW = 92.82mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 199.65mW + 92.82mW = 292.47mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 0 linear feet per minute and a multi-layer board, the appropriate value is 51.5°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ C + 0.293W * 51.5^\circ C/W = 100.1^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

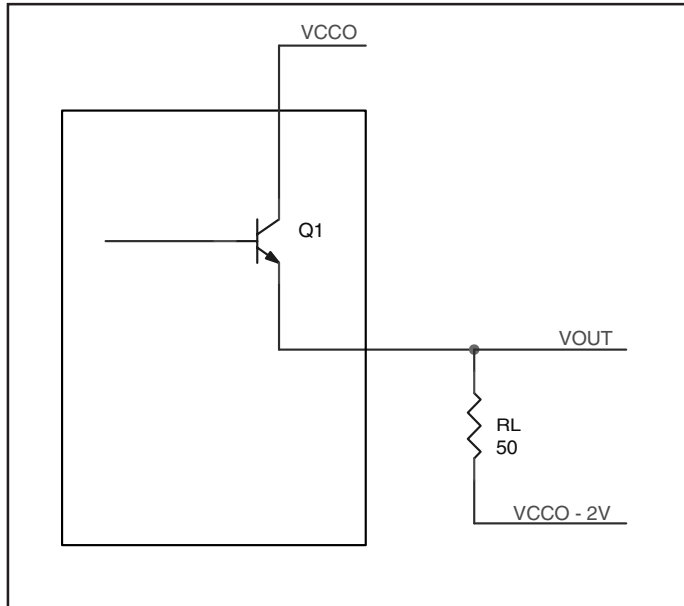
**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 16-PIN VFQFN FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)	
	<b>0</b>
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*.



**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CC} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.935V$

$$(V_{CC\_MAX} - V_{OH\_MAX}) = 0.935V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.67V$

$$(V_{CC\_MAX} - V_{OL\_MAX}) = 1.67V$$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - 0.935V)/50\Omega] * 0.935V = 19.92mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - 1.67V)/50\Omega] * 1.67V = 11.2mW$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = 30.94mW$

## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  vs. AIR FLOW TABLE FOR 16 LEAD VFQFN

$\theta_{JA}$ vs. 0 Air Flow (Linear Feet per Minute)	
Multi-Layer PCB, JEDEC Standard Test Boards	51.5°C/W

### TRANSISTOR COUNT

The transistor count for ICS889871 is: 429

Pin compatible with SY89871U

PACKAGE OUTLINE - K SUFFIX FOR 16 LEAD VFQFN

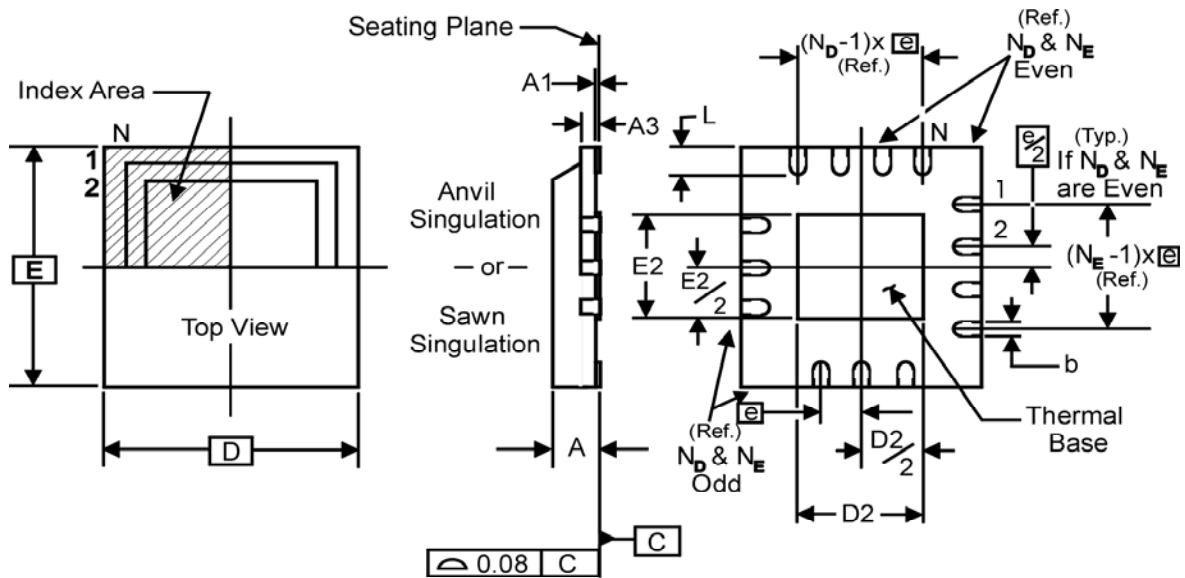


TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS		
SYMBOL	MINIMUM	MAXIMUM
N	16	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
$N_D$	4	
$N_E$	4	
D	3.0	
D2	0.25	1.25
E	3.0	
E2	0.25	1.25
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS889871AK	871A	16 Lead VFQFN	tube	-40°C to 85°C
ICS889871AKT	871A	16 Lead VFQFN	2500 tape & reel	-40°C to 85°C
ICS889871AKLF	71AL	16 Lead "Lead-Free" VFQFN	tube	-40°C to 85°C
ICS889871AKLFT	71AL	16 Lead "Lead-Free" VFQFN	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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