### **General Description**

The MAX4838A/MAX4840A/MAX4842A are overvoltageprotection ICs that protect low-voltage systems against voltages of up to +28V. If the input voltage exceeds the overvoltage trip level, the MAX4838A/MAX4840A/ MAX4842A turn off the low-cost external n-channel FET(s) to prevent damage to the protected components. An internal charge pump eliminates the need for external capacitors and drives the FET gate for a simple, robust solution.

The MAX4838A has a 7.4V overvoltage threshold, and the MAX4840A has a 5.8V overvoltage threshold. The MAX4842A has a 4.7V overvoltage threshold. The MAX4838A/MAX4840A have an undervoltage-lockout (UVLO) threshold of 3.25V, while the MAX4842A has a UVLO of 2.5V. In addition to the single FET configuration, the devices can be configured with back-to-back external FETs to prevent currents from being back-driven into the adapter.

On power-up, the device waits for 50ms before driving GATE high. FLAG is held low for an additional 50ms after GATE goes high before deasserting. The MAX4838A/MAX4840A/MAX4842A have an open-drain FLAG output. The FLAG output asserts immediately to an overvoltage fault.

Additional features include a  $\pm 15 kV$  (HBM) ESD-protected input (when bypassed with a 1µF capacitor) and a shutdown pin ( $\overline{EN}$ ) to turn off the device.

All devices are offered in a small 6-pin SC70 and 6-pin 1.5mm x 1.0mm  $\mu$ DFN packages and are specified over the -40°C to +85°C extended temperature range.

Cell Phones Digital Still Cameras PDAs and Palmtop Devices MP3 Players

### **Selector Guide**

**Applications** 

PART	UVLO THRESHOLD (V)	OV TRIP LEVEL (V)	En INPUT	FLAG OUTPUT
MAX4838A	3.25	7.4	Yes	Open-Drain
MAX4840A	3.25	5.8	Yes	Open-Drain
MAX4842A	2.50	4.7	Yes	Open-Drain

### Features

- Overvoltage Protection Up to +28V
- Preset 7.4V, 5.8V, or 4.7V Overvoltage Trip Level
- Drives Low-Cost nMOS FET
- Internal 50ms Startup Delay
- Internal Charge Pump
- Undervoltage Lockout
- ±15kV ESD-Protected Input
- ♦ Voltage Fault FLAG Indicator
- ♦ 6-Pin SC70 and µDFN Packages
- Lead Free

### **Ordering Information**

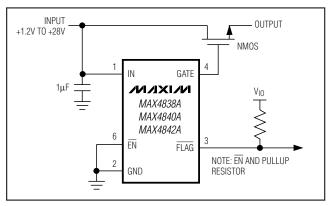
PART	PIN- PACKAGE	TOP MARK	PKG CODE
MAX4838AEXT+T	6 SC70	ACY	X6S-1
MAX4838AELT+	6 µDFN	KU	L611-1
MAX4840AEXT+T	6 SC70	ACZ	X6S-1
MAX4840AELT+	6 µDFN	KV	L611-1
MAX4842AEXT+T	6 SC70	ADA	X6S-1
MAX4842AELT+*	6 µDFN	KW	L611-1

**Note:** All devices specified for the -40°C to +85°C extended temperature range.

\*Future product—contact factory for availability.

+Denotes lead-free package.

### **Typical Operating Circuit**



Pin Configuration appears at end of data sheet.

### 

Maxim Integrated Products 1

**ation PKG CODE** X6S-1 L611-1 X6S-1 L611-1 X6S-1 L611-1 anded

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

### **ABSOLUTE MAXIMUM RATINGS**

IN to GND	0.3V to +30V
GATE to GND	0.3V to +12V
EN, FLAG to GND	0.3V to +6V
Continuous Power Dissipation ( $T_A = +70^{\circ}C$ )	
6-Pin SC70 (derate 3.1mW/°C above +70°C	C)245mW
6-Pin µDFN (derate 2.1mW/°C above +70°C	C)477mW

Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 1	0s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### **ELECTRICAL CHARACTERISTICS**

(VIN = +5V (MAX4838A/MAX4840A), VIN = +4V (MAX4842A), T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	ТҮР	MAX	UNITS	
Input Voltage Range	VIN			1.2		28.0	V	
			MAX4838A/MAX4840A	3.0	3.25	3.5		
Undervoltage-Lockout Threshold	UVLO	V <sub>IN</sub> falling	MAX4842A	2.3	2.5	2.7	V	
Undervoltage-Lockout Hysteresis					50		mV	
		V <sub>IN</sub> rising	MAX4838A	7.0	7.4	7.8		
Overvoltage Trip Level	OVLO	V <sub>IN</sub> rising	MAX4840A	5.5	5.8	6.1	V	
		V <sub>IN</sub> rising	MAX4842A	4.4	4.7	5.0		
		MAX4838A			100			
Overvoltage Trip Level Hysteresis		MAX4840A			80		mV	
		MAX4842A			50			
IN Supply Current	la i	No load, <del>EN</del> = GND or 5V, V <sub>IN</sub> = 5V (MAX4838A/MAX4840A)			80	200	μA	
	lin	No load, $\overline{EN} = GND$ or 4.0V, V <sub>IN</sub> = 4V (MAX4842A)			75	160		
		V <sub>IN</sub> = 2.9V (MAX4838A/MAX4840A)				30		
UVLO Supply Current	IUVLO	V <sub>IN</sub> = 2.2V (MAX4842A)				22	μA	
0.175.1/1	VGATE		MAX4838A/MAX4840A	9		10	- V	
GATE Voltage		IGATE sourcing 1µA	MAX4842A	7.5		8.0		
GATE Pulldown Current	IPD	V <sub>IN</sub> > V <sub>OVLO</sub> , V <sub>GATE</sub> = 5.5V			27		mA	
FLAG Output Low Voltage		FLAG asserted	$1.2V \le V_{IN} < UVLO,$ $I_{SINK} = 50 \mu A$			0.4	- V	
	V <sub>OL</sub>		V <sub>IN</sub> ≥ OVLO, I <sub>SINK</sub> = 1mA			0.4		
FLAG Output High Leakage	lон	$V_{\overline{FLAG}} = 5.5V, \overline{FLAG}$ deasserted				1	μA	
EN Input High Voltage	VIH			1.5			V	
EN Input Low Voltage	VIL					0.4	V	
EN Input Leakage	I <sub>LKG</sub>	$\overline{EN} = GND \text{ or } 5.5V$				1	μA	

### ELECTRICAL CHARACTERISTICS (continued)

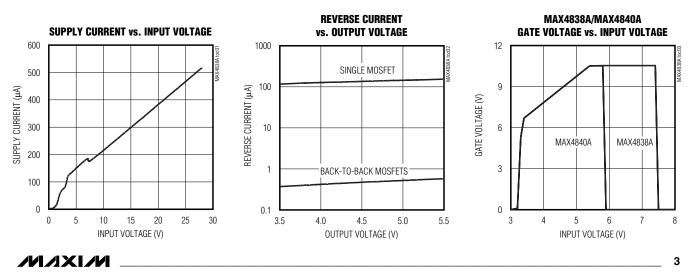
(V<sub>IN</sub> = +5V (MAX4838A/MAX4840A), V<sub>IN</sub> = +4V (MAX4842A), T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING		·				
Startup Delay	<b>t</b> START	V <sub>IN</sub> > V <sub>UVLO</sub> , V <sub>GATE</sub> > 0.3V, Figure 1	20	50	80	ms
FLAG Blanking Time	<b>t</b> BLANK	$V_{GATE} > 0.3V$ , $V_{\overline{FLAG}} > 2.4V$ , Figure 1	20	50	80	ms
GATE Turn-On Time	tgon				ms	
GATE Turn-Off Time	tgoff	$V_{IN}$ increasing from 5V to 8V at 3V/µs (MAX4838A/MAX4840A), $V_{IN}$ increasing from 4V to 6V at 3V/µs (MAX4842A), $V_{GATE} = 0.3V$ , $C_{GATE} = 1500$ pF, Figure 2	6		20	μs
FLAG Assertion Delay	<sup>t</sup> FLAG	$V_{IN}$ increasing from 5V to 8V at 3V/µs (MAX4838A/MAX4840A), $V_{IN}$ increasing from 4V to 6V at 3V/µs (MAX4842A), $V_{FLAG} = 0.4V$ , Figure 2	5.8		μs	
Initial Overvoltage Fault Delay	tovp	$V_{IN}$ increasing from 0 to 8V (MAX4838A/MAX4840A), $V_{IN}$ increasing from 0V to 6V (MAX4842A), $I_{GATE} = 80\%$ of $I_{PD}$ , Figure 3	1.5		μs	
Disable Time	tDIS	$V_{\overline{EN}} = 2.4V, V_{GATE} = 0.3V, Figure 4$ 2				μs

Note 1: All parts are 100% tested at +25°C. Electrical limits across the full temperature range are guaranteed by design and correlation.

### **Typical Operating Characteristics**

(V<sub>IN</sub> = +5V (MAX4838A/MAX4840A), V<sub>IN</sub> = +4V (MAX4842A); Si9936DY external MOSFET in back-to-back configuration;  $T_A$  = +25°C, unless otherwise noted.)



### **Typical Operating Characteristics (continued)**

5V

0V

10V

0V

5V

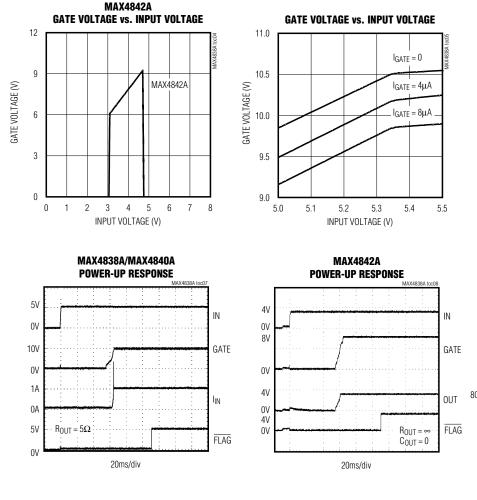
0V

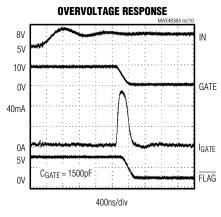
5V

 $R_{OUT} = \infty$ 

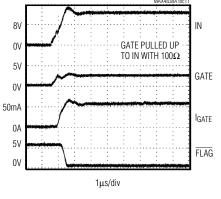
 $C_{OUT} = 0$ 

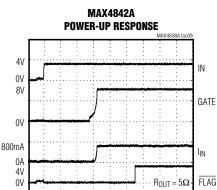
 $(V_{IN} = +5V (MAX4838A/MAX4840A), V_{IN} = +4V (MAX4842A); Si9936DY external MOSFET in back-to-back configuration; T_A = +25°C, unless otherwise noted.)$ 











20ms/div

MAX4838A/MAX4840A

**POWER-UP RESPONSE** 

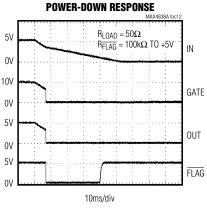
IN

GATE

OUT

FLAG







### \_Pin Description

PIN	NAME	FUNCTION		
1	1 IN Input. IN is both the power-supply input and the overvoltage sense input. In a $1\mu$ F capacitor or larger.			
2	GND	Ground		
3	FLAG	Fault Indication Output, Open-Drain, Active Low. FLAG is asserted low during undervoltage-lockout and overvoltage-lockout conditions. FLAG is deasserted during normal operation.		
4	GATE	Gate-Drive Output. GATE is the output of an on-chip charge pump. When $V_{UVLO} < V_{IN} < V_{OVLO}$ , GATE is driven high to turn on the external n-channel MOSFET(s).		
5	N.C.	No Connection. Not internally connected for µDFN package. Connected to ground for SC70 6-pin package; connect to ground or leave unconnected.		
6	ĒN	Device Enable Input, Active Low. Drive EN low or connect to ground to allow normal device operation. Drive EN high to turn off the external MOSFET.		

### \_Timing Diagrams

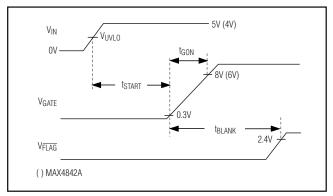


Figure 1. Startup Timing Diagram

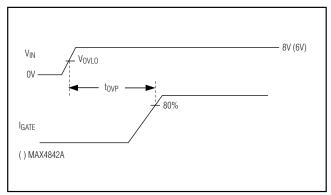
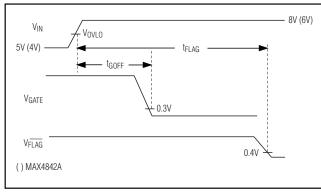
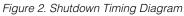


Figure 3. Power-Up Overvoltage Timing Diagram





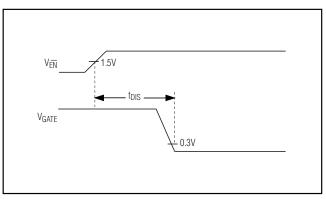


Figure 4. Disable Timing Diagram

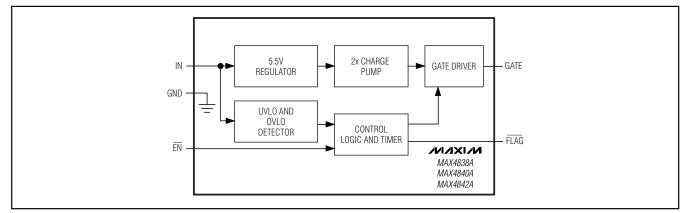


Figure 5. Functional Diagram

### \_Detailed Description

The MAX4838A/MAX4840A/MAX4842A provide up to +28V overvoltage protection for low-voltage systems. When the input voltage exceeds the overvoltage trip level, the MAX4838A/MAX4840A/MAX4842A turn off a low-cost external n-channel FET(s) to prevent damage to the protected components. An internal charge pump (Figure 5) drives the FET gate for a simple, robust solution.

### **Undervoltage Lockout (UVLO)**

The MAX4838A/MAX4840A have a fixed 3.25V typical undervoltage-lockout level (UVLO) while the MAX4842A has a 2.5V typical UVLO. When  $V_{IN}$  is less than the UVLO, the GATE driver is held low and FLAG is asserted.

### **Overvoltage Lockout (OVLO)**

The MAX4838A has a 7.4V typical overvoltage threshold (OVLO), and the MAX4840A has a 5.8V typical overvoltage threshold. The MAX4842A has a 4.7V typical overvoltage threshold. When  $V_{IN}$  is greater than OVLO, the GATE driver is held low and FLAG is asserted.

### **FLAG** Output

The FLAG output is used to signal the host system there is a fault with the input voltage. FLAG asserts immediately to an overvoltage fault. FLAG is held low for 50ms after GATE turns on before deasserting.

All devices have an open-drain FLAG output. Connect a pullup resistor from FLAG to the logic I/O voltage of the host system.

### **EN** Enable Input

 $\overline{\text{EN}}$  is an active-low enable input. Drive  $\overline{\text{EN}}$  low or connect to ground to enable normal device operation. Drive  $\overline{\text{EN}}$  high to force the external MOSFET(s) off.  $\overline{\text{EN}}$  does not override an OVLO or UVLO fault.

### **GATE** Driver

An on-chip charge pump is used to drive GATE above IN, allowing the use of low-cost n-channel MOSFETS. The charge pump operates from the internal 5.5V regulator.

The actual GATE output voltage tracks approximately two times V<sub>IN</sub> until V<sub>IN</sub> exceeds 5.5V or the OVLO trip level is exceeded, whichever comes first. The MAX4838A has a 7.4V typical OVLO; therefore GATE remains relatively constant at approximately 10.5V for  $5.5V < V_{IN} < 7.4V$ . The MAX4840A has a 5.8V typical OVLO, but this can be as low as 5.5V. The MAX4840A in practice may never actually achieve the full 10.5V GATE output. The MAX4842A has a 4.7V (typ) OVLO, and the GATE output voltage is 2x the input voltage. The GATE output voltage as a function of input voltage is shown in the *Typical Operating Characteristics*.

### **Device Operation**

The MAX4838A/MAX4840A/MAX4842A have an onboard state machine to control device operation. A flowchart is shown in Figure 6. On initial power-up, if  $V_{\rm IN}$  < UVLO or if  $V_{\rm IN}$  > OVLO, GATE is held at 0V, and FLAG is low.

If UVLO < V<sub>IN</sub> < OVLO and  $\overline{\text{EN}}$  is low, the device enters startup after a 50ms internal delay. The internal charge pump is enabled, and GATE begins to be driven above V<sub>IN</sub> by the internal charge pump. FLAG is held low during startup until the FLAG blanking period expires, typically 50ms after the GATE starts going high. At this point the device is in its on state.

At any time if  $V_{IN}$  drops below UVLO,  $\overline{FLAG}$  is driven low and GATE is driven to ground.



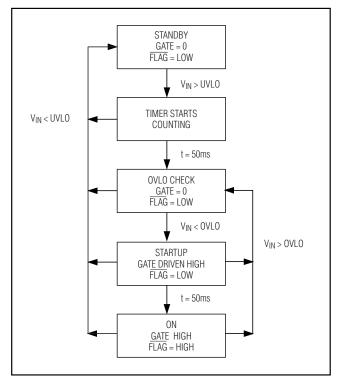


Figure 6. State Diagram

### **Applications Information**

### **MOSFET** Configuration

The MAX4838A/MAX4840A/MAX4842A can be used with either a single MOSFET configuration as shown in the *Typical Operating Circuit*, or can be configured with a back-to-back MOSFET as shown in Figure 7. The back-to-back configuration has almost zero reverse current when the input supply is below the output.

If reverse current leakage is not a concern, a single MOSFET can be used. This approach has half the loss of the back-to-back configuration when used with similar MOSFET types, and is a lower cost solution. Note that if the input is actually pulled low, the output is pulled low as well due to the parasitic body diode in the MOSFET. If this is a concern, then the back-to-back configuration should be used.

### **MOSFET Selection**

The MAX4838A/MAX4840A/MAX4842A are designed for use with either a single n-channel MOSFET or dual back-to-back n-channel MOSFETs. In most situations, MOSFETs with  $R_{DS(ON)}$  specified for a V<sub>GS</sub> of 4.5V work well. If the input supply is near the UVLO maximum of

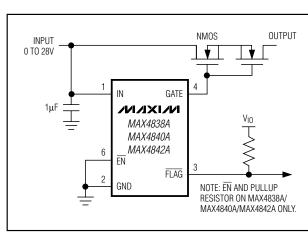


Figure 7. Back-to-Back External MOSFET Configuration

3.5V, consider using a MOSFET specified for a lower VGS voltage. Also, the VDS should be 30V for the MOSFET to withstand the full 28V IN range of all devices. Table 1 shows a selection of MOSFETs appropriate for use with the MAX4838A/MAX4840A/MAX4842A.

### **IN Bypass Considerations**

For most applications, bypass IN to GND with a  $1\mu$ F ceramic capacitor. If the power source has significant inductance due to long lead length, take care to prevent overshoots due to the LC tank circuit and provide protection if necessary to prevent exceeding the 30V absolute maximum rating on IN.

The MAX4838A/MAX4840A/MAX4842A provide protection against voltage faults up to 28V, but this does not include negative voltages. If negative voltages are a concern, connect a Schottky diode from IN to GND to clamp negative input voltages.

### **ESD** Test Conditions

ESD performance depends on a number of conditions. The MAX4838A/MAX4840A/MAX4842A are specified for  $\pm 15$ kV typical ESD resistance on IN when IN is bypassed to ground with a 1µF ceramic capacitor. Contact Maxim for a reliability report that documents test setup, methodology, and results.

### Human Body Model

Figure 8 shows the Human Body Model, and Figure 9 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a  $1.5 \mathrm{k}\Omega$  resistor.

### Table 1. MOSFET Suggestions

PART	CONFIGURATION/ PACKAGE	V <sub>DS</sub> MAX (V)	R <sub>ON</sub> AT 4.5V (mΩ)	MANUFACTURER
Si5902DC	Dual/1206-8	30	143	Vishay Silconix
Si1426DH	Single/SC70-6	30	115	www.vishay.com 402-563-6866
FDC6305N	Dual/SSOT-6	20	80	Fairchild Semiconductor
FDC6561AN	Dual/ SSOT-6	30	145	www.fairchildsemi.com
FDG315N	Single/SC70-6	30	160	207-775-8100

### IEC 61000-4-2

Since January 1996, all equipment manufactured and/or sold in the European community has been required to meet the stringent IEC 61000-4-2 specification. The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX4838A/MAX4840A/ MAX4842A help users design equipment that meets Level 3 of IEC 61000-4-2, without additional ESD-protection components.

The main difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2 ESD test model (Figure 10),

the ESD-withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 11 shows the current waveform for the  $\pm 8kV$  IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap test involves approaching the device with a charger probe. The Contact Discharge method connects the probe to the device before the probe is energized.

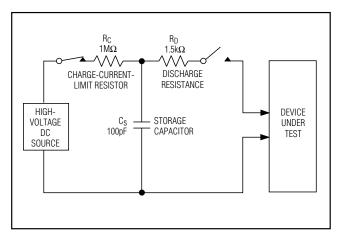


Figure 8. Human Body ESD Test Model

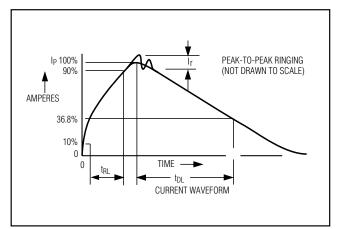


Figure 9. Human Body Model Current Waveform

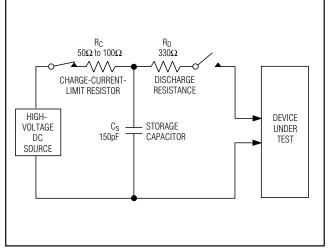


Figure 10. IEC 61000-4-2 ESD Test Model

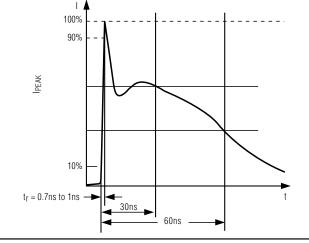
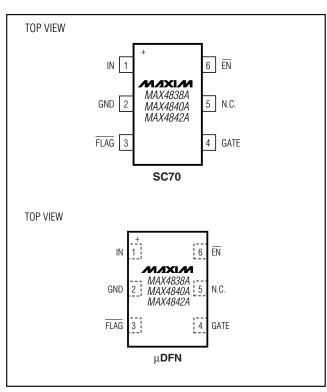


Figure 11. IEC 61000-4-2 ESD Generator Current

PROCESS: BICMOS

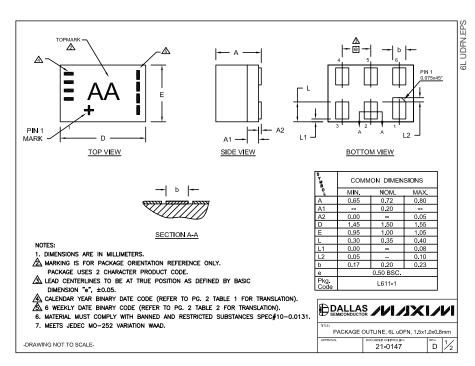


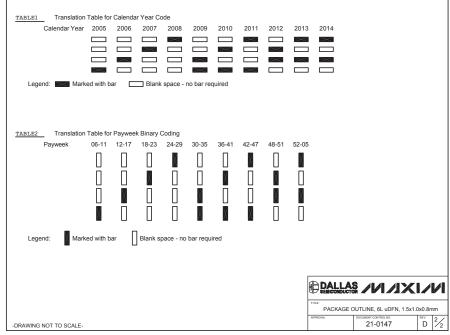
### Pin Configurations

# AX4838AMAX4838AMAX4840AMAX4840AMAX4840AMAX4840AMAX4840A

### **Package Information**

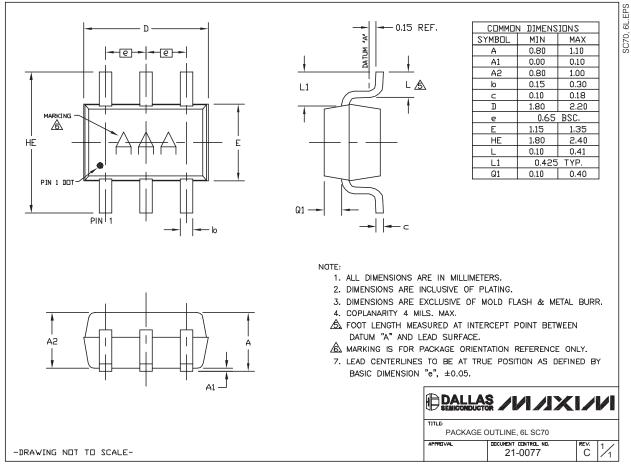
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)





### Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



MAX4838A/MAX4840A/MAX4842A

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