Introduction

This register descriptions and programming guide describes the behavior and function of the customer-programmable non-volatile-memory registers in the 5P1103 / 5P1105 programmable fanout buffers. Table 1 gives a brief overview of the 5P1103 / 5P1105 products.

Table 1. Programmable Fanout Buffer Products

Product	Description	Package
5P1103	3-Output Programmable Fanout Buffer	4 × 4 mm 24-VFQFPN (NLG24P2)
5P1105	5-Output Programmable Fanout Buffer	4 × 4 mm 24-VFQFPN (NLG24P2)

For details of operation, refer to the 5P1103 and 5P1105 product datasheets.

Programmable Fanout Buffer Register Set

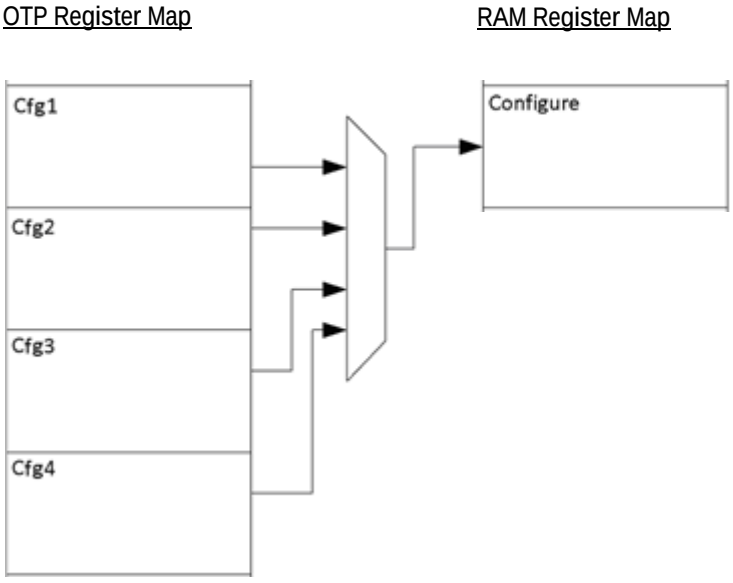
The devices contain volatile (RAM) 8-bit registers and non-volatile 8-bit registers (Figure 1). The non-volatile registers are One-Time Programmable (OTP), and bit values can only be changed from 1 (unburned state) to 0.

The OTP registers include factory trim data and four user configuration tables (Figure 1, Table 3). This document does not describe the format or methods for programming factory trim data, which is programmed by the factory before shipment.

Each configuration table contains all the information to set up the device's output frequencies. When these configuration tables are programmed into the device, the device will automatically load the RAM registers with the desired configuration on power-up. The device initializes in either I^2C mode or selection-pin mode, depending on the state of the OUT0/SELB_I2C pin on power-up, and remains in the selected mode until power is toggled (Table 2). When powered up in I^2C mode, the first configuration table, CFG0, is loaded. When powered up in selection-pin mode, the SEL0 and SEL1 inputs are decoded to select one of the four configuration tables CFG0-CFG3.

The RAM registers (Table 4) include status registers for read-back of the device's operating conditions in I^2C mode.

Figure 1. Register Maps



User Configuration Table Selection

At power-up, the voltage at OUT0_SEL_I2CB pin 24 is latched by the part and is used to select the state of SEL0/SCL pin 9 and SEL1/SDA pin 8 (Table 2).

If a weak pull-up (10kΩ) is placed on OUT0_SEL_I2CB, the SEL0/SCL and SEL1/SDA pins will be configured as hardware select inputs, SEL0 and SEL1. Connecting SEL0 and SEL1 to VDDD and/or GND selects one of 4 configuration register sets, CFG0 through CFG3, which is then loaded into the non-volatile configuration registers to configure the clock synthesizer.

If a weak pull-down is placed on OUT0_SEL_I2CB (or if it is left floating to use internal pull-down), the pins SEL0 and SEL1 will be configured as an I^2C interface's SDA and SCL slave bus. Configuration register set CFG0 is always loaded into the non-volatile configuration registers to configure the clock synthesizer. The host system can use the I^2C bus to update the non-volatile configuration registers to change the configuration and to read status registers.

Table 2. Power-up Setting of Hardware Select Pin vs I^2C Mode and Default OTP Configuration Register

OUT0_SEL_I2CB Strap at Power-up	SEL1/SDA pin	SEL0/SCL pin	Function
10kΩ pull-up	0	0	OTP bank CFG0 used to initialize RAM configuration
	0	1	OTP bank CFG1 used to initialize RAM configuration
	1	0	OTP bank CFG2 used to initialize RAM configuration
	1	1	OTP bank CFG3 used to initialize RAM configuration
10kΩ pull-down or floating	SDA	SCL	I^2C bus enabled to access registers OTP bank CFG0 used to initialize RAM configuration

I^2C Interface and Register Access

When powered-up in I^2C mode (Table 2), the device allows access to internal RAM registers (Table 4). The OTP registers (Table 3) are programmed by loading the desired values into the RAM registers that shadow the target OTP registers (Table 4), and initiating the internal programming sequence for the desired register range.

Users should not write to the trim RAM in address range 0x01–0x0F, or the Test RAM in address range 0x6A–0x6F, and should only write to the OTP Control in address range 0x70–0x7F when programming the OTP.

The RAM in address range 0x80–0x8F is not used by the device and may be used for any purpose.

Table 3. OTP Register Map Summary

Register Range	OTP Register Block Name	Register Block Description
0x000	OTP Control	OTP burned status and I^2C address setting
0x001–x00F	Factory Use	Factory settings–do not over-program
0x010–0x069	CFG0	User configuration settings bank 0
0x06A –0x0C3	CFG1	User configuration settings bank 1
0x0C4–0x11D	CFG2	User configuration settings bank 2
0x11E–0x177	CFG3	User configuration settings bank 3
0x178–0x1AF	Factory Use	Factory settings–do not over-program

Table 4. RAM Register Map Summary

Register Range	RAM Register Block Name	Corresponding OTP Register Block Name	Corresponding OTP Register Block Address Range
0x00	OTP Control	OTP Control	0x000
0x01–0x0F	Trim	Trim	0x000–0x00F
0x10–0x1F	Configuration–Main	CFG0 CFG1 CFG2 CFG3	0x010–0x069 0x06A–0x0C3 0x0C4–0x11D 0x11E–0x177
0x20–0x5F	Unused and Reserved RAM		
0x60–0x69	Configuration–Outputs		
0x6A–0x6F	Factory Use	—	—
0x70–0x7F	OTP Control	—	—
0x80–0x8F	Unused RAM	—	—
0x90–0x9F	Factory Use	—	—

Programmable Fanout Buffer–Power-Up Behavior

On power-up, the following RAM register loading sequence occurs:

1. The RAM registers always initialize to a hard-wired set of default values, which are also the “default register values” for OTP shown in subsequent tables.
2. If OTP_ burned bit D7 = 0 in the OTP Control register (Table 7), this indicates that both the trim OTP tables and at least one of the four OTP user configuration tables have been programmed.
   - Standard product is typically shipped in this condition, with factory trim performed, and with either standard or customer-specific configuration tables.
   - Trim RAM data will be updated from the trim OTP registers into the appropriate trim RAM registers, overwriting the initial default values.
   - Configuration data will be read from the one of the four OTP user configuration tables into the appropriate configuration RAM registers, overwriting the initial default values. When powered up in I^2C mode, the first configuration table, CFG0, is loaded. When powered up in selection-pin mode, the SEL0 and SEL1 input pins are decoded to select one of the four configuration tables (Table 23).
   - Initialization is now complete, and the part will operate per the configuration settings.
3. If OTP_ burned bit D7 = 1 and OTP_TRIM bit D6 = 0 in the OTP control register (Table 7), this indicates that the trim OTP tables are programmed and the four OTP user configuration tables are unconfigured.
   - Standard product can also be shipped in this condition, with factory trim performed, and ready for configuration table(s) to be customer-programmed.
   - Trim RAM data will be updated from the trim OTP registers into the appropriate trim RAM registers, overwriting the initial default values.
   - Configuration RAM data remains at the hard-wired set of default values.
   - Initialization is now complete and the part will operate per the default configuration settings.
   - When powered up in I^2C mode, the Configuration RAM registers can be written with the user's desired settings by the host system, and the clock generator operated without ever programming any of the four OTP user configuration tables. Alternatively, the host system (or a programming system) can program one of more of the four OTP user configuration tables, and also clear the OTP_ burned bit D7 in the OTP Control register (Table 7) to 0. The programmable buffer device will now follow the behavior according to sequence step 2 above for subsequent power-ups.

OTP Programming

The steps for OTP programming are given in Table 5. The procedure is to write the desired default data to the appropriate RAM registers, and then to instruct the device to burn a desired register address range into OTP.

The RAM registers have an 8-bit register address (0x00 to 0x9F), while the user OTP registers have a 9-bit address (0x000 to 0x177). This is because there are 4 banks of configuration data in OTP. The OTP addressing therefore extends across two RAM registers (Table 5). The 9-bit user start address is set by register 0x73[7:0] + 0x74[7]. The 9-bit user end address is set by register 0x75[7:0] + 0x76[7].

Table 5. OTP Programming Procedure

Step	Procedure	Notes
0	Connect all VDD pins to a single 3.3V, with OUT0_SEL_I2CB pin left floating.	Power on the part in I^2C mode.
1	Wait 100ms.	Part power-up initialization
2	Write device RAM configuration registers 0x10 to 0x69 to the desired state.	These RAM values will be programmed into OTP as new default register values.
3	Write registers 0x73 to 0x78 following the procedure in Table 5.	Set burn register source address range and destination register bank CFG0, 1, 2, or 3.
4	Write register 0x72 = 0xF0.	Reset burn bit.
5	Write register 0x72 = 0xF8.	Burn the OTP range defined above.
6	Wait 500ms.	Wait for burn to complete. Device stops acknowledging while burning.
7	Write register 0x72 = 0xF0.	Reset burn bit.
8	Write register 0x72 = 0xF8.	Repeat the burn.
9	Wait 500ms.	Wait for burn to complete. Device stops acknowledging while burning.
10	Write register 0x72 = 0xF0.	Reset burn bit.
11	Done programming.	Programming complete.
12	Write register 0x72 = 0xF2.	Perform margin read.
13	Write register 0x72 = 0xF0.	Reset margin read bit.
14	Read register 0x9F: If bit D1 = 0, programming was successful If bit D1 = 1, programming failed.	Test if OTP programming was successful.
15	Write register 0x9F = 0x00.	Reset margin read status bit.
16	One configuration register bank (CFG0, 1, 2, or 3) is now burned. To burn another bank, repeat the procedure from step 2.	Burn further configuration register banks if desired.
17	When all desired configuration register banks have been burned, write device OTP control register 0x00 with OTP_burned bit D7 clear.	Burn OTP control register clearing OTP_burned bit D7. This sets the part to load configuration data from OTP on power-up.
18	Exit.	Done.

Table 6. OTP Addressing For Programming

Register	User Start Address[8:0] Part-Select Bit 0x73	Enable Sub-block's Test Mode 0x74	User End Address[8:0] Part-Select Bit 0x75	User End Address[8:0] Part-Select Bits 0x76	Burned Register Start Address 0x77	Read Register Start Address 0x78	Registers Burned To OTP
OTP Control Register	0x00	0x4E	0x00	0x61	0x00	0x00	0x00
Configuration CFG0	0x08	0x4E	0x34	0xE1	0x10	0x10	0x10 to 0x69
Configuration CFG1	0x35	0x4E	0x61	0xE1	0x10	0x10	0x10 to 0x69
Configuration CFG2	0x62	0x4E	0x8E	0xE1	0x10	0x10	0x10 to 0x69
Configuration CFG3	0x8F	0x4E	0xBB	0xE1	0x10	0x10	0x10 to 0x69

Use the steps in the following example as guidelines to program trim and configuration 0 OTP registers:

1. Write the value from register address 0x00 to 0x69 (first bank) to RAM registers:

   Reg Address (hex): 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F 30 31 32 33 34 35 36 37 38 39 3A 3B 3C 3D 3E 3F 40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F 50 51 52 53 54 55 56 57 58 59 5A 5B 5C 5D 5E 5F 60 61 62 63 64 65 66 67 68 69

   Configuration 0: 61 FF 00 00 00 00 00 00 00 FF 01 00 00 B6 B4 92 80 0C 01 00 00 00 8C 07 00 00 00 00 85 8F BA 32 00 80 00 00 00 00 00 00 00 00 00 00 00 E0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 BB 01 5B 00 7B 00 1B 00 FF FC

   In the above example, 61 is the value in register 0x00 that corresponds to I^2C address of D4.

2. Write the following values to program the OTP with config0 and trim bits (Table 6):

   Reg Address (hex): 73 74 75 76 77 78

   Configuration 0: 08 4E 34 E1 10 10

3. Start burn with Reg 0x72 set to F8.
4. Wait 500ms.
5. Reset burn start Bit 0x72 set to F0.

Please note that this example programs the register range 0x10–0x69, skipping the 0x01–0x0F trim range and the 0x00 OTP control register. When programming OTP of the 5P1105A000 “blank” device, the 0x01–0x0F trim range is preprogrammed at the factory and should not be over written. However, register 0x00 still needs to be programmed, commonly with 61# for I^2C device address D4. You can write OTP in two burn sessions, one for the range 0x10–0x69 and one for register 0x00 only (see Table 6, row 1). You can also write OTP in one session for the whole range 0x00–0x69 but make sure to write the same values in the trim range as what is already programmed, to avoid changing the trim range. The values that should be in the 0x01–0x0F trim range of the 5P1105A000 are:

ff 00 00 00 00 00 00 00 ff 01 00 00 b6 b4 92

Set registers 0x73–0x78 to “00 4E 34 E1 00 00” for writing registers 0x00–0x69 to OTP when starting a burn process.

Default Register Values

The following tables have a column “Default Value”. These are values as they display in a 5P1103A000 or 5P1105A000; a so-called “blank” device that is meant for field programming. When the device is still unprogrammed, it runs a default mode with all outputs enabled with CMOS logic levels. The default values are the register settings for this default mode.

OTP Control Register

The I^2C slave address can be changed from the default 0xD4 to 0xD0 by programming the I2C_ADDR bit D0. Note that the I^2C address change occurs on the I^2C ACK of the write transaction. An I^2C write sequence to register 0x00 that changes the value of I2C_ADDR bit D0 should be followed by an I2C STOP condition. Further I^2C transactions to the part use the new address.

In the OTP control register (Table 7), bits can be set for the OTP burn, OTP trim status and I^2C address setting. Four bits are left unused.

Table 7. RAM0 0x00–OTP Control Register

Bits	Default Value	Name	Function
D7	1	OTP_burned	It's an active low state that indicates all the OTP burn process is done. D7 = 1 tells the chip that OTP is not burned and it will run the default mode. D7 = 0 tells the chip that OTP is burned and it will transfer OTP content to the registers for operating settings.
D6	1	OTP_TRIM	It's an active low state that indicates OTP trim part is burned.
D5	1	unused	Unused.
D4	0	unused	Unused.
D3	0	unused	Unused.
D2	0	unused	Unused.
D1	0	unused	Unused.
D0	1	Device I2C_ADDR	If I2C_ADDR = 0, then D0; if I2C_ADDR = 1, then D4.

Factory Reserved Registers for Internal Use Only

Registers from address 0x01 to 0x0F are for factory use. Do not over-program them.

Table 8. RAM0–0x01: Factory Reserved Bits–Device ID for Chip Identification

Bits	Default Value	Name	Function
D7	1	DEVICE_ID[7]	Device ID bit 7
D6	1	DEVICE_ID[6]	Device ID bit 6
D5	1	DEVICE_ID[5]	Device ID bit 5
D4	1	DEVICE_ID[4]	Device ID bit 4
D3	1	DEVICE_ID[3]	Device ID bit 3
D2	1	DEVICE_ID[2]	Device ID bit 2
D1	1	DEVICE_ID[1]	Device ID bit 1
D0	1	DEVICE_ID[0]	Device ID bit 0

Table 9. RAM0–0x02: Factory Reserved Bits–ADC Gain Setting

Bits	Default Value	Name	Function
D7	0	ADC gain[7:0]	ADC gain setting, factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 10. RAM0–0x03: Factory Reserved Bits–ADC Gain Setting

Bits	Default Value	Name	Function
D7	0	ADC gain[15:8]	ADC gain setting, factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 11. RAM0–0x04: Factory Reserved Bits–ADC Offset

Bits	Default Value	Name	Function
D7	0	ADC offset[7:0]	ADC offset, factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 12. RAM0–0x05: Factory Reserved Bits–ADC OFFSET

Bits	Default Value	Name	Function
D7	0	ADC offset[15:8]	ADC offset, factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 13. RAM0–0x06: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	TEMPY[7:0]	Factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 14. RAM0–0x07: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	OFFSET_TBIN[7:0]	Unused factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 15. RAM0–0x08: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	GAIN[7:0]	Unused factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0		
D0	0		

Table 16. RAM0–0x08: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	1	test[3:0]	Factory reserved bits
D6	1		
D5	1		
D4	1		
D3	1	NP[3:0]	Factory reserved bits
D2	1		
D1	1		
D0	1		

Table 17. RAM0–0x0A: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	Unused bit	Factory reserved bits
D6	0	Unused bit	
D5	0	Unused bit	
D4	0	Unused bit	
D3	0	Unused bit	
D2	0	Unused bit	
D1	0	Unused bit	
D0	1	Unused bit	

Table 18. RAM0–0x0B: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	bandgap_trim_up[5:0]	bandgap voltage trim, one step is 1.2mV higher than current, factory reserved bits
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	Unused bit	
D0	0	Unused bit	

Table 19. RAM0–0x0C: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	0	bandgap_trim_dn[5:0]	bandgap voltage trim, one step is 1.2mV higher than current
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	Unused bit	
D0	0	Unused bit	

Table 20. RAM0–0x0D: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	1	clk1_R_trim[2:0]	clk_R_trim: trim for “R” variation, 1LSB is 10%, default is in the middle level
D6	0		
D5	1		
D4	1	clk2_R_trim[2:0]	clk_R_trim: trim for “R” variation, 1LSB is 10%, default is in the middle level
D3	0		
D2	1		
D1	1	CLK4_amp[2]	clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level
D0	0	CLK4_amp[1]	clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level

Table 21. RAM0–0x0E: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	1	clk3_R_trim[2:0]	clk_R_trim: trim for “R” variation, 1LSB is 10%, default is in the middle level
D6	0		
D5	1		
D4	1	clk4_R_trim[2:0]	clk_R_trim: trim for “R” variation, 1LSB is 10%, default is in the middle level
D3	0		
D2	1		
D1	0	CLK4_amp[0]	clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level
D0	0	CLK3_amp[0]	clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level

Table 22. RAM0–0x0F: Factory Reserved Bits

Bits	Default Value	Name	Function
D7	1	CLK1_amp[2]	clk_amp: tune the amplitude of PAD, 1LSB is 10%, default is in the middle level, factory reserved bits
D6	0	CLK1_amp[1]	
D5	0	CLK1_amp[0]	
D4	1	CLK2_amp[2]	
D3	0	CLK2_amp[1]	
D2	0	CLK2_amp[0]	
D1	1	CLK3_amp[2]	
D0	0	CLK3_amp[1]	

Configuration Registers

The internal RAM configuration registers occupy 0x10 to 0x69 (Table 4).

The 4 OTP configuration banks CFG0, CFG1, CFG2, and CFG3 use the same register structure and setting behavior.

The tables with register details refer to the RAM register address for simplicity. Table 23 shows the 3-digit OTP register addresses 0x010 to 0x177 for the four banks of identical configuration registers, and the corresponding RAM register address.

Table 23. RAM Configuration Registers and OTP Configuration Registers CFG0, CFG1, CFG2, CFG3 Summary

Register Address					Function
RAM	CFG0	CFG1	CFG2	CFG3	
0x10	0x010	0x06A	0x0C4	0x11E	Primary source and shutdown register
0x11	0x011	0x06B	0x0C5	0x11F	Factory reserved register
0x12	0x012	0x06C	0x0C6	0x120	Crystal X1 load capacitor register
0x13	0x013	0x06D	0x0C7	0x121	Crystal X2 load capacitor register
0x14	0x014	0x06E	0x0C8	0x122	Factory reserved register

Table 23. RAM Configuration Registers and OTP Configuration Registers CFG0, CFG1, CFG2, CFG3 Summary (Cont.)

Register Address					Function
RAM	CFG0	CFG1	CFG2	CFG3	
0x15	0x015	0x06F	0x0C9	0x123	Factory reserved register
0x16	0x016	0x070	0x0CA	0x124	Factory reserved register
0x17	0x017	0x071	0x0CB	0x125	Factory reserved register
0x18	0x018	0x072	0x0CC	0x126	Factory reserved register
0x19	0x019	0x073	0x0CD	0x127	Factory reserved register
0x1A	0x01A	0x074	0x0CE	0x128	Factory reserved register
0x1B	0x01B	0x075	0x0CF	0x129	Factory reserved register
0x1C	0x01C	0x076	0x0D0	0x12A	Factory reserved register
0x1D	0x01D	0x077	0x0D1	0x12B	Factory reserved register
0x1E	0x01E	0x078	0x0D2	0x12C	Factory reserved register
0x1F	0x01F	0x079	0x0D3	0x12D	Factory reserved register
0x20	0x020	0x07A	0x0D4	0x12E	Factory reserved register
0x21	0x021	0x07B	0x0D5	0x12F	Factory reserved register
0x22	0x022	0x07C	0x0D6	0x130	Factory reserved register
0x23	0x023	0x07D	0x0D7	0x131	Factory reserved register
0x24	0x024	0x07E	0x0D8	0x132	Factory reserved register
0x25	0x025	0x07F	0x0D9	0x133	Factory reserved register
0x26	0x026	0x080	0x0DA	0x134	Factory reserved register
0x27	0x027	0x081	0x0DB	0x135	Factory reserved register
0x28	0x028	0x082	0x0DC	0x136	Factory reserved register
0x29	0x029	0x083	0x0DD	0x137	Factory reserved register
0x2A	0x02A	0x084	0x0DE	0x138	Factory reserved register
0x2B	0x02B	0x085	0x0DF	0x139	Factory reserved register
0x2C	0x02C	0x086	0x0E0	0x13A	Factory reserved register
0x2D	0x02D	0x087	0x0E1	0x13B	Factory reserved register
0x2E	0x02E	0x088	0x0E2	0x13C	Factory reserved register
0x2F	0x02F	0x089	0x0E3	0x13D	Factory reserved register
0x30	0x030	0x08A	0x0E4	0x13E	Factory reserved register
0x31	0x031	0x08B	0x0E5	0x13F	Factory reserved register
0x32	0x032	0x08C	0x0E6	0x140	Factory reserved register
0x33	0x033	0x08D	0x0E7	0x141	Factory reserved register
0x34	0x034	0x08E	0x0E8	0x142	Factory reserved register

Table 23. RAM Configuration Registers and OTP Configuration Registers CFG0, CFG1, CFG2, CFG3 Summary (Cont.)

Register Address					Function
RAM	CFG0	CFG1	CFG2	CFG3	
0x35	0x035	0x08F	0x0E9	0x143	Factory reserved register
0x36	0x036	0x090	0x0EA	0x144	Factory reserved register
0x37	0x037	0x091	0x0EB	0x145	Factory reserved register
0x38	0x038	0x092	0x0EC	0x146	Factory reserved register
0x39	0x039	0x093	0x0ED	0x147	Factory reserved register
0x3A	0x03A	0x094	0x0EE	0x148	Factory reserved register
0x3B	0x03B	0x095	0x0EF	0x149	Factory reserved register
0x3C	0x03C	0x096	0x0F0	0x14A	Factory reserved register
0x3D	0x03D	0x097	0x0F1	0x14B	Factory reserved register
0x3E	0x03E	0x098	0x0F2	0x14C	Factory reserved register
0x3F	0x03F	0x099	0x0F3	0x14D	Factory reserved register
0x40	0x040	0x09A	0x0F4	0x14E	Factory reserved register
0x41	0x041	0x09B	0x0F5	0x14F	Factory reserved register
0x42	0x042	0x09C	0x0F6	0x150	Factory reserved register
0x43	0x043	0x09D	0x0F7	0x151	Factory reserved register
0x44	0x044	0x09E	0x0F8	0x152	Factory reserved register
0x45	0x045	0x09F	0x0F9	0x153	Factory reserved register
0x46	0x046	0x0A0	0x0FA	0x154	Factory reserved register
0x47	0x047	0x0A1	0x0FB	0x155	Factory reserved register
0x48	0x048	0x0A2	0x0FC	0x156	Factory reserved register
0x49	0x049	0x0A3	0x0FD	0x157	Factory reserved register
0x4A	0x04A	0x0A4	0x0FE	0x158	Factory reserved register
0x4B	0x04B	0x0A5	0x0FF	0x159	Factory reserved register
0x4C	0x04C	0x0A6	0x100	0x15A	Factory reserved register
0x4D	0x04D	0x0A7	0x101	0x15B	Factory reserved register
0x4E	0x04E	0x0A8	0x102	0x15C	Factory reserved register
0x4F	0x04F	0x0A9	0x103	0x15D	Factory reserved register
0x50	0x050	0x0AA	0x104	0x15E	Factory reserved register
0x51	0x051	0x0AB	0x105	0x15F	Factory reserved register
0x52	0x052	0x0AC	0x106	0x160	Factory reserved register
0x53	0x053	0x0AD	0x107	0x161	Factory reserved register
0x54	0x054	0x0AE	0x108	0x162	Factory reserved register

Table 23. RAM Configuration Registers and OTP Configuration Registers CFG0, CFG1, CFG2, CFG3 Summary (Cont.)

Register Address					Function
RAM	CFG0	CFG1	CFG2	CFG3	
0x55	0x055	0x0AF	0x109	0x163	Factory reserved register
0x56	0x056	0x0B0	0x10A	0x164	Factory reserved register
0x57	0x057	0x0B1	0x10B	0x165	Factory reserved register
0x58	0x058	0x0B2	0x10C	0x166	Factory reserved register
0x59	0x059	0x0B3	0x10D	0x167	Factory reserved register
0x5A	0x05A	0x0B4	0x10E	0x168	Factory reserved register
0x5B	0x05B	0x0B5	0x10F	0x169	Factory reserved register
0x5C	0x05C	0x0B6	0x110	0x16A	Factory reserved register
0x5D	0x05D	0x0B7	0x111	0x16B	Factory reserved register
0x5E	0x05E	0x0B8	0x112	0x16C	Factory reserved register
0x5F	0x05F	0x0B9	0x113	0x16D	Factory reserved register
0x60	0x060	0x0BA	0x114	0x16E	Clock 1 output configuration
0x61	0x061	0x0BB	0x115	0x16F	Clock 1 output configuration
0x62	0x062	0x0BC	0x116	0x170	Clock 2 output configuration
0x63	0x063	0x0BD	0x117	0x171	Clock 2 output configuration
0x64	0x064	0x0BE	0x118	0x172	Clock 3 output configuration
0x65	0x065	0x0BF	0x119	0x173	Clock 3 output configuration
0x66	0x066	0x0C0	0x11A	0x174	Clock4 output configuration
0x67	0x067	0x0C1	0x11B	0x175	Clock 4 output configuration
0x68	0x068	0x0C2	0x11C	0x176	CLK_OE/Shutdown function
0x69	0x069	0x0C3	0x11D	0x177	CLK_OS/Shutdown function

Configuration Register Detail and Functionality Description

Shutdown Function

The shutdown logic offers flexible configuration of shutdown signaling and clock output enable control. The shutdown logic is summarized in Table 24

When SP bit D1 = 0 in the shutdown register 0x00 (Table 25), the SD/OE input is active low. When SP bit D1 = 1, SD/OE is active high.

SH bit D0 in the shutdown register 0x10 (Table 25) configures the SD/OE input's action as either output enable (OE) for the clock outputs (leaving the PLL running), or full part shutdown. SH bit D1 = 0 for OE function, or 1 for shutdown function.

In shutdown, the part is shut down, differential outputs are driven High/low, and the single-ended LVCMOS outputs are driven low. In output-disable, individual outputs can be selected to be either Hi-Z or driven high/low, depending on the configuration of the CLKx_OS and CLKx_OE bits shown in Table 24.

Table 24. Shutdown Truth Table

SH bit	SP bit	OSn bit	OEn bit	SD/OE	OUTn
0	x	1	0	x	Output active
x	0	1	1	0	Output active
0	1	1	1	1	Output active
1	x	1	0	0	Output active
0	0	1	1	1	Output driven High Low
x	1	1	1	0	Output driven High Low
1	x	x	x	1	Global shutdown
x	x	0	x	x	That output only depending on input bit

Note: If the SH and SD/OE bits are both high (1) and the OSn bit and OEn bits can be don't care for the output to be global shutdown. If the SH and SD/OE bits are don't care and OSn bit being 0, the output would also be 0 for CLK_OS and output of CLK_OE depends on the state of the OEn bit.

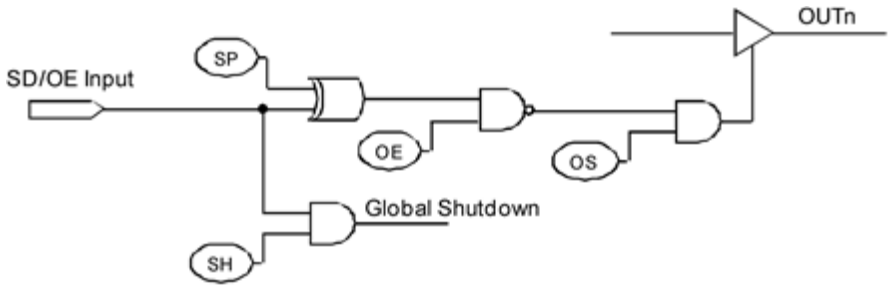
The shutdown logic diagram is shown in Figure 2, where: SD/OE is an input pin on the package.

SP is bit D1 in the shutdown register 0x10 and sets SD/OE input to be either active high or active low.

SH is bit D0 in the shutdown register 0x10 and can force software shutdown.

OE is the appropriate output enable CLK0_OE, CLK1_OE, CLK2_OE, CLK3_OE, or CLK4_OE. OS is the appropriate output select CLK0_OS, CLK1_OS, CLK2_OS, CLK3_OS, or CLK4_OS.

Figure 2. Shutdown Logic



Entering Shutdown Mode through I^2C

1. Tristate the outputs by writing b'001ss000' to registers 0x60, 0x62, 0x64, and 0x66 where ss = 00, 10, or 11 for output clock supply voltages 1.8V, 2.5V, or 3.3V.
2. Program all outputs to single-ended CMOS by writing 0x00 to registers 0x68.
3. Enable shutdown functionality by either writing 0x83 or 0x43 to register 0x10, for crystal clock source or external clock respectively.
4. Disable all output dividers by writing 0x80 to registers 0x21, 0x31, 0x41, and 0x51.
5. Take the SD/OE input pin 7 high.

Table 25. RAM1–0x10: Primary Source and Shutdown Register

Bits	Default Value	Name	Function
D7	1	en_xtal	XTAL (crystal frequency) is disabled in 0 and enabled if 1; enable crystal input.
D6	0	en_clkin	clkin which is clock input is disabled if 0 and enabled if 1.
D5	0	unused	Unused factory reserved bit.
D4	0	unused	Unused factory reserved bit.
D3	0	en_double XTAL freq_0	Unused factory reserved bit.
D2	0	en_refmode	Unused factory reserved bit.
D1	0	SP	SD/OE input pin is active low if this bit is 0 and active high if this bit is 1. (If D0 = 0 then D1 reverses SD/OE pin polarity, affecting OE bits in output polarity. If D0 = 1, SD/OE pin = 1 causes global shutdown).
D0	0	en_global shutdown	D1 reverses SD/OE pin polarity, affecting OE bits in output buffers and SD/OE input pin is shutdown (SD) if this bit is 1.

Table 26. RAM6–0x68: CLK_OE/Shutdown Function

Bits	Default Value	Name	Function
D7	1	CLK0_OE	CLK_OE checks the shutdown truth table; see *Shutdown Function* and *Shutdown Truth Table*–output enable (active high).
D6	1	CLK1_OE	CLK_OE checks the shutdown truth table; see *Shutdown Function* and *Shutdown Truth Table*–output enable (active high).
D5	1	CLK2_OE	CLK_OE checks the shutdown truth table; see *Shutdown Function* and *Shutdown Truth Table*–output enable (active high).
D4	1	CLK3_OE	CLK_OE checks the shutdown truth table; see *Shutdown Function* and *Shutdown Truth Table*–output enable (active high).
D3	1	CLK4_OE	CLK_OE checks the shutdown truth table; see *Shutdown Function* and *Shutdown Truth Table*–output enable (active high).
D2	1	clk0_slewrate[1]	Depends on slew rate (depends on Shutdown function and truth table)–set slew rate.
D1	1	clk0_pwr_sel[1:0]	Clock output drive voltage is indicated by these bits. D1 D0 = 0x indicates 1.8V D1 D0 = 10 indicates 2.5V D1 D0 = 11 indicates 3.3V–set output amplitude.
D0	1		

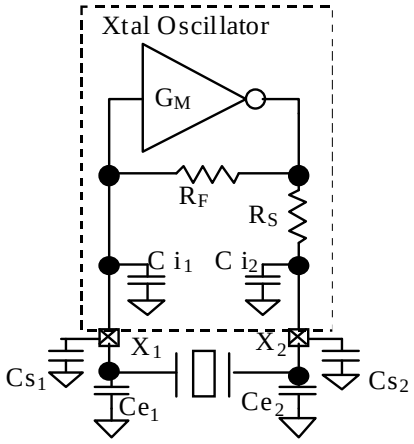
Table 27. RAM6–0x69: CLK_OS/Shutdown Function

Bits	Default Value	Name	Function
D7	1	CLK0_OS	CLK_OS checks the shutdown truth table; see *Shutdown Function* and *Shutdown Truth Table*–output suspend (active high).
D6	1	CLK1_OS	CLK_OS checks the shutdown truth table; see *Shutdown Function* and *Shutdown Truth Table*–output suspend (active high).
D5	1	CLK2_OS	CLK_OS checks the shutdown truth table; see *Shutdown Function* and *Shutdown Truth Table*–output suspend (active high).
D4	1	CLK3_OS	CLK_OS checks the shutdown truth table; see *Shutdown Function* and *Shutdown Truth Table*–output suspend (active high).
D3	1	CLK4_OS	CLK_OS checks the shutdown truth table; see *Shutdown Function* and *Shutdown Truth Table*–output suspend (active high).
D2	1	clk0_slewrate[0]	Depends on slew rate (depends on shutdown function and truth table)–set slew rate for clk0.
D1	0	otp_pwr_sel[1:0]	Set output amplitude for OTP voltage. D1 D0 = 00 indicates 3.3V D1 D0 = 01 indicates 1.8V D1 D0 = 10 indicates 2.5V D1 D0 = 11 indicates no value
D0	0		

Crystal Load Capacitor Registers

Registers 0x12 and 0x13 are crystal X1 and X2 load capacitor registers that are used to add load capacitance to X1 and X2 respectively. In X1, switch mode is provided with different mode selection options, and in X2, polarity selection of clock can be made whose values are given in the table.

Figure 3. Crystal Oscillator



Short Example of Programming the Crystal

Ci1 and Ci2 are on-chip capacitors that are programmable.

Cs is stray capacitance in the PCB and Ce is external capacitors for frequency fine tuning or for achieving load capacitance values beyond the range of the on-chip programmability.

All of these capacitors combined make the load capacitance for the crystal.

Capacitance on pin X1: Cx1 = Ci1 + Cs1 + Ce1.
Capacitance on pin X2: Cx2 = Ci2 + Cs2 + Ce2.
Total crystal load capacitance C_L = Cx1 × Cx2 / (Cx1 + Cx2).

Example: For a crystal C_L of 8pF, the registers need to be programmed with X1 = X2 = 6.92pF to get a total C_L= (6.92pF + 7.5pF + 1.5pF) / 2 = 7.9pF, which is the closest value to 8pF.

Here, Cstray = 1.5pF; package stray = 7.5pF.

The binary settings corresponding to this value will be: X1 = X2 = “10000”.

Table 28. RAM1–0x12: Crystal X1 Load Capacitor Register

Bits	Default Value	Name	Function
D7	0	xtal_load_cap_x1[5:0]	Add 6.92pF load capacitance to X1.
D6	0		Add 3.46pF load capacitance to X1.
D5	0		Add 1.73pF load capacitance to X1.
D4	0		Add 0.86pF load capacitance to X1.
D3	0		Add 0.43pF load capacitance to X1.
D2	0		Add 0.43pF load capacitance to X1.
D1	0	otp_pwr_sel[1:0]	A switch mode that indicates: D1 D0 = 00 and 01: manual D1 D0 = 10: auto and non-revertive D1 D0 = 11: auto and revertive.
D0	1		

Table 29. RAM1–0x13: Crystal X2 Load Capacitor Register and Primary Clock Source

Bits	Default Value	Name	Function
D7	0	xtal_load_cap_x2[5:0]	Add 6.92pF load capacitance to X2.
D6	0		Add 3.46pF load capacitance to X2.
D5	0		Add 1.73pF load capacitance to X2.
D4	0		Add 0.86pF load capacitance to X2.
D3	0		Add 0.43pF load capacitance to X2.
D2	0		Add 0.43pF load capacitance to X2.
D1	0	PRIMSRC	The PRIMSRC (primary source) bit inverts CLKSEL pin 6 reference clock selection and is normally set to 0 (i.e., If PRIMSRC bit is 0 while CLKSEL pin is low, then reference clock selected is XIN/REF. If PRIMSCR bit is 1 while CLKSEL pin is low, then CLKIN/CLKINB is selected). PRIMSRC: 0 for clksel to be active high and 1 to be active low. Clkok1024 is a factory reserved bit.
D0	0	clkok1024	

Clock Output Configurations Registers

In clock output configuration registers described in the tables below, the CLKx_pwr_sel bits must be configured to match the clock outputs supply voltages applied externally. The bits do not adjust the clock output signal swings. CMOSX2 provides two phase-coherent single-ended CMOS outputs while CMOSD provides 2 signals out of phase by 180 degrees. In clock output configuration registers, bits are intended specifically for disabling/enabling clock output/value and slew rate for differential outputs.

Table 30. RAM6–0x60: Clock1 Output Configuration

Bits	Default Value	Name	Function
D7	1	CLK1_cfg[2]	These bits give us the output type configuration mode. For D7, D6, D5 respectively: (D7, D6, D5) = 000: low-voltage positive/pseudo emitter-coupled logic (LVPECL). (D7, D6, D5) = 001: CMOS. (D7, D6, D5) = 010: HCSL33. (D7, D6, D5) = 011: Low Voltage Differential Signal (LVDS). (D7, D6, D5) = 100: CMOS2. (D7, D6, D5) = 101: CMOSD. (D7, D6, D5) = 110: HCSL25.
D6	0	CLK1_cfg[1]	
D5	1	CLK1_cfg[0]	
D4	1	clk1_pwr_sel[1:0]	Output Drive Voltage is set by those bits. D4 D3 = 00 sets 1.8V. D4 D3 = 10 sets 2.5V. D4 D3 = 11 sets 3.3V.
D3	1		
D2	0	Unused Bits	Factory reserved unused bits.
D1	1	CLK1_slew[1]	Enforces slew rate control for CMOS to be single-ended. D1 D0 = 00 then output slew rate is 0.8 × Normal. D1 D0 = 01 then output slew rate indicates 0.85 × Normal. D1 D0 = 10 then output slew rate indicates 0.9 × Normal. D1 D0 = 11 then output slew rate indicates 1 × Normal.
D0	1	CLK1_slew[0]	

Table 31. RAM6–0x61: Clock1 Output Configuration

Bits	Default Value	Name	Function
D7	0	CLK1_slew_diff[5:0]	Unused register bits.
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	clk1_amuxen2	This bit is used to disable the output value. Active high (1) to disable output.
D0	1	en_clkbuf1	This bit is used to enable the clock output. Active high (1) to enable the clock output.

Table 32. RAM6–0x62: Clock {Page} Output

Bits	Default Value	Name	Function
D7	0	CLK2_cfg[2]	These bits control the output type configuration mode. For D7, D6, D5 respectively: (D7, D6, D5) = 000: low-voltage positive/pseudo emitter-coupled logic (LVPECL). (D7, D6, D5) = 001: CMOS. (D7, D6, D5) = 010: HCSL33. (D7, D6, D5) = 011: Low voltage differential signal (LVDS). (D7, D6, D5) = 100: CMOS2. (D7, D6, D5) = 101: CMOSD. (D7, D6, D5) = 110: HCSL25.
D6	1	CLK2_cfg[1]	
D5	0	CLK2_cfg[0]	
D4	1	clk2_pwr_sel[1:0]	Output drive voltage is set by those bits. D4 D3 = 00 sets 1.8V. D4 D3 = 10 sets 2.5V. D4 D3 = 11 sets 3.3V.
D3	1		
D2	0	Unused Bit	Unused factory reserved bit.
D1	1	CLK2_slew[1]	Enforces slew rate control for CMOS to be single-ended. D1 D0 = 00 then output slew rate is 0.8 × Normal. D1 D0 = 01 then output slew rate indicates 0.85 × Normal. D1 D0 = 10 then output slew rate indicates 0.9 × Normal. D1 D0 = 11 then output slew rate indicates 1 × Normal.
D0	1	CLK2_slew[0]	

Table 33. RAM6–0x63: Clock2 Output Configuration

Bits	Default Value	Name	Function
D7	0	CLK2_slew_diff[5:0]	Unused register bits.
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	clk2_amuxen2	This bit is used to disable the output value. Active high (1) to disable output.
D0	0	en_clkbuf2	This bit is used to disable the output value. Active high (1) to disable output.

Table 34. RAM6–0x62: Clock {Page} Output

Bits	Default Value	Name	Function
D7	0	CLK3_cfg[2]	These bits control the output type configuration mode. For D7, D6, D5 respectively: (D7, D6, D5) = 000: low-voltage positive/pseudo emitter-coupled logic (LVPECL). (D7, D6, D5) = 001: CMOS. (D7, D6, D5) = 010: HCSL33. (D7, D6, D5) = 011: Low voltage differential signal (LVDS). (D7, D6, D5) = 100: CMOS2. (D7, D6, D5) = 101: CMOSD. (D7, D6, D5) = 110: HCSL25.
D6	1	CLK3_cfg[1]	
D5	1	CLK3_cfg[0]	
D4	1	clk3_pwr_sel[1:0]	Output drive voltage is set by those bits. D4 D3 = 00 sets 1.8V. D4 D3 = 10 sets 2.5V. D4 D3 = 11 sets 3.3V.
D3	1		
D2	0	Unused Bit	Unused factory reserved bit.
D1	1	CLK3_slew[1]	Enforces slew rate control for CMOS to be single-ended. D1 D0 = 00 then output slew rate is 0.8 × Normal. D1 D0 = 01 then output slew rate indicates 0.85 × Normal. D1 D0 = 10 then output slew rate indicates 0.9 × Normal. D1 D0 = 11 then output slew rate indicates 1 × Normal.
D0	1	CLK3_slew[0]	

Table 35. RAM6–0x65: Clock3 Output Configuration

Bits	Default Value	Name	Function
D7	0	CLK3_slew_diff[5:0]	Unused register bits.
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	clk3_amuxen2	This bit is used to disable the output value. Active high (1) to disable output.
D0	0	en_clkbuf3	This bit is used to disable the output value. Active high (1) to disable output.

Table 36. RAM6–0x66: Clock {Page} Output

Bits	Default Value	Name	Function
D7	0	CLK4_cfg[2]	These bits control the output type configuration mode. For D7, D6, D5 respectively: (D7, D6, D5) = 000: low-voltage positive/pseudo emitter-coupled logic (LVPECL). (D7, D6, D5) = 001: CMOS. (D7, D6, D5) = 010: HCSL33. (D7, D6, D5) = 011: Low voltage differential signal (LVDS). (D7, D6, D5) = 100: CMOS2. (D7, D6, D5) = 101: CMOSD. (D7, D6, D5) = 110: HCSL25.
D6	0	CLK4_cfg[1]	
D5	0	CLK4_cfg[0]	
D4	1	clk4_pwr_sel[1:0]	Output drive voltage is set by those bits. D4 D3 = 00 sets 1.8V. D4 D3 = 10 sets 2.5V. D4 D3 = 11 sets 3.3V.
D3	1		
D2	0	Unused Bit	Unused factory reserved bit.
D1	1	CLK4_slew[1]	Enforces slew rate control for CMOS to be single-ended. D1 D0 = 00 then output slew rate is 0.8 × Normal. D1 D0 = 01 then output slew rate indicates 0.85 × Normal. D1 D0 = 10 then output slew rate indicates 0.9 × Normal. D1 D0 = 11 then output slew rate indicates 1 × Normal.
D0	1	CLK4_slew[0]	

Table 37. RAM6–0x67: Clock4 Output Configuration

Bits	Default Value	Name	Function
D7	0	CLK4_slew_diff[5:0]	Unused register bits.
D6	0		
D5	0		
D4	0		
D3	0		
D2	0		
D1	0	clk4_amuxen2	This bit is used to disable the output value. Active high (1) to disable output.
D0	0	en_clkbuf4	This bit is used to disable the output value. Active high (1) to disable output.

Table 38. Unused Factory Reserved Registers

Registers	Default / Recommended Value (hex)
0x14, 0x15	00
0x16	8C
0x17	07
0x18–0x1B	00
0x1C	85
0x1D	8F
0x1E	BA
0x1F	32
0x20	00
0x21	80
0x22–0x2D	00
0x2E	E0
0x2F–0x5F	00

Revision History

Table 39. Revision History

Revision Date	Description of Change
August 11, 2017	Initial release.

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