DS2152
Enhanced T1 Single-Chip Transceiver

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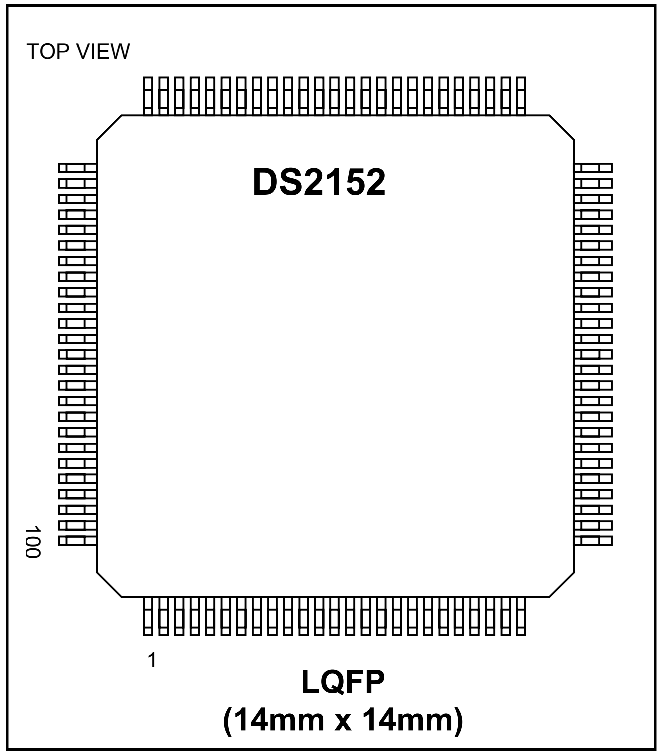
FEATURES

- Complete DS1/ISDN-PRI Transceiver Functionality
- Line Interface can Handle Both Long- and Short-Haul Trunks
- 32-Bit or 128-Bit Crystal-Less Jitter Attenuator
- Generates DSX-1 and CSU Line Build-Outs
- Frames to D4, ESF, and SLC-96[R] Formats
- Dual On-Board Two-Frame Elastic Store Slip Buffers That can Connect to Asynchronous Backplanes Up to 8.192MHz
- 8-Bit Parallel Control Port That can be Used Directly on Either Multiplexed or Nonmultiplexed Buses (Intel or Motorola)
- Extracts and Inserts Robbed-Bit Signaling
- Detects and Generates Yellow (RAI) and Blue (AIS) Alarms
- Programmable Output Clocks for Fractional T1
- Fully Independent Transmit and Receive Functionality
- Integral HDLC Controller with 16-Byte Buffers for the FDL
- Generates and Detects In-Band Loop Codes from 1 to 8 bits in Length Including CSU Loop Codes
- Contains ANSI Ones Density Monitor and Enforcer
- Large Path and Line Error Counters Including BPV, CV, CRC6, and Framing Bit Errors
- Pin Compatible with DS2154 E1 Enhanced Single-Chip Transceiver
- 5V Supply; Low-Power CMOS
- 100-Pin, $14mm^2$ LQFP Package

PIN CONFIGURATION



ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS2152L	0°C to +70°C	100 LQFP
DS2152L+	0°C to +70°C	100 LQFP
DS2152LN	-40°C to +85°C	100 LQFP
DS2152LN+	-40°C to +85°C	100 LQFP

+*Denotes lead-free/RoHS-compliant package.*

***Note:** Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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1 DETAILED DESCRIPTION

The DS2152 T1 enhanced single-chip transceiver (SCT) contains all the necessary functions for connection to T1 lines, whether they be DS-1 long haul or DSX-1 short haul. The clock recovery circuitry automatically adjusts to T1 lines from 0 feet to over 6000 feet in length. The device can generate both DSX-1 line build-outs as well as CSU line build-outs of -7.5dB, -15dB, and -22.5dB. The on-board jitter attenuator (selectable to either 32 bits or 128 bits) can be placed in either the transmit or receive data paths. The framer locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting robbed-bit signaling data and FDL data. The device contains a set of internal registers that the user can access and control the operation of the unit. Quick access via the parallel control port allows a single controller to handle many T1 lines. The device fully meets all the latest T1 specifications including ANSI T1.403-1995, ANSI T1.231-1993, AT&T TR 62411 (12-90), AT&T TR54016, and ITU G.703, G.704, G.706, G.823, and I.431.

1.1 Introduction

The DS2152 is a superset version of the popular DS2151 T1 single-chip transceiver offering the new features listed below. All of the original features of the DS2151 have been retained and software created for the original devices is transferable into the DS2152.

1.1.1 New Features

- Option for non-multiplexed bus operation
- Crystal-less jitter attenuation
- Additional hardware signaling capability including:
  - Receive signaling reinsertion to a backplane multiframe sync
  - Availability of signaling in a separate PCM data stream
  - Signaling freezing
  - Interrupt generated on change of signaling data
- Per-channel code insertion in both transmit and receive paths
- Full HDLC controller for the FDL with 16-byte buffers in both transmit and receive paths
- RCL, RLOS, RRA, and RAIS alarms now interrupt on change of state
- 8.192MHz clock synthesizer
- Per-channel loopback
- Addition of hardware pins to indicate carrier loss and signaling freeze
- Line interface function can be completely decoupled from the framer/formatter to allow:
  - Interface to optical, HDSL, and other NRZ interfaces
  - Ability to "tap" the transmit and receive bipolar data streams for monitoring purposes
  - Ability to corrupt data and insert framing errors, CRC errors, etc.
- Transmit and receive elastic stores now have independent backplane clocks
- Ability to monitor one DS0 channel in both the transmit and receive paths
- Access to the data streams in between the framer/formatter and the elastic stores
- AIS generation in the line interface that is independent of loopbacks
- Ability to calculate and check CRC6 according to the Japanese standard
- Ability to pass the F-bit position through the elastic stores in the 2.048MHz backplane mode
- Programmable in-band loop code generator and detector

1.2 Functional Description

The analog AMI/B8ZS waveform off the T1 line is transformer-coupled into the RRING and RTIP pins of the DS2152. The device recovers clock and data from the analog signal and passes it through the jitter attenuation mux to the receive side framer where the digital serial stream is analyzed to locate the framing/multi-frame pattern. The DS2152 contains an active filter that reconstructs the analog received signal for the non-linear losses that occur in transmission. The device has a usable receive sensitivity of 0dB to -36dB, which allows the device to operate on cables up to 6000 feet in length. The receive side framer locates D4 (SLC-96) or ESF multiframe boundaries as well as detects incoming alarms, including carrier loss, loss of synchronization, blue (AIS) and yellow alarms. If needed, the receive side elastic store can be enabled in order to absorb the phase and frequency differences between the recovered T1 data stream and an asynchronous backplane clock which is provided at the RSYSCLK input. The clock applied at the RSYSCLK input can be either a 2.048MHz clock or a 1.544MHz clock. The RSYSCLK can be a bursty clock with speeds up to 8.192MHz.

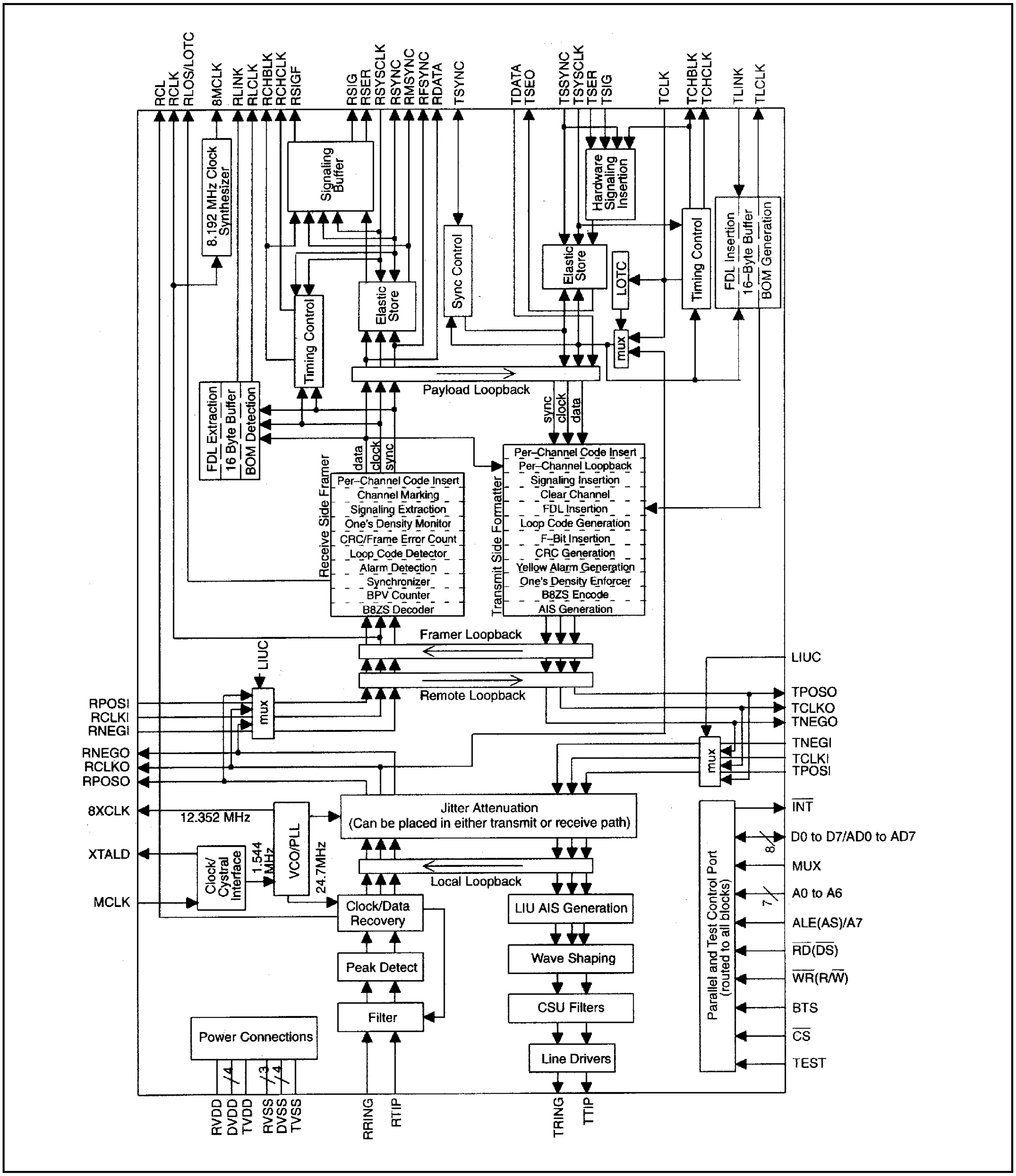
The transmit side of the DS2152 is totally independent from the receive side in both the clock requirements and characteristics. Data off of a backplane can be passed through a transmit side elastic store if necessary. The transmit formatter will provide the necessary frame/multiframe data overhead for T1 transmission. Once the data stream has been prepared for transmission, it is sent via the jitter attenuation mux to the waveshaping and line driver functions. The DS2152 will drive the T1 line from the TTIP and TRING pins via a coupling transformer. The line driver can handle both long (CSU) and short haul (DSX-1) lines.

1.3 Reader’s Note

This data sheet assumes a particular nomenclature of the T1 operating environment. In each 125µs frame, there are 24 8-bit channels plus a framing bit. It is assumed that the framing bit is sent first followed by channel 1. Each channel is made up of 8 bits that are numbered 1 to 8. Bit number 1 is the MSB and is transmitted first. Bit number 8 is the LSB and is transmitted last. Throughout this data sheet, the following abbreviations are used:

D4	Superframe (12 frames per multiframe) Multiframe Structure
SLC-96	Subscriber Loop Carrier - 96 Channels (SLC-96 is an AT&T registered trademark)
ESF	Extended Superframe (24 frames per multiframe) Multiframe Structure
B8ZS	Bipolar with 8 0 Substitution
CRC	Cyclical Redundancy Check
Ft	Terminal Framing Pattern in D4
Fs	Signaling Framing Pattern in D4
FPS	Framing Pattern in ESF
MF	Multiframe
BOC	Bit Oriented Code
HDLC	High Level Data Link Control
FDL	Facility Data Link

Figure 1-1. DS2152 Enhanced T1 Single-Chip Transceiver



2 PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	RCHBLK	O	Receive Channel Block
2, 4, 5, 7–10, 15, 23, 26, 27, 28, 36, 54, 76	N.C.	—	No Connection. These pins should be left open circuited.
3	8MCLK	O	8.192MHz Clock
6	RCL	O	Receive Carrier Loss
11	BTS	I	Bus Type Select
12	LIUC	I	Line Interface Connect
13	8XCLK	O	Eight Times Clock
14	TEST	I	Test
16	RTIP	I	Receive Analog Tip Input
17	RRING	I	Receive Analog Ring Input
18	RVDD	—	Receive Analog Positive Supply
19, 20, 24	RVSS	—	Receive Analog Signal Ground
21	MCLK	I	Master Clock Input
22	XTALD	O	Quartz Crystal Driver
25	$\overline{\text{INT}}$	O	Active-Low Interrupt
29	TTIP	O	Transmit Analog Tip Output
30	TVSS	—	Transmit Analog Signal Ground
31	TVDD	—	Transmit Analog Positive Supply
32	TRING	O	Transmit Analog Ring Output
33	TCHBLK	O	Transmit Channel Block
34	TLCLK	O	Transmit Link Clock
35	TLINK	I	Transmit Link Data
37	TSYNC	I/O	Transmit Sync
38	TPOSI	I	Transmit Positive Data Input
39	TNEGI	I	Transmit Negative Data Input
40	TCLKI	I	Transmit Clock Input
41	TCLKO	O	Transmit Clock Output
42	TNEGO	O	Transmit Negative Data Output
43	TPOSO	O	Transmit Positive Data Output
44, 61, 81, 83	DVDD	—	Digital Positive Supply
45, 60, 80, 84	DVSS	—	Digital Signal Ground
46	TCLK	I	Transmit Clock
47	TSER	I	Transmit Serial Data
48	TSIG	I	Transmit Signaling Input
49	TESO	O	Transmit Elastic Store Output
50	TDATA	I	Transmit Data
51	TSYSCLK	I	Transmit System Clock
52	TSSYNC	I	Transmit System Sync
53	TCHCLK	O	Transmit Channel Clock
55	MUX	I	Bus Operation
56	D0/AD0	I/O	Data Bus Bit 0/Address/Data Bus Bit 0

PIN	NAME	TYPE	FUNCTION
57	D1/AD1	I/O	Data Bus Bit 1/Address/Data Bus Bit 1
58	D2/AD2	I/O	Data Bus Bit 2/Address/Data Bus Bit 2
59	D3/AD3	I/O	Data Bus Bit 3/Address/Data Bus Bit 3
62	D4/AD4	I/O	Data Bus Bit 4/Address/Data Bus Bit 4
63	D5/AD5	I/O	Data Bus Bit 5/Address/Data Bus Bit 5
64	D6/AD6	I/O	Data Bus Bit 6/Address/Data Bus Bit 6
65	D7/AD7	I/O	Data Bus Bit 7/Address/Data Bus Bit 7
66–72	A0–A6	I	Address Bus Bit 0
73	A7/ALE	I	Address Bus Bit 7/Address Latch Enable
74	$\overline{RD}$($\overline{DS}$)	I	Active-Low Read Input (Data Strobe)
75	$\overline{CS}$	I	Active-Low Chip Select
77	$\overline{WR}$(R/$\overline{W}$)	I	Active-Low Write Input (Read/Write)
78	RLINK	O	Receive Link Data
79	RLKCLK	O	Receive Link Clock
82	RCLK	O	Receive Clock
85	RDATA	O	Receive Data
86	RPOSI	I	Receive Positive Data Input
87	RNEGI	I	Receive Negative Data Input
88	RCLKI	I	Receive Clock Input
89	RCLKO	O	Receive Clock Output
90	RNEGO	O	Receive Negative Data Output
91	RPOSO	O	Receive Positive Data Output
92	RCHCLK	O	Receive Channel Clock
93	RSIGF	O	Receive Signaling Freeze Output
94	RSIG	O	Receive Signaling Output
95	RSER	O	Receive Serial Data
96	RMSYNC	O	Receive Multiframe Sync
97	RFSYNC	O	Receive Frame Sync
98	RSYNC	I/O	Receive Sync
99	RLOS/LOTC	O	Receive Loss of Sync/Loss of Transmit Clock
100	RSYSCLK	I	Receive System Clock

2.1 Transmit Side Digital Pins

PIN	NAME	FUNCTION
46	TCLK	**Transmit Clock.** A 1.544MHz primary clock. Used to clock data through the transmit side formatter.
47	TSER	**Transmit Serial Data.** Transmit NRZ serial data. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.
53	TCHCLK	**Transmit Channel Clock.** A 192kHz clock that pulses high during the LSB of each channel. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for parallel to serial conversion of channel data.
33	TCHBLK	**Transmit Channel Block.** A user-programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with TCLK when the transmit side elastic store is disabled. Synchronous with TSYSCLK when the transmit side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used such as Fractional T1, 384kbps (H0), 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See Section 10 for details.
51	TSYSCLK	**Transmit System Clock.** 1.544MHz or 2.048MHz clock. Only used when the transmit side elastic store function is enabled. Should be tied low in applications that do not use the transmit side elastic store. Can be burst at rates up to 8.192MHz.
34	TLCLK	**Transmit Link Clock.** 4 kHz or 2kHz (ZBTSI) demand clock for the TLINK input. See Section 12 for details. Transmit Link Data [TLINK].
35	TLINK	**Transmit Link Data.** If enabled via TCR1.2, this pin will be sampled on the falling edge of TCLK for data insertion into either the FDL stream (ESF) or the Fs-bit position (D4) or the Z-bit position (ZBTSI). See Section 12 for details.
37	TSYNC	**Transmit Sync.** A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Via TCR2.2, the DS2152 can be programmed to output either a frame or multiframe pulse at this pin. If this pin is set to output pulses at frame boundaries, it can also be set via TCR2.4 to output double-wide pulses at signaling frames. See Section 16 for details.
52	TSSYNC	**Transmit System Sync.** Only used when the transmit side elastic store is enabled. A pulse at this pin will establish either frame or multiframe boundaries for the transmit side. Should be tied low in applications that do not use the transmit side elastic store.
48	TSIG	**Transmit Signaling Input.** When enabled, this input will sample signaling bits for insertion into outgoing PCM T1 data stream. Sampled on the falling edge of TCLK when the transmit side elastic store is disabled. Sampled on the falling edge of TSYSCLK when the transmit side elastic store is enabled.
49	TESO	**Transmit Elastic Store Data Output.** Updated on the rising edge of TCLK with data out of the transmit side elastic store whether the elastic store is enabled or not. This pin is normally tied to TDATA.
50	TDATA	**Transmit Data.** Sampled on the falling edge of TCLK with data to be clocked through the transmit side formatter. This pin is normally tied to TESO.
43	TPOSO	**Transmit Positive Data Output.** Updated on the rising edge of TCLKO with the bipolar data out of the transmit side formatter. Can be programmed to source NRZ data via the Output Data Format (CCR1.6) control bit. This pin is normally tied to TPOSI.
42	TNEGO	**Transmit Negative Data Output.** Updated on the rising edge of TCLKO with the bipolar data out of the transmit side formatter. This pin is normally tied to TNEGI.
41	TCLKO	**Transmit Clock Output.** Buffered clock that is used to clock data through the transmit side formatter (i.e., either TCLK or RCLKI). This pin is normally tied to TCLKI.
38	TPOSI	**Transmit Positive Data Input.** Sampled on the falling edge of TCLKI for data to be

PIN	NAME	FUNCTION
		transmitted out onto the T1 line. Can be internally connected to TPOSO by tying the LIUC pin high. TPOSI and TNEGI can be tied together in NRZ applications.
39	TNEGI	**Transmit Negative Data Input.** Sampled on the falling edge of TCLKI for data to be transmitted out onto the T1 line. Can be internally connected to TNEGO by tying the LIUC pin high. TPOSI and TNEGI can be tied together in NRZ applications.
40	TCLKI	**Transmit Clock Input.** Line interface transmit clock. Can be internally connected to TCLKO by tying the LIUC pin high.

2.2 Receive Side Digital Pins

PIN	NAME	FUNCTION
78	RLINK	**Receive Link Data.** Updated with either FDL data (ESF) or Fs bits (D4) or Z bits (ZBTSI) one RCLK before the start of a frame. See Section 16 for details.
79	RLCLK	**Receive Link Clock.** A 4kHz or 2 kHz (ZBTSI) clock for the RLINK output.
82	RCLK	**Receive Clock.** 1.544MHz clock that is used to clock data through the receive side framer.
92	RCHCLK	**Receive Channel Clock.** A 192kHz clock that pulses high during the LSB of each channel. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for parallel to serial conversion of channel data.
1	RCHBLK	**Receive Channel Block.** A user-programmable output that can be forced high or low during any of the 24 T1 channels. Synchronous with RCLK when the receive side elastic store is disabled. Synchronous with RSYSCLK when the receive side elastic store is enabled. Useful for blocking clocks to a serial UART or LAPD controller in applications where not all T1 channels are used, such as Fractional T1, 384kbps service, 768kbps, or ISDN-PRI. Also useful for locating individual channels in drop-and-insert applications, for external per-channel loopback, and for per-channel conditioning. See Section 10 for details.
95	RSER	**Receive Serial Data.** Received NRZ serial data. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.
98	RSYNC	**Receive Sync.** An extracted pulse, one RCLK wide, is output at this pin, which identifies either frame (RCR2.4 = 0) or multiframe (RCR2.4 = 1) boundaries. If set to output frame boundaries then via RCR2.5, RSYNC can also be set to output double-wide pulses on signaling frames. If the receive side elastic store is enabled via CCR1.2, then this pin can be enabled to be an input via RCR2.3 at which a frame or multiframe boundary pulse is applied. See Section 16 for details.
97	RFSYNC	**Receive Frame Sync.** An extracted 8kHz pulse 1 RCLK wide is output at this pin that identifies frame boundaries.
96	RMSYNC	**Receive Multiframe Sync.** Only used when the receive side elastic store is enabled. An extracted pulse, 1 RSYSCLK wide, is output at this pin, which identifies multiframe boundaries. If the receive side elastic store is disabled, then this output will output multiframe boundaries associated with RCLK.
85	RDATA	**Receive Data.** Updated on the rising edge of RCLK with the data out of the receive side framer.
100	RSYSCLK	**Receive System Clock.** 1.544MHz or 2.048MHz clock. Only used when the elastic store function is enabled. Should be tied low in applications that do not use the elastic store. Can be burst at rates up to 8.192MHz.
94	RSIG	**Receive Signaling Output.** Outputs signaling bits in a PCM format. Updated on rising edges of RCLK when the receive side elastic store is disabled. Updated on the rising edges of RSYSCLK when the receive side elastic store is enabled.

PIN	NAME	FUNCTION
99	RLOS/LOTC	**Receive Loss of Sync/Loss of Transmit Clock.** A dual function output that is controlled by the CCR3.5 control bit. This pin can be programmed to either toggle high when the synchronizer is searching for the frame and multiframe or to toggle high if the TCLK pin has not been toggled for 5µs.
6	RCL	**Receive Carrier Loss.** Set high when the line interface detects a loss of carrier.
93	RSIGF	**Receive Signaling Freeze.** Set high when the signaling data is frozen via either automatic or manual intervention. Used to alert downstream equipment of the condition.
3	8MCLK	**8MHz Clock.** A 8.192MHz output clock that is referenced to the clock that is output at the RCLK pin and is used to clock data through the receive side framer.
91	RPOSO	**Receive Positive Data Output.** Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally tied to RPOSI.
90	RNEGO	**Receive Negative Data Output.** Updated on the rising edge of RCLKO with the bipolar data out of the line interface. This pin is normally tied to RNEGI.
89	RCLKO	**Receive Clock Output.** Buffered recovered clock from the T1 line. This pin is normally tied to RCLKI.
86	RPOSI	**Receive Positive Data Input.** Sampled on the falling edge of RCLKI for data to be clocked through the receive side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RPOSO by tying the LIUC pin high.
87	RNEGI	**Receive Negative Data Input.** Sampled on the falling edge of RCLKI for data to be clocked through the receive side framer. RPOSI and RNEGI can be tied together for a NRZ interface. Can be internally connected to RNEGO by tying the LIUC pin high.
88	RCLKI	**Receive Clock Input.** Clock used to clock data through the receive side framer. This pin is normally tied to RCLKO. Can be internally connected to RCLKO by tying the LIUC pin high.

2.3 Parallel Control Port Pins

PIN	NAME	FUNCTION
25	$\overline{\text{INT}}$	**Interrupt.** Flags host controller during conditions and change of conditions defined in the Status Registers 1 and 2 and the FDL Status Register. Active-low, open-drain output.
14	TEST	**Tri-State Control.** Set high to tri-state all output and I/O pins (including the parallel control port). Set low for normal operation. Useful in board-level testing.
55	MUX	**Bus Operation.** Set low to select nonmultiplexed bus operation. Set high to select multiplexed bus operation.
56–65	D0–D7/ AD0–AD7	**Data Bus or Address/Data Bus.** In nonmultiplexed bus operation (MUX = 0), serves as the data bus. In multiplexed bus operation (MUX = 1), serves as an 8-bit multiplexed address/data bus.
66–72	A0–A6	**Address Bus.** In nonmultiplexed bus operation (MUX = 0), serves as the address bus. In multiplexed bus operation (MUX = 1), these pins are not used and should be tied low.
11	BTS	**Bus Type Select.** Strap high to select Motorola bus timing; strap low to select Intel bus timing. This pin controls the function of the $\overline{\text{RD}}$ ($\overline{\text{DS}}$), ALE(AS), and $\overline{\text{WR}}$ (R/$\overline{\text{W}}$) pins. If BTS = 1, then these pins assume the function listed in parentheses.
74	$\overline{\text{RD}}$($\overline{\text{DS}}$)	**Read Input (Data Strobe).** $\overline{\text{RD}}$ and $\overline{\text{DS}}$ are active-low signals when MUX = 1. DS is active high when MUX = 0. See bus timing diagrams.
75	$\overline{\text{CS}}$	**Chip Select.** Must be low to read or write to the device. $\overline{\text{CS}}$ is an active-low signal.
73	ALE(AS)	**A7 or Address Latch Enable (Address Strobe).** In non-multiplexed bus operation (MUX = 0), serves as the upper address bit. In multiplexed bus operation (MUX = 1), serves to demultiplex the bus on a positive-going edge.
77	$\overline{\text{WR}}$(R/$\overline{\text{W}}$)	**Write Input (Read/Write).** $\overline{\text{WR}}$ is an active-low signal.

2.4 Line Interface Pins

PIN	NAME	FUNCTION
21	MCLK	**Master Clock Input.** A 1.544MHz (±50ppm) clock source with TTL levels is applied at this pin. This clock is used internally for both clock/data recovery and for jitter attenuation. A quartz crystal of 1.544MHz may be applied across MCLK and XTALD instead of the TTL level clock source.
22	XTALD	**Quartz Crystal Driver.** A quartz crystal of 1.544MHz may be applied across MCLK and XTALD instead of a TTL level clock source at MCLK. Leave open circuited if a TTL clock source is applied at MCLK.
13	8XCLK	**Eight Times Clock**. A 12.352MHz clock that is frequency locked to the 1.544MHz clock provided from the clock/data recovery block (if the jitter attenuator is enabled on the receive side) or from the TCLKI pin (if the jitter attenuator is enabled on the transmit side). Can be internally disabled via the TEST2 register if not needed.
12	LIUC	**Line Interface Connect.** Tie low to separate the line interface circuitry from the framer/formatter circuitry and activate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/ RCLKI pins. Tie high to connect the line interface circuitry to the framer/formatter circuitry and deactivate the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins. When LIUC is tied high, the TPOSI/TNEGI/TCLKI/RPOSI/RNEGI/RCLKI pins should be tied low.
16, 17	RTIP, RRING	**Receive Tip and Ring.** Analog inputs for clock recovery circuitry. These pins connect via a 1:1 transformer to the T1 line. See Section 15 for details.
29, 32	TTIP, TRING	**Transmit Tip and Ring.** Analog line driver outputs. These pins connect via a 1:1.15 or 1:1.36 step-up transformer to the T1 line. See Section 15 for details.

2.5 Supply Pins

PIN	NAME	FUNCTION
44, 61, 81, 83	DVDD	**Digital Positive Supply.** 5.0V ±5%. Should be tied to the RVDD and TVDD pins.
18	RVDD	**Receive Analog Positive Supply.** 5.0V ±5%. Should be tied to the DVDD and TVDD pins.
31	TVDD	**Transmit Analog Positive Supply.** 5.0V ±5%. Should be tied to the RVDD and DVDD pins.
45, 60, 80, 84	DVSS	**Digital Signal Ground.** Should be tied to the RVSS and TVSS pins.
19, 20, 24	RVSS	**Receive Analog Signal Ground.** 0V. Should be tied to the DVSS and TVSS pins.
30	TVSS	**Transmit Analog Ground.** 0V. Should be tied to the RVSS and DVSS pins.

Table 2-1. Register Map

ADDRESS	R/W	REGISTER	
		DESCRIPTION	NAME
00	R/W	FDL Control	FDLC
01	R/W	FDL Status	FDLS
02	R/W	FDL Interrupt Mask	FIMR
03	R/W	Receive Performance Report Message	RPRM
04	R/W	Receive Bit Oriented Code	RBOC
05	R	Receive FDL FIFO	RFFR
06	R/W	Transmit Performance Report Message	TPRM
07	R/W	Transmit Bit Oriented Code	TBOC
08	W	Transmit FDL FIFO	TFFR
09	R/W	Test 2	TEST2 (set to 00h)
0A	R/W	Common Control 7	CCR7
0B–0E	—	Not present	—
0F	R	Deceive ID	IDR
10	R/W	Receive Information 3	RIR3
11	R/W	Common Control 4	CCR4
12	R/W	In-Band Code Control	IBCC
13	R/W	Transmit Code Definition	TCD
14	R/W	Receive Up Code Definition	RUPCD
15	R/W	Receive Down Code Definition	RDNCD
16	R/W	Transmit Channel Control 1	TCC1
17	R/W	Transmit Channel Control 2	TCC2
18	R/W	Transmit Channel Control 3	TCC3
19	R/W	Common Control 5	CCR5
1A	R	Transmit DS0 Monitor	TDS0M
1B	R/W	Receive Channel Control 1	RCC1
1C	R/W	Receive Channel Control 2	RCC2
1D	R/W	Receive Channel Control 3	RCC3
1E	R/W	Common Control 6	CCR6
1F	R	Receive DS0 Monitor	RDS0M
20	R/W	Status 1	SR1
21	R/W	Status 2	SR2
22	R/W	Receive Information 1	RIR1
23	R	Line Code Violation Count 1	LCVCR1
24	R	Line Code Violation Count 2	LCVCR2
25	R	Path Code Violation Count 1	PCVCR1
26	R	Path Code Violation Count 2	PCVCR2
27	R	Multiframe Out of Sync Count 2	MOSCR2
28	R	Receive FDL Register	RFDL
29	R/W	Receive FDL Match 1	RMTCH1
2A	R/W	Receive FDL Match 2	RMTCH2
2B	R/W	Receive Control 1	RCR1
2C	R/W	Receive Control 2	RCR2
2D	R/W	Receive Mark 1	RMR1
2E	R/W	Receive Mark 2	RMR2
2F	R/W	Receive Mark 3	RMR3
30	R/W	Common Control 3	CCR3
31	R/W	Receive Information 2	RIR2
32	R/W	Transmit Channel Blocking 1	TCBR1

ADDRESS	R/W	REGISTER	
		DESCRIPTION	NAME
33	R/W	Transmit Channel Blocking 2	TCBR2
34	R/W	Transmit Channel Blocking 3	TCBR3
35	R/W	Transmit Control 1	TCR1
36	R/W	Transmit Control 2	TCR2
37	R/W	Common Control 1	CCR1
38	R/W	Common Control 2	CCR2
39	R/W	Transmit Transparency 1	TTR1
3A	R/W	Transmit Transparency 2	TTR2
3B	R/W	Transmit Transparency 3	TTR3
3C	R/W	Transmit Idle 1	TIR1
3D	R/W	Transmit Idle 2	TIR2
3E	R/W	Transmit Idle 3	TIR3
3F	R/W	Transmit Idle Definition	TIDR
40	R/W	Transmit Channel 9	TC9
41	R/W	Transmit Channel 10	TC10
42	R/W	Transmit Channel 11	TC11
43	R/W	Transmit Channel 12	TC12
44	R/W	Transmit Channel 13	TC13
45	R/W	Transmit Channel 14	TC14
46	R/W	Transmit Channel 15	TC15
47	R/W	Transmit Channel 16	TC16
48	R/W	Transmit Channel 17	TC17
49	R/W	Transmit Channel 18	TC18
4A	R/W	Transmit Channel 19	TC19
4B	R/W	Transmit Channel 20	TC20
4C	R/W	Transmit Channel 21	TC21
4D	R/W	Transmit Channel 22	TC22
4E	R/W	Transmit Channel 23	TC23
4F	R/W	Transmit Channel 24	TC24
50	R/W	Transmit Channel 1	TC1
51	R/W	Transmit Channel 2	TC2
52	R/W	Transmit Channel 3	TC3
53	R/W	Transmit Channel 4	TC4
54	R/W	Transmit Channel 5	TC5
55	R/W	Transmit Channel 6	TC6
56	R/W	Transmit Channel 7	TC7
57	R/W	Transmit Channel 8	TC8
58	R/W	Receive Channel 1	RC17
59	R/W	Receive Channel 18	RC18
5A	R/W	Receive Channel 19	RC19
5B	R/W	Receive Channel 20	RC20
5C	R/W	Receive Channel 21	RC21
5D	R/W	Receive Channel 22	RC22
5E	R/W	Receive Channel 23	RC23
5F	R/W	Receive Channel 24	RC24
60	R	Receive Signaling 1	RS1
61	R	Receive Signaling 2	RS2
62	R	Receive Signaling 3	RS3
63	R	Receive Signaling 4	RS4
64	R	Receive Signaling 5	RS5
65	R	Receive Signaling 6	RS6

ADDRESS	R/W	REGISTER	
		DESCRIPTION	NAME
66	R	Receive Signaling 7	RS7
67	R	Receive Signaling 8	RS8
68	R	Receive Signaling 9	RS9
69	R	Receive Signaling 10	RS10
6A	R	Receive Signaling 11	RS11
6B	R	Receive Signaling 12	RS12
6C	R/W	Receive Channel Blocking 1	RCBR1
6D	R/W	Receive Channel Blocking 2	RCBR2
6E	R/W	Receive Channel Blocking 3	RCBR3
6F	R/W	Interrupt Mask 2	IMR2
70	R/W	Transmit Signaling 1	TS1
71	R/W	Transmit Signaling 2	TS2
72	R/W	Transmit Signaling 3	TS3
73	R/W	Transmit Signaling 4	TS4
74	R/W	Transmit Signaling 5	TS5
75	R/W	Transmit Signaling 6	TS6
76	R/W	Transmit Signaling 7	TS7
77	R/W	Transmit Signaling 8	TS8
78	R/W	Transmit Signaling 9	TS9
79	R/W	Transmit Signaling 10	TS10
7A	R/W	Transmit Signaling 11	TS11
7B	R/W	Transmit Signaling 12	TS12
7C	R/W	Line Interface Control	LICR
7D	R/W	Test 1	TEST1 (set to 00h)
7E	R/W	Transmit FDL Register	TFDL
7F	R/W	Interrupt Mask Register 1	IMR1
80	R/W	Receive Channel 1	RC1
81	R/W	Receive Channel 2	RC2
82	R/W	Receive Channel 3	RC3
83	R/W	Receive Channel 4	RC4
84	R/W	Receive Channel 5	RC5
85	R/W	Receive Channel 6	RC6
86	R/W	Receive Channel 7	RC7
87	R/W	Receive Channel 8	RC8
88	R/W	Receive Channel 9	RC9
89	R/W	Receive Channel 10	RC10
8A	R/W	Receive Channel 11	RC11
8B	R/W	Receive Channel 12	RC12
8C	R/W	Receive Channel 13	RC13
8D	R/W	Receive Channel 14	RC14
8E	R/W	Receive Channel 15	RC15
8F	R/W	Receive Channel 16	RC16

Note 1: *Test Registers 1 and 2 are used only by the factory; these registers must be cleared (set to all 0s) on power-up initialization to ensure proper operation.*
Note 2: *Register banks 9xh, Axh, Bxh, Cxh, Dxh, Exh, and Fxh are not accessible.*

3 PARALLEL PORT

The DS2152 is controlled via either a nonmultiplexed (MUX = 0) or a multiplexed (MUX = 1) bus by an external microcontroller or microprocessor. The DS2152 can operate with either Intel or Motorola bus timing configurations. If the BTS pin is tied low, Intel timing will be selected; if tied high, Motorola timing will be selected. All Motorola bus signals are listed in parentheses. See the timing diagrams in the AC Electrical Characteristics in Section 18 for more details.

4 CONTROL, ID, AND TEST REGISTERS

The operation of the DS2152 is configured via a set of 11 control registers. Typically, the control registers are only accessed when the system is first powered up. Once the DS2152 has been initialized, the control registers will only need to be accessed when there is a change in the system configuration. There are two Receive Control Register (RCR1 and RCR2), two Transmit Control Registers (TCR1 and TCR2), and seven Common Control Registers (CCR1 to CCR7). Each of the 11 registers is described in this section.

There is a device Identification Register (IDR) at address 0Fh. The MSB of this read-only register is fixed to a 0 indicating that the DS2152 is present. The E1 pin-for-pin compatible version of the DS2152 is the DS2154, which also has an ID register at address 0Fh. The user can read the MSB to determine which chip is present since in the DS2152 the MSB will be set to 0 and in the DS2154 it will be set to 1. The lower 4 bits of the IDR are used to display the die revision of the chip.

IDR: DEVICE IDENTIFICATION REGISTER (Address = 0F Hex)

(MSB)							(LSB)
T1E1	0	0	0	ID3	ID2	ID1	ID0

SYMBOL	POSITION	NAME AND DESCRIPTION
T1E1	IDR.7	**T1 or E1 Chip Determination Bit.** 0 = T1 chip 1 = E1 chip
ID3	IDR.3	**Chip Revision Bit 3.** MSB of a decimal code that represents the chip revision.
ID2	IDR.1	**Chip Revision Bit 2.**
ID1	IDR.2	**Chip Revision Bit 1.**
ID0	IDR.0	**Chip Revision Bit 0.** LSB of a decimal code that represents the chip revision.

The two Test Registers at addresses 09 and 7D hex are used by the factory in testing the DS2152. On power-up, the Test Registers should be set to 00 hex for the DS2152 to operate properly.

RCR1: RECEIVE CONTROL REGISTER 1 (Address = 2B Hex)

(MSB)							(LSB)
LCVCRF	ARC	OOF1	OOF2	SYNCC	SYNCT	SYNCE	RESYNC

SYMBOL	POSITION	NAME AND DESCRIPTION
LCVCRF	RCR1.7	**Line Code Violation Count Register Function Select.** 0 = do not count excessive 0s 1 = count excessive 0s
ARC	RCR1.6	**Auto Resync Criteria.** 0 = Resync on OOF or RCL event 1 = Resync on OOF only
OOF1	RCR1.5	**Out Of Frame Select 1.** 0 = 2/4 frame bits in error 1 = 2/5 frame bits in error
OOF2	RCR1.4	**Out Of Frame Select 2.** 0 = follow RCR1.5 1 = 2/6 frame bits in error
SYNCC	RCR1.3	**Sync Criteria.** **In D4 Framing Mode** 0 = search for Ft pattern, then search for Fs pattern 1 = cross couple Ft and Fs pattern **In ESF Framing Mode** 0 = search for FPS pattern only 1 = search for FPS and verify with CRC6
SYNCT	RCR1.2	**Sync Time.** 0 = qualify 10 bits 1 = qualify 24 bits
SYNCE	RCR1.1	**Sync Enable.** 0 = auto resync enabled 1 = auto resync disabled
RESYNC	RCR1.0	**Resync.** When toggled from low to high, a resynchronization of the receive side framer is initiated. Must be cleared and set again for a subsequent resync.

RCR2: RECEIVE CONTROL REGISTER 2 (Address = 2C Hex)

(MSB)							(LSB)
RCS	RZBTSI	RSDW	RSM	RSIO	RD4YM	FSBE	MOSCRF

SYMBOL	POSITION	NAME AND DESCRIPTION
RCS	RCR2.7	**Receive Code Select.** See Section 9 for more details. 0 = idle code (7F Hex) 1 = digital milliwatt code (1E/0B/0B/1E/9E/8B/8B/9E Hex)
RZBTSI	RCR2.6	**Receive Side ZBTSI Enable.** 0 = ZBTSI disabled 1 = ZBTSI enabled
RSDW	RCR2.5	**RSYNC Double-Wide.** (Note: This bit must be set to 0 when RCR2.4 = 1 or when RCR2.3 = 1.) 0 = do not pulse double-wide in signaling frames 1 = do pulse double-wide in signaling frames
RSM	RCR2.4	**RSYNC Mode Select.** (A don't care if RSYNC is programmed as an input.) 0 = frame mode (see the timing diagrams in Section 16) 1 = multiframe mode (see the timing diagrams in Section 16)
RSIO	RCR2.3	**RSYNC I/O Select.** (Note: This bit must be set to 0 when CCR1.2 = 0.) 0 = RSYNC is an output 1 = RSYNC is an input (only valid if elastic store enabled)
RD4YM	RCR2.2	**Receive Side D4 Yellow Alarm Select.** 0 = 0s in bit 2 of all channels 1 = a 1 in the S-bit position of frame 12
FSBE	RCR2.1	**PCVCR Fs-Bit Error Report Enable.** 0 = do not report bit errors in Fs-bit position; only Ft bit position 1 = report bit errors in Fs-bit position as well as Ft bit position
MOSCRF	RCR2.0	**Multiframe Out of Sync Count Register Function Select.** 0 = count errors in the framing bit position 1 = count the number of multiframes out of sync

TCR1: TRANSMIT CONTROL REGISTER 1 (Address = 35 Hex)

(MSB)							(LSB)
LOTCMC	TFPT	TCPT	TSSE	GB7S	TFDLS	TBL	TYEL

SYMBOL	POSITION	NAME AND DESCRIPTION
LOTCMC	TCR1.7	**Loss Of Transmit Clock Mux Control.** Determines whether the transmit side formatter should switch to the ever present RCLKO if the TCLK input should fail to transition (see Figure 1-1 for details). 0 = do not switch to RCLKO if TCLK stops 1 = switch to RCLKO if TCLK stops
TFPT	TCR1.6	**Transmit F-Bit Pass Through.** (See note below.) 0 = F bits sourced internally 1 = F bits sampled at TSER
TCPT	TCR1.5	**Transmit CRC Pass Through.** (See note below.) 0 = source CRC6 bits internally 1 = CRC6 bits sampled at TSER during F-bit time
TSSE	TCR1.4	**Software Signaling Insertion Enable.** (See note below.) 0 = no signaling is inserted in any channel from the TS1–TS12 registers 1 = signaling is inserted in all channels from the TS1–TS12 registers (the TTR registers can be used to block insertion on a channel-by-channel basis)
GB7S	TCR1.3	**Global Bit 7 Stuffing.** (See note below.) 0 = allow the TTR registers to determine which channels containing all 0s are to be Bit 7 stuffed 1 = force Bit 7 stuffing in all 0-byte channels regardless of how the TTR registers are programmed
TFDLS	TCR1.2	**TFDL Register Select.** (See note below.) 0 = source FDL or Fs bits from the internal TFDL register (legacy FDL support mode) 1 = source FDL or Fs bits from the internal HDLC/BOC controller or the TLINK pin
TBL	TCR1.1	**Transmit Blue Alarm.** (See note below.) 0 = transmit data normally 1 = transmit an unframed all 1s code at TPOSO and TNEGO
TYEL	TCR1.0	**Transmit Yellow Alarm.** (See note below.) 0 = do not transmit yellow alarm 1 = transmit yellow alarm

***Note:** For a description of how the bits in TCR1 affect the transmit side formatter, see Figure 16-11.*

TCR2: TRANSMIT CONTROL REGISTER 2 (Address = 36 Hex)

(MSB)							(LSB)
TEST1	TEST0	TZBTSI	TSDW	TSM	TSIO	TD4YM	TB7ZS

SYMBOL	POSITION	NAME AND DESCRIPTION
TEST1	TCR2.7	**Test Mode Bit 1 for Output Pins.** See Table 4-1.
TEST0	TCR2.6	**Test Mode Bit 0 for Output Pins.** See Table 4-1.
TZBTSI	TCR2.5	**Transmit Side ZBTSI Enable.** 0 = ZBTSI disabled 1 = ZBTSI enabled
TSDW	TCR2.4	**TSYNC Double-Wide.** (Note: this bit must be set to 0 when TCR2.3 = 1 or when TCR2.2 = 0.) 0 = do not pulse double-wide in signaling frames 1 = do pulse double-wide in signaling frames
TSM	TCR2.3	**TSYNC Mode Select.** 0 = frame mode (see the timing diagrams in Section 16) 1 = multiframe mode (see the timing diagrams in Section 16)
TSIO	TCR2.2	**TSYNC I/O Select.** 0 = TSYNC is an input 1 = TSYNC is an output
TD4YM	TCR2.1	**Transmit Side D4 Yellow Alarm Select.** 0 = 0s in bit 2 of all channels 1 = a 1 in the S-bit position of frame 12
TB7ZS	TCR2.0	**Transmit Side Bit 7 Zero Suppression Enable.** 0 = no stuffing occurs 1 = Bit 7 force to a 1 in channels with all 0s

Table 4-1. Output Pin Test Modes

TEST 1	TEST 0	EFFECT ON OUTPUT PINS
0	0	Operate normally
0	1	Force all output pins tri-state (including all I/O pins and parallel port pins)
1	0	Force all output pins low (including all I/O pins except parallel port pins)
1	1	Force all output pins high (including all I/O pins except parallel port pins)

CCR1: COMMON CONTROL REGISTER 1 (Address = 37 Hex)

(MSB)							(LSB)
TESE	ODF	RSAO	TSCLKM	RSCLKM	RESE	PLB	FLB

SYMBOL	POSITION	NAME AND DESCRIPTION
TESE	CCR1.7	**Transmit Elastic Store Enable.** 0 = elastic store is bypassed 1 = elastic store is enabled
ODF	CCR1.6	**Output Data Format.** 0 = bipolar data at TPOSO and TNEGO 1 = NRZ data at TPOSO; TNEGO = 0
RSAO	CCR1.5	**Receive Signaling All 1s.** This bit should not be enabled if hardware signaling is being utilized. See Section 8 for more details. 0 = allow robbed signaling bits to appear at RSER 1 = force all robbed signaling bits at RSER to 1
TSCLKM	CCR1.4	**TSYSCLK Mode Select.** 0 = if TSYSCLK is 1.544MHz 1 = if TSYSCLK is 2.048MHz
RSCLKM	CCR1.3	**RSYSCLK Mode Select.** 0 = if RSYSCLK is 1.544MHz 1 = if RSYSCLK is 2.048MHz
RESE	CCR1.2	**Receive Elastic Store Enable.** 0 = elastic store is bypassed 1 = elastic store is enabled
PLB	CCR1.1	**Payload Loopback.** 0 = loopback disabled 1 = loopback enabled
FLB	CCR1.0	**Framer Loopback.** 0 = loopback disabled 1 = loopback enabled

4.1 Payload Loopback

When CCR1.1 is set to 1, the DS2152 is forced into Payload Loopback (PLB). Normally, this loopback is only enabled when ESF framing is being performed but can be enabled also in D4 framing applications. In a PLB situation, the DS2152 loops the 192 bits of payload data (with BPVs corrected) from the receive section back to the transmit section. The FPS framing pattern, CRC6 calculation, and the FDL bits are not looped back, rather, they are reinserted by the DS2152. When PLB is enabled, the following occurs:

1) Data is transmitted from the TPOSO and TNEGO pins synchronous with RCLK instead of TCLK.
2) All the receive side signals continue to operate normally.
3) The TCHCLK and TCHBLK signals are forced low.
4) Data at the TSER, TDATA, and TSIG pins is ignored.
5) The TLCLK signal becomes synchronous with RCLK instead of TCLK.

4.2 Framer Loopback

When CCR1.0 is set to 1, the DS2152 enters a Framer Loopback (FLB) mode. This loopback is useful in testing and debugging applications. In FLB, the DS2152 loops data from the transmit side back to the receive side. When FLB is enabled, the following occurs:

1) An unframed all-1s code is transmitted at TPOSO and TNEGO.
2) Data at RPOSI and RNEGI is ignored.
3) All receive side signals take on timing synchronous with TCLK instead of RCLKI.

Note that it is not acceptable to have RCLK tied to TCLK during this loopback because this causes an unstable condition.

4.3 Pulse Density Enforcer

The SCT always examines both the transmit and receive data streams for violations of the following rules which are required by ANSI T1.403:

- No more than 15 consecutive 0s,
- At least N 1s in each and every time window of 8 x (N + 1) bits where N = 1 through 23,

Violations for the transmit and receive data streams are reported in the RIR2.0 and RIR2.1 bits, respectively. When the CCR3.3 is set to 1, the DS2152 forces the transmitted stream to meet this requirement no matter the content of the transmitted stream. When running B8ZS, the CCR3.3 bit should be set to 0 since B8ZS encoded data streams cannot violate the pulse density requirements.

4.4 Local Loopback

When CCR5.6 is set to 1, the DS2152 is forced into Local Loopback (LLB). In this loopback, data continues to be transmitted as normal through the transmit side of the DS2152 (unless LIAIS = 1). Data being received at RTIP and RRING is replaced with the data being transmitted. Data in this loopback passes through the jitter attenuator. See Figure 1-1 for more details. Note that it is not acceptable to have RCLKO tied to TCLKI during this loopback because this causes an unstable condition. Also, it is recommended that the jitter attenuator be placed on the transmit side during this loopback.

CCR2: COMMON CONTROL REGISTER 2 (Address = 38 Hex)

(MSB)							(LSB)
TFM	TB8ZS	TSLC96	TFDL	RFM	RB8ZS	RSLC96	RFDL

SYMBOL	POSITION	NAME AND DESCRIPTION
TFM	CCR2.7	**Transmit Frame Mode Select.** 0 = D4 framing mode 1 = ESF framing mode
TB8ZS	CCR2.6	**Transmit B8ZS Enable.** 0 = B8ZS disabled 1 = B8ZS enabled
TSLC96	CCR2.5	**Transmit SLC-96/Fs-Bit Loading Enable.** Only set this bit to a 1 in D4 framing applications. Must be set to 1 to source the Fs pattern. See Section 12 for details. 0 = SLC-96/Fs-bit loading disabled 1 = SLC-96/Fs-bit loading enabled
TFDL	CCR2.4	**Transmit FDL 0 Stuffer Enable.** Set this bit to 0 if using the internal HDLC/BOC controller instead of the legacy support for the FDL. See Section 12 for details. 0 = 0 stuffer disabled 1 = 0 stuffer enabled
RFM	CCR2.3	**Receive Frame Mode Select.** 0 = D4 framing mode 1 = ESF framing mode
RB8ZS	CCR2.2	**Receive B8ZS Enable.** 0 = B8ZS disabled 1 = B8ZS enabled
RSLC96	CCR2.1	**Receive SLC-96 Enable.** Only set this bit to a 1 in D4/SLC-96 framing applications. See Section 12 for details. 0 = SLC-96 disabled 1 = SLC-96 enabled
RFDL	CCR2.0	**Receive FDL 0 Destuffer Enable.** Set this bit to 0 if using the internal HDLC/BOC controller instead of the legacy support for the FDL. See Section 12 for details. 0 = 0 destuffer disabled 1 = 0 destuffer enabled

CCR3: COMMON CONTROL REGISTER 3 (Address = 30 Hex)

(MSB) **(LSB)**

ESMDM	ESR	RLOSF	RSMS	PDE	ECUS	TLOOP	—

SYMBOL	POSITION	NAME AND DESCRIPTION
ESMDM	CCR3.7	**Elastic Store Minimum Delay Mode.** See Section 11.3 for details. 0 = elastic stores operate at full two-frame depth 1 = elastic stores operate at 32-bit depth
ESR	CCR3.6	**Elastic Store Reset.** Setting this bit from a 0 to a 1 will force the elastic stores to a known depth. Should be toggled after RSYSCLK and TSYSCLK have been applied and are stable. Must be cleared and set again for a subsequent reset.
RLOSF	CCR3.5	**Function of the RLOS/LOTC Output.** 0 = Receive Loss of Sync (RLOS) 1 = Loss of Transmit Clock (LOTC)
RSMS	CCR3.4	**RSYNC Multiframe Skip Control.** Useful in framing format conversions from D4 to ESF. This function is not available when the receive side elastic store is enabled. 0 = RSYNC will output a pulse at every multiframe 1 = RSYNC will output a pulse at every other multiframe Note: for this bit to have any affect, the RSYNC must be set to output multiframe pulses (RCR2.4 = 1 and RCR2.3 = 0).
PDE	CCR3.3	**Pulse Density Enforcer Enable.** 0 = disable transmit pulse density enforcer 1 = enable transmit pulse density enforcer
ECUS	CCR3.2	**Error Counter Update Select.** See Section 6 for details. 0 = update error counters once a second 1 = update error counters every 42ms (333 frames)
TLOOP	CCR3.1	**Transmit Loop Code Enable.** See Section 13 for details. 0 = transmit data normally 1 = replace normal transmitted data with repeating code as defined in TCD register
—	CCR3.0	**Not Assigned.** Must be set to 0 when written.

CCR4: COMMON CONTROL REGISTER 4 (Address = 11 Hex)

(MSB)							(LSB)
RSRE	RPCSI	RFSA1	RFE	RFF	THSE	TPCSI	TIRFS

SYMBOL	POSITION	NAME AND DESCRIPTION
RSRE	CCR4.7	**Receive Side Signaling Reinsertion Enable.** See Section 8.2 for details. 0 = do not re-insert signaling bits into the data stream presented at the RSER pin 1 = re-insert the signaling bits into data stream presented at the RSER pin
RPCSI	CCR4.6	**Receive Per-Channel Signaling Insert.** See Section 8.2 for more details. 0 = do not use RCHBLK to determine which channels should have signaling re-inserted 1 = use RCHBLK to determine which channels should have signaling re-inserted
RFSA1	CCR4.5	**Receive Force Signaling All 1s.** See Section 8.2 for more details. 0 = do not force extracted robbed-bit signaling bit positions to a 1 1 = force extracted robbed-bit signaling bit positions to a 1
RFE	CCR4.4	**Receive Freeze Enable.** See Section 8.2 for details. 0 = no freezing of receive signaling data will occur 1 = allow freezing of receive signaling data at RSIG (and RSER if CCR4.7 = 1).
RFF	CCR4.3	**Receive Force Freeze.** Freezes receive side signaling at RSIG (and RSER if CCR4.7 = 1); will override Receive Freeze Enable (RFE). See Section 8.2 for details. 0 = do not force a freeze event 1 = force a freeze event
THSE	CCR4.2	**Transmit Hardware Signaling Insertion Enable.** See Section 8.2 for details. 0 = do not insert signaling from the TSIG pin into the data stream presented at the TSER pin 1 = insert the signaling from the TSIG pin into data stream presented at the TSER pin
TPCSI	CCR4.1	**Transmit Per-Channel Signaling Insert.** See Section 8.2 for details. 0 = do not use TCHBLK to determine which channels should have signaling inserted from TSIG 1 = use TCHBLK to determine which channels should have signaling inserted from TSIG
TIRFS	CCR4.0	**Transmit Idle Registers (TIR) Function Select.** See Section 9 for timing details. 0 = TIRs define in which channels to insert idle code 1 = TIRs define in which channels to insert data from RSER (i.e., Per-Channel Loopback function)

CCR5: COMMON CONTROL REGISTER 5 (Address = 19 Hex)

(MSB)							(LSB)
TJC	LLB	LIAIS	TCM4	TCM3	TCM2	TCM1	TCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
TJC	CCR5.7	**Transmit Japanese CRC6 Enable.** 0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation) 1 = use Japanese standard JT-G704 CRC6 calculation
LLB	CCR5.6	**Local Loopback.** 0 = loopback disabled 1 = loopback enabled
LIAIS	CCR5.5	**Line Interface AIS Generation Enable.** See Figure 1-1 for details. 0 = allow normal data from TPOSI/TNEGI to be transmitted at TTIP and TRING 1 = force unframed all 1s to be transmitted at TTIP and TRING
TCM4	CCR5.4	**Transmit Channel Monitor Bit 4.** MSB of a channel decode that determines which transmit channel data will appear in the TDS0M register. See Section 7 for details.
TCM3	CCR5.3	**Transmit Channel Monitor Bit 3.**
TCM2	CCR5.2	**Transmit Channel Monitor Bit 2.**
TCM1	CCR5.1	**Transmit Channel Monitor Bit 1.**
TCM0	CCR5.0	**Transmit Channel Monitor Bit 0.** LSB of the channel decode.

CCR6: COMMON CONTROL REGISTER 6 (Address = 1E Hex)

(MSB)							(LSB)
RJC	—	—	RCM4	RCM3	RCM2	RCM1	RCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
RJC	CCR6.7	**Receive Japanese CRC6 Enable.** 0 = use ANSI/AT&T/ITU CRC6 calculation (normal operation) 1 = use Japanese standard JT-G704 CRC6 calculation
—	CCR6.6	**Not Assigned.** Should be set to 0 when written.
—	CCR6.5	**Not Assigned.** Should be set to 0 when written.
RCM4	CCR6.4	**Receive Channel Monitor Bit 4.** MSB of a channel decode that determines which receive channel data will appear in the RDS0M register. See Section 7 for details.
RCM3	CCR6.3	**Receive Channel Monitor Bit 3.**
RCM2	CCR6.2	**Receive Channel Monitor Bit 2.**
RCM1	CCR6.1	**Receive Channel Monitor Bit 1.**
RCM0	CCR6.0	**Receive Channel Monitor Bit 0.** LSB of the channel decode.

CCR7: COMMON CONTROL REGISTER 7 (Address = 0A Hex)

(MSB)							(LSB)
LIRST	RLB	—	—	—	—	—	—

SYMBOL	POSITION	NAME AND DESCRIPTION
LIRST	CCR7.7	**Line Interface reset.** Setting this bit from a 0 to a 1 will initiate an internal reset that affects the clock recovery state machine and jitter attenuator. Normally this bit is only toggled on power-up. Must be cleared and set again for a subsequent reset.
RLB	CCR7.6	**Remote Loopback.** 0 = loopback disabled 1 = loopback enabled
—	CCR7.5 to CCR7.0	**Not Assigned.** Should be set to 0 when written to.

4.5 Power-Up Sequence

On power-up, after the supplies are stable, the DS2152 should be configured for operation by writing to all the internal registers (this includes setting the Test Registers to 00 hex) since the contents of the internal registers cannot be predicted on power-up. Finally, after the TSYSCLK and RSYSCLK inputs are stable, the ESR bit should be toggled from 0 to 1 (this step can be skipped if the elastic stores are disabled).

4.6 Remote Loopback

When CCR7.6 is set to 1, the DS2152 is forced into Remote Loopback (RLB). In this loopback, data input via the RPOSI and RNEGI pins is transmitted back to the TPOSO and TNEGO pins. Data continues to pass through the receive side framer of the DS2152 as it would normally, and the data from the transmit side formatter is ignored. See Figure 1-1 for more details.

5 STATUS AND INFORMATION REGISTERS

There is a set of nine registers that contain information on the current real-time status of the DS2152: Status Register 1 (SR1), Status Register 2 (SR2), Receive Information Registers 1 to 3 (RIR1/RIR2/RIR3), and a set of four registers for the on-board HDLC and BOC controller for the FDL. The specific details on the four registers pertaining to the FDL are covered in Section 12.1, but they operate the same as the other status registers in the DS2152, described below.

When a particular event has occurred (or is occurring), the appropriate bit in one of these nine registers is set to 1. All the bits in SR1, SR2, RIR1, RIR2, and RIR3 registers operate in a latched fashion. This means that if an event or an alarm occurs and a bit is set to 1 in any of the registers, it remains set until the user reads that bit. The bit is cleared when it is read and it is not set again until the event has occurred again (or in the case of the RBL, RYEL, LRCL, and RLOS alarms, the bit remains set if the alarm is still present). The bits in the four FDL status registers that are not latched are listed in Section 12.1.

The user will always precede a read of any of the nine registers with a write. The byte written to the register will inform the DS2152 which bits the user wishes to read and have cleared. The user will write a byte to one of these registers, with a 1 in the bit positions he or she wishes to read and a 0 in the bit positions he or she does not wish to obtain the latest information on. When a 1 is written to a bit location, the read register will be updated with the latest information. When a 0 is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically ANDed with the mask byte that was just written, and this value should be written back into the same register to ensure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write-read-write scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2152 with higher-order software languages.

The SR1, SR2, and FDLS registers have the unique ability to initiate a hardware interrupt via the $\overline{\text{INT}}$ output pin. Each of the alarms and events in the SR1, SR2, and FDLS can be either masked or unmasked from the interrupt pin via the Interrupt Mask Register 1 (IMR1), Interrupt Mask Register 2 (IMR2), and FDL Interrupt Mask Register (FIMR) respectively. The FIMR register is covered in Section 12.1.

The interrupts caused by alarms in SR1 (namely RYEL, LRCL, RBL, and RLOS) act differently than the interrupts caused by events in SR1 and SR2 (namely LUP, LDN, LOTC, RSLIP, RMF, TMF, SEC, RFDL, TFDL, RMTCH, RAF, and RSC) and FIMR. The alarm caused interrupts will force the $\overline{\text{INT}}$ pin low whenever the alarm changes state (i.e., the alarm goes active or inactive according to the set/clear criteria in Table 5-2). The $\overline{\text{INT}}$ pin will be allowed to return high (if no other interrupts are present) when the user reads the alarm bit that caused the interrupt to occur even if the alarm is still present.

The event caused interrupts will force the $\overline{\text{INT}}$ pin low when the event occurs. The $\overline{\text{INT}}$ pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

RIR1: RECEIVE INFORMATION REGISTER 1 (Address = 22 Hex)

(MSB)							(LSB)
COFA	8ZD	16ZD	RESF	RESE	SEFE	B8ZS	FBE

SYMBOL	POSITION	NAME AND DESCRIPTION
COFA	RIR1.7	**Change of Frame Alignment.** Set when the last resync resulted in a change of frame or multiframe alignment.
8ZD	RIR1.6	**Eight-0 Detect.** Set when a string of at least eight consecutive 0s (regardless of the length of the string) have been received at RPOSI and RNEGI.
16ZD	RIR1.5	**16-Zero Detect.** Set when a string of at least 16 consecutive 0s (regardless of the length of the string) have been received at RPOSI and RNEGI.
RESF	RIR1.4	**Receive Elastic Store Full.** Set when the receive elastic store buffer fills and a frame is deleted.
RESE	RIR1.3	**Receive Elastic Store Empty.** Set when the receive elastic store buffer empties and a frame is repeated.
SEFE	RIR1.2	**Severely Errored Framing Event.** Set when 2 out of 6 framing bits (Ft or FPS) are received in error.
B8ZS	RIR1.1	**B8ZS Codeword Detect.** Set when a B8ZS codeword is detected at RPOS and RNEG independent of whether the B8ZS mode is selected or not via CCR2.6. Useful for automatically setting the line coding.
FBE	RIR1.0	**Frame Bit Error.** Set when a Ft (D4) or FPS (ESF) framing bit is received in error.

RIR2: RECEIVE INFORMATION REGISTER 2 (Address = 31 Hex)

(MSB)							(LSB)
RLOSC	LRCLC	TESF	TESE	TSLIP	RBLC	RPDV	TPDV

SYMBOL	POSITION	NAME AND DESCRIPTION
RLOSC	RIR2.7	**Receive Loss of Sync Clear.** Set when the framer achieves synchronization; will remain set until read.
LRCLC	RIR2.6	**Line Interface Receive Carrier Loss Clear.** Set when the carrier signal is restored; will remain set until read. See Table 5-2.
TESF	RIR2.5	**Transmit Elastic Store Full.** Set when the transmit elastic store buffer fills and a frame is deleted.
TESE	RIR2.4	**Transmit Elastic Store Empty.** Set when the transmit elastic store buffer empties and a frame is repeated.
TSLIP	RIR2.3	**Transmit Elastic Store Slip Occurrence.** Set when the transmit elastic store has either repeated or deleted a frame.
RBLC	RIR2.2	**Receive Blue Alarm Clear.** Set when the Blue Alarm (AIS) is no longer detected; will remain set until read. See Table 5-2.
RPDV	RIR2.1	**Receive Pulse Density Violation.** Set when the receive data stream does not meet the ANSI T1.403 requirements for pulse density.
TPDV	RIR2.0	**Transmit Pulse Density Violation.** Set when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density.

RIR3: RECEIVE INFORMATION REGISTER 3 (Address = 10 Hex)

(MSB)							(LSB)
RL1	RL0	JALT	LORC	FRCL	—	—	—

SYMBOL	POSITION	NAME AND DESCRIPTION
RL1	RIR3.7	**Receive Level Bit 1.** See Table 5-1.
RL0	RIR3.6	**Receive Level Bit 0.** See Table 5-1.
JALT	RIR3.5	**Jitter Attenuator Limit Trip.** Set when the jitter attenuator FIFO reaches to within 4 bits of its limit; useful for debugging jitter attenuation operation.
LORC	RIR3.4	**Loss of Receive Clock.** Set when the RCLKI pin has not transitioned for at least 2µs (3µs ±1µs).
FRCL	RIR3.3	**Framer Receive Carrier Loss.** Set when 192 consecutive 0s have been received at the RPOSI and RNEGI pins; allowed to be cleared when 14 or more 1s out of 112 possible bit positions are received.
—	RIR3.2, RIR3.1, RIR3.0	**Not Assigned.** Could be any value when read.

Table 5-1. Receive T1 Level Indication

RL1	RL0	TYPICAL LEVEL RECEIVED (dB)
0	0	+2 to -7.5
0	1	-7.5 to -15
1	0	-15 to -22.5
1	1	less than -22.5

SR1: STATUS REGISTER 1 (Address = 20 Hex)

(MSB)							(LSB)
LUP	LDN	LOTC	RSLIP	RBL	RYEL	LRCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
LUP	SR1.7	**Loop Up Code Detected.** Set when the loop up code as defined in the RUPCD register is being received. See Section 13 for details.
LDN	SR1.6	**Loop Down Code Detected.** Set when the loop down code as defined in the RDNCD register is being received. See Section 13 for details.
LOTC	SR1.5	**Loss of Transmit Clock.** Set when the TCLK pin has not transitioned for one channel time (or 5.2µs). Will force the RLOS/LOTC pin high if enabled via CCR1.6. Also will force transmit side formatter to switch to RCLKO if so enabled via TCR1.7.
RSLIP	SR1.4	**Receive Elastic Store Slip Occurrence.** Set when the receive elastic store has either repeated or deleted a frame.
RBL	SR1.3	**Receive Blue Alarm.** Set when an unframed all 1s code is received at RPOSI and RNEGI.
RYEL	SR1.2	**Receive Yellow Alarm.** Set when a yellow alarm is received at RPOSI and RNEGI.
LRCL	SR1.1	**Line Interface Receive Carrier Loss.** Set when 192 consecutive 0s have been detected at RTIP and RRING. See Table 5-2.
RLOS	SR1.0	**Receive Loss of Sync.** Set when the device is not synchronized to the receive T1 stream.

Table 5-2. Alarm Criteria

ALARM	SET CRITERIA	CLEAR CRITERIA
Blue Alarm (AIS) (See note 1 below)	When over a 3ms window, five or less 0s are received	When over a 3ms window, six or more 0s are received
Yellow Alarm (RAI) 1. D4 bit 2 mode(RCR2.2 = 0) 2. D4 12th F-bit mode (RCR2.2=1; this mode is also referred to as the "Japanese Yellow Alarm" 3. ESF mode	When bit 2 of 256 consecutive channels is set to 0 for at least 254 occurrences When the 12th framing bit is set to 1 for two consecutive occurrences When 16 consecutive patterns of 00FF appear in the FDL	When bit 2 of 256 consecutive channels is set to 0 for less than 254 occurrences When the 12th framing bit is set to 0 for two consecutive occurrences When 14 or less patterns of 00FF hex out of 16 possible appear in the FDL
Red Alarm (LRCL) (This alarm is also referred to as Loss Of Signal)	When 192 consecutive 0s are received	When 14 or more 1s out of 112 possible bit positions are received starting with the first one received

Note 1: *The definition of Blue Alarm (or Alarm Indication Signal) is an unframed all 1s signal. Blue alarm detectors should be able to operate properly in the presence of a 10-3 error rate and they should not falsely trigger on a framed all 1s signal. The blue alarm criteria in the DS2152 have been set to achieve this performance. It is recommended that the RBL bit be qualified with the RLOS bit.*
Note 2: *ANSI specifications use a different nomenclature than the DS2152 does; the following terms are equivalent:*

RBL = AIS
LRCL = LOS
RLOS = LOF
RYEL = RAI

SR2: STATUS REGISTER 2 (Address = 21 Hex)

(MSB)							(LSB)
RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	RSC

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	SR2.7	**Receive Multiframe.** Set on receive multiframe boundaries.
TMF	SR2.6	**Transmit Multiframe.** Set on transmit multiframe boundaries.
SEC	SR2.5	**1-Second Timer.** Set on increments of 1 second based on RCLK; will be set in increments of 999ms, 999ms, and 1002ms every 3 seconds.
RFDL	SR2.4	**Receive FDL Buffer Full.** Set when the receive FDL buffer (RFDL) fills to capacity (8 bits).
TFDL	SR2.3	**Transmit FDL Buffer Empty.** Set when the transmit FDL buffer (TFDL) empties.
RMTCH	SR2.2	**Receive FDL Match Occurrence.** Set when the RFDL matches either RFDLM1 or RFDLM2.
RAF	SR2.1	**Receive FDL Abort.** Set when eight consecutive 1s are received in the FDL.
RSC	SR2.0	**Receive Signaling Change.** Set when the DS2152 detects a change of state in any of the robbed-bit signaling bits.

IMR1: INTERRUPT MASK REGISTER 1 (Address = 7F Hex)

(MSB)							(LSB)
LUP	LDN	LOTC	SLIP	RBL	RYEL	LRCL	RLOS

SYMBOL	POSITION	NAME AND DESCRIPTION
LUP	IMR1.7	**Loop Up Code Detected.** 0 = interrupt masked 1 = interrupt enabled
LDN	IMR1.6	**Loop Down Code Detected.** 0 = interrupt masked 1 = interrupt enabled
LOTC	IMR1.5	**Loss of Transmit Clock.** 0 = interrupt masked 1 = interrupt enabled
SLIP	IMR1.4	**Elastic Store Slip Occurrence.** 0 = interrupt masked 1 = interrupt enabled
RBL	IMR1.3	**Receive Blue Alarm.** 0 = interrupt masked 1 = interrupt enabled
RYEL	IMR1.2	**Receive Yellow Alarm.** 0 = interrupt masked 1 = interrupt enabled
LRCL	IMR1.1	**Line Interface Receive Carrier Loss.** 0 = interrupt masked 1 = interrupt enabled
RLOS	IMR1.0	**Receive Loss of Sync.** 0 = interrupt masked 1 = interrupt enabled

IMR2: INTERRUPT MASK REGISTER 2 (Address = 6F Hex)

(MSB) **(LSB)**

RMF	TMF	SEC	RFDL	TFDL	RMTCH	RAF	RSC

SYMBOL	POSITION	NAME AND DESCRIPTION
RMF	IMR2.7	**Receive Multiframe.** 0 = interrupt masked 1 = interrupt enabled
TMF	IMR2.6	**Transmit Multiframe.** 0 = interrupt masked 1 = interrupt enabled
SEC	IMR2.5	**1-Second Timer.** 0 = interrupt masked 1 = interrupt enabled
RFDL	IMR2.4	**Receive FDL Buffer Full.** 0 = interrupt masked 1 = interrupt enabled
TFDL	IMR2.3	**Transmit FDL Buffer Empty.** 0 = interrupt masked 1 = interrupt enabled
RMTCH	IMR2.2	**Receive FDL Match Occurrence.** 0 = interrupt masked 1 = interrupt enabled
RAF	IMR2.1	**Receive FDL Abort.** 0 = interrupt masked 1 = interrupt enabled
RSC	IMR2.0	**Receive Signaling Change.** 0 = interrupt masked 1 = interrupt enabled

6 ERROR COUNT REGISTERS

There are a set of three counters in the DS2152 that record bipolar violations, excessive 0s, errors in the CRC6 codewords, framing bit errors, and number of multiframes that the device is out of receive synchronization. Each of these three counters is automatically updated on either 1-second boundaries (CCR3.2 = 0) or every 42ms (CCR3.2 = 1) as determined by the timer in Status Register 2 (SR2.5). Hence, these registers contain performance data from either the previous second or the previous 42ms. The user can use the interrupt from the 1-second timer to determine when to read these registers. The user has a full second (or 42ms) to read the counters before the data is lost. All three counters will saturate at their respective maximum counts and they will not rollover (note: only the Line Code Violation Count Register has the potential to overflow but the bit error would have to exceed 10^{-2} before this would occur).

6.1 Line Code Violation Count Register (LCVCR)

Line Code Violation Count Register 1 High (LCVCR1) is the most significant word and LCVCR2 is the least significant word of a 16-bit counter that records code violations (CVs). CVs are defined as Bipolar Violations (BPVs) or excessive 0s. See Table 6-1 for details of exactly what the LCVCRs count. If the B8ZS mode is set for the receive side via CCR2.2, then B8ZS codewords are not counted. This counter is always enabled; it is not disabled during receive loss of synchronization (RLOS = 1) conditions.

LCVCR1: LINE CODE VIOLATION COUNT REGISTER 1 (Address = 23 Hex)
LCVCR2: LINE CODE VIOLATION COUNT REGISTER 2 (Address = 24 Hex)

(MSB)							(LSB)	
LCV15	LCV14	LCV13	LCV12	LCV11	LCV10	LCV9	LCV8	LCVCR1
LCV7	LCV6	LCV5	LCV4	LCV3	LCV2	LCV1	LCV0	LCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
LCV15	LCVCR1.7	**MSB of the 16-bit code violation count.**
LCV0	LCVCR2.0	**LSB of the 16-bit code violation count.**

Table 6-1. Line Code Violation Counting Arrangements

COUNT EXCESSIVE 0S? (RCR1.7)	B8ZS ENABLED? (CCR2.2)	WHAT IS COUNTED IN THE LCVCRs
No	No	BPVs
Yes	No	BPVs + 16 consecutive 0s
No	Yes	BPVs (B8ZS codewords not counted)
Yes	Yes	BPVs + 8 consecutive 0s

6.2 Path Code Violation Count Register (PCVCR)

When the receive side of the DS2152 is set to operate in the ESF framing mode (CCR2.3 = 1), PCVCR will automatically be set as a 12-bit counter that will record errors in the CRC6 codewords. When set to operate in the D4 framing mode (CCR2.3 = 0), PCVCR will automatically count errors in the Ft framing bit position. Via the RCR2.1 bit, the DS2152 can be programmed to also report errors in the Fs framing bit position. The PCVCR will be disabled during receive loss of synchronization (RLOS=1) conditions. See Table 6-2 for a detailed description of exactly what errors the PCVCR counts.

PCVCR1: PATH VIOLATION COUNT REGISTER 1 (Address = 25 Hex)
PCVCR2: PATH VIOLATION COUNT REGISTER 2 (Address = 26 Hex)

(MSB) **(LSB)**

(Note 1)	(Note 1)	(Note 1)	(Note 1)	CRC/FB11	CRC/FB10	CRC/FB9	CRC/FB8	PCVCR1
CRC/FB7	CRC/FB6	CRC/FB5	CRC/FB4	CRC/FB3	CRC/FB2	CRC/FB1	CRC/FB0	PCVCR2

SYMBOL	POSITION	NAME AND DESCRIPTION
CRC/FB11	PCVCR1.3	**MSB of the 12-Bit CRC6 Error or Frame Bit Error Count** (Note 2)
CRC/FB0	PCVCR2.0	**LSB of the 12-Bit CRC6 Error or Frame Bit Error Count** (Note 2)

Note 1: *The upper nibble of the counter at address 25 is used by the Multiframes Out of Sync Count Register.*

Note 2: *PCVCR counts either errors in CRC codewords (in the ESF framing mode; CCR2.3 = 1) or errors in the framing bit position (in the D4 framing mode; CCR2.3 = 0).*

Table 6-2. Path Code Violation Counting Arrangements

FRAMING MODE (CCR2.3)	COUNT Fs ERRORS? (RCR2.1)	WHAT IS COUNTED IN THE PCVCRs
D4	No	Errors in the Ft pattern
D4	Yes	Errors in both the Ft and Fs patterns
ESF	Don't Care	Errors in the CRC6 codewords

6.3 Multiframes Out of Sync Count Register (MOSCR)

Normally, the MOSCR is used to count the number of multiframes that the receive synchronizer is out of sync (RCR2.0 = 1). This number is useful in ESF applications needing to measure the parameters Loss Of Frame Count (LOFC) and ESF Error Events as described in AT&T publication TR54016. When the MOSCR is operated in this mode, it is not disabled during receive loss of synchronization (RLOS = 1) conditions. The MOSCR has alternate operating mode whereby it will count either errors in the Ft framing pattern (in the D4 mode) or errors in the FPS framing pattern (in the ESF mode). When the MOSCR is operated in this mode, it is disabled during receive loss of synchronization (RLOS = 1) conditions. See Table 6-3 for a detailed description of what the MOSCR is capable of counting.

MOSCR1: MULTIFRAMES OUT OF SYNC COUNT REGISTER 1 (Address = 25 Hex)
MOSCR2: MULTIFRAMES OUT OF SYNC COUNT REGISTER 2 (Address = 27 Hex)

(MSB) **(LSB)**

(MSB)							(LSB)	
MOS/FB 11	MOS/FB 10	MOS/FB 9	MOS/FB 8	(Note 1)	(Note 1)	(Note 1)	(Note 1)	MOSCR 1
MOS/FB 7	MOS/FB 6	MOS/FB 5	MOS/FB 4	MOS/FB 3	MOS/FB 2	MOS/F B1	MOS/FB 0	MOSCR 2

SYMBOL	POSITION	NAME AND DESCRIPTION
MOS/FB11	MOSCR1.7	**MSB of the 12-Bit Multiframes Out of Sync or F-Bit Error Count** (Note 2)
MOS/FB0	MOSCR2.0	**LSB of the 12-Bit Multiframes Out of Sync or F-Bit Error Count** (Note 2)

Note 1: *The lower nibble of the counter at address 25 is used by the Path Code Violation Count Register.*
Note 2: *MOSCR counts either errors in framing bit position (RCR2.0 = 0) or the number of multiframes out of sync (RCR2.0 = 1).*

Table 6-3. Multiframes Out of Sync Counting Arrangements

FRAMING MODE (CCR2.3)	COUNT MOS OR F-BIT ERRORS (RCR2.0)	WHAT IS COUNTED IN THE MOSCRs
D4	MOS	Number of multiframes out of sync
D4	F-Bit	Errors in the Ft pattern
ESF	MOS	Number of multiframes out of sync
ESF	F-Bit	Errors in the FPS pattern

7 DS0 MONITORING FUNCTION

The DS2152 can monitor one DS0 64kbps channel in the transmit direction and one DS0 channel in the receive direction at the same time. In the transmit direction, the user determines which channel is to be monitored by properly setting the TCM0 to TCM4 bits in the CCR5 register. In the receive direction, the RCM0 to RCM4 bits in the CCR6 register need to be properly set. The DS0 channel pointed to by the TCM0 to TCM4 bits will appear in the Transmit DS0 Monitor (TDS0M) register and the DS0 channel pointed to by the RCM0 to RCM4 bits will appear in the Receive DS0 (RDS0M) register.

The TCM4 to TCM0 and RCM4 to RCM0 bits should be programmed with the decimal decode of the appropriate T1 channel. For example, if DS0 channel 6 in the transmit direction and DS0 channel 15 in the receive direction needed to be monitored, then the following values would be programmed into CCR5 and CCR6:

TCM4 = 0	RCM4 = 0
TCM3 = 0	RCM3 = 1
TCM2 = 1	RCM2 = 1
TCM1 = 0	RCM1 = 1
TCM0 = 1	RCM0 = 0

CCR5: COMMON CONTROL REGISTER 5 (Address = 19 Hex)

(Repeated here from Section 4 for convenience.)

(MSB)							(LSB)
TJC	LLB	LIAIS	TCM4	TCM3	TCM2	TCM1	TCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
TJC	CCR5.7	**Transmit Japanese CRC Enable.** See Section 4 for details.
LLB	CCR5.6	**Local Loopback.** See Section 4 for details.
LIAIS	CCR5.5	**Line Interface AIS Generation Enable.** See Section 4 for details.
TCM4	CCR5.4	**Transmit Channel Monitor Bit 4.** MSB of a channel decode that determines which transmit DS0 channel data will appear in the TDS0M register.
TCM3	CCR5.3	**Transmit Channel Monitor Bit 3.**
TCM2	CCR5.2	**Transmit Channel Monitor Bit 2.**
TCM1	CCR5.1	**Transmit Channel Monitor Bit 1.**
TCM0	CCR5.0	**Transmit Channel Monitor Bit 0.** LSB of the channel decode that determines which transmit DS0 channel data will appear in the TDS0M register.

TDS0M: TRANSMIT DS0 MONITOR REGISTER (Address = 1A Hex)

(MSB)							(LSB)
B1	B2	B3	B4	B5	B6	B7	B8

SYMBOL	POSITION	NAME AND DESCRIPTION
B1	TDS0M.7	**Transmit DS0 Channel Bit 1.** MSB of the DS0 channel (first bit to be transmitted).
B2	TDS0M.6	**Transmit DS0 Channel Bit 2.**
B3	TDS0M.5	**Transmit DS0 Channel Bit 3.**
B4	TDS0M.4	**Transmit DS0 Channel Bit 4.**
B5	TDS0M.3	**Transmit DS0 Channel Bit 5.**
B6	TDS0M.2	**Transmit DS0 Channel Bit 6.**
B7	TDS0M.1	**Transmit DS0 Channel Bit 7.**
B8	TDS0M.0	**Transmit DS0 Channel Bit 8.** LSB of the DS0 channel (last bit to be transmitted).

CCR6: COMMON CONTROL REGISTER 6 (Address = 1E Hex)

(Repeated here from Section 4 for convenience.)

(MSB)							(LSB)
RJC	—	—	RCM4	RCM3	RCM2	RCM1	RCM0

SYMBOL	POSITION	NAME AND DESCRIPTION
RJC	CCR6.7	**Receive Japanese CRC Enable.** See Section 4 for details.
—	CCR6.6, CCR6.5	**Not Assigned.** Should be set to 0 when written.
RCM4	CCR6.4	**Receive Channel Monitor Bit 4.** MSB of a channel decode that determines which receive DS0 channel data will appear in the RDS0M register.
RCM3	CCR6.3	**Receive Channel Monitor Bit 3.**
RCM2	CCR6.2	**Receive Channel Monitor Bit 2.**
RCM1	CCR6.1	**Receive Channel Monitor Bit 1.**
RCM0	CCR6.0	**Receive Channel Monitor Bit 0.** LSB of the channel decode that determines which receive DS0 channel data will appear in the RDS0M register.

RDS0M: RECEIVE DS0 MONITOR REGISTER (Address = 1F Hex)

(MSB)							(LSB)
B1	B2	B3	B4	B5	B6	B7	B8

SYMBOL	POSITION	NAME AND DESCRIPTION
B1	RDS0M.7	**Receive DS0 Channel Bit 1.** MSB of the DS0 channel (first bit to be received).
B2	RDS0M.6	**Receive DS0 Channel Bit 2.**
B3	RDS0M.5	**Receive DS0 Channel Bit 3.**
B4	RDS0M.4	**Receive DS0 Channel Bit 4.**
B5	RDS0M.3	**Receive DS0 Channel Bit 5.**
B6	RDS0M.2	**Receive DS0 Channel Bit 6.**
B7	RDS0M.1	**Receive DS0 Channel Bit 7.**
B8	RDS0M.0	**Receive DS0 Channel Bit 8.** LSB of the DS0 channel (last bit to be received).

8 SIGNALING OPERATION

The DS2152 contains provisions for both processor based (i.e., software based) signaling bit access and for hardware-based access. Both the processor-based access and the hardware-based access can be used simultaneously if necessary. The processor based signaling is covered in Section 8.1 and the hardware based signaling is covered in Section 8.2.

8.1 Processor-Based Signaling

The robbed-bit signaling bits embedded in the T1 stream can be extracted from the receive stream and inserted into the transmit stream by the DS2152. There is a set of 12 registers for the receive side (RS1 to RS12) and 12 registers on the transmit side (TS1 to TS12). The signaling registers are detailed below. The CCR1.5 bit is used to control the robbed signaling bits as they appear at RSER. If CCR1.5 is set to 0, then the robbed signaling bits will appear at the RSER pin in their proper position as they are received. If CCR1.5 is set to 1, the robbed-signaling bit positions are forced to 1 at RSER. If hardware-based signaling is being used, then CCR1.5 must be set to 0.

RS1 TO RS12: RECEIVE SIGNALING REGISTERS (Address = 60 to 6B Hex)

(MSB)							(LSB)	
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	RS1 (60)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	RS2 (61)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	RS3 (62)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	RS4 (63)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	RS5 (64)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	RS6 (65)
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	RS7 (66)
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	RS8 (67)
A/C(24)	A/C(23)	A/C(22)	A/C(21)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	RS9 (68)
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	RS10 (69)
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	RS11 (6A)
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	RS12 (6B)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	RS12.7	**Signaling Bit D in Channel 24**
A(1)	RS1.0	**Signaling Bit A in Channel 1**

Each Receive Signaling Register (RS1 to RS12) reports the incoming robbed-bit signaling from eight DS0 channels. In the ESF framing mode, there can be up to four signaling bits per channel (A–D). In the D4 framing mode, there are only two signaling bits per channel (A and B). In the D4 framing mode, the DS2152 replaces the C and D signaling bit positions with the A and B signaling bits from the previous multiframe. Hence, whether the DS2152 is operated in either framing mode, the user needs only to retrieve the signaling bits every 3ms. The bits in the Receive Signaling Registers are updated on multiframe boundaries so the user can use the Receive Multiframe Interrupt in the Receive Status Register 2 (SR2.7) to know when to retrieve the signaling bits. The Receive Signaling Registers are frozen and not updated during a loss of sync condition (SR1.0 = 1). They will contain the most recent signaling information before the "OOF" occurred. The signaling data reported in RS1 to RS12 is also available at the RSIG and RSER pins.

A change in the signaling bits from one multiframe to the next will cause the RSC status bit (SR2.0) to be set. The user can enable the $\overline{INT}$ pin to toggle low upon detection of a change in signaling by setting the IMR2.0 bit. Once a signaling change has been detected, the user has at least 2.75ms to read the data out of the RS1 to RS12 registers before the data will be lost.

TS1 TO TS12: TRANSMIT SIGNALING REGISTERS (Address = 70 to 7B Hex)

(MSB)							(LSB)	
A(8)	A(7)	A(6)	A(5)	A(4)	A(3)	A(2)	A(1)	TS1 (70)
A(16)	A(15)	A(14)	A(13)	A(12)	A(11)	A(10)	A(9)	TS2 (71)
A(24)	A(23)	A(22)	A(21)	A(20)	A(19)	A(18)	A(17)	TS3 (72)
B(8)	B(7)	B(6)	B(5)	B(4)	B(3)	B(2)	B(1)	TS4 (73)
B(16)	B(15)	B(14)	B(13)	B(12)	B(11)	B(10)	B(9)	TS5 (74)
B(24)	B(23)	B(22)	B(21)	B(20)	B(19)	B(18)	B(17)	TS6 (75)
A/C(8)	A/C(7)	A/C(6)	A/C(5)	A/C(4)	A/C(3)	A/C(2)	A/C(1)	TS7 (76)
A/C(16)	A/C(15)	A/C(14)	A/C(13)	A/C(12)	A/C(11)	A/C(10)	A/C(9)	TS8 (77)
A/C(24)	A/C(23)	A/C(22)	A/C(21)	A/C(20)	A/C(19)	A/C(18)	A/C(17)	TS9 (78)
B/D(8)	B/D(7)	B/D(6)	B/D(5)	B/D(4)	B/D(3)	B/D(2)	B/D(1)	TS10 (79)
B/D(16)	B/D(15)	B/D(14)	B/D(13)	B/D(12)	B/D(11)	B/D(10)	B/D(9)	TS11 (7A)
B/D(24)	B/D(23)	B/D(22)	B/D(21)	B/D(20)	B/D(19)	B/D(18)	B/D(17)	TS12 (7B)

SYMBOL	POSITION	NAME AND DESCRIPTION
D(24)	TS12.7	**Signaling Bit A in Channel 24**
A(1)	TS1.0	**Signaling Bit D in Channel 1**

Each Transmit Signaling Register (TS1 to TS12) contains the robbed-bit signaling for eight DS0 channels that will be inserted into the outgoing stream if enabled to do so via TCR1.4. In the ESF framing mode, there can be up to four signaling bits per channel (A–D). On multiframe boundaries, the DS2152 will load the values present in the Transmit Signaling Register into an outgoing signaling shift register that is internal to the device. The user can utilize the Transmit Multiframe Interrupt in Status Register 2 (SR2.6) to know when to update the signaling bits. In the ESF framing mode, the interrupt will come every 3 ms and the user has a full 3ms to update the TSRs. In the D4 framing mode, there are only 2 signaling bits per channel (A and B). However, in the D4 framing mode the DS2152 uses the C and D bit positions as the A and B bit positions for the next multiframe. The DS2152 loads the values in the TSRs into the outgoing shift register every other D4 multiframe.

8.2 Hardware-Based Signaling

8.2.1 Receive Side

In the receive side of the hardware based signaling, there are two operating modes for the signaling buffer: signaling extraction and signaling reinsertion. Signaling extraction involves pulling the signaling bits from the receive data stream and buffering them over a four multiframe buffer and outputting them in a serial PCM fashion on a channel-by-channel basis at the RSIG output. This mode is always enabled. In this mode, the receive elastic store may be enabled or disabled. If the receive elastic store is enabled, then the backplane clock (RSYSCLK) can be either 1.544MHz or 2.048MHz. In the ESF framing mode, the ABCD signaling bits are output on RSIG in the lower nibble of each channel. The RSIG data is updated once a multiframe (3ms) unless a freeze is in effect. In the D4 framing mode, the AB signaling bits are output twice on RSIG in the lower nibble of each channel. Hence, bits 5 and 6 contain the same data as bits 7 and 8, respectively, in each channel. The RSIG data is updated once a multiframe (1.5ms) unless a freeze is in effect. See the timing diagrams in Section 16 for some examples.

The other hardware-based signaling operating mode called signaling reinsertion can be invoked by setting the RSRE control bit high (CCR4.7 = 1). In this mode, the user will provide a multiframe sync at the RSYNC pin and the signaling data will be re-aligned at the RSER output according to this applied multiframe boundary. In this mode, the elastic store must be enabled however the backplane clock can be either 1.544MHz or 2.048MHz.

If the signaling reinsertion mode is enabled, the user can control which channels have signaling reinsertion performed on a channel-by-channel basis by setting the RPCSI control bit high (CCR4.6) and then programming the RCHBLK output pin to go high in the channels in which the signaling reinsertion should not occur. If the RPCSI bit is set low, then signaling reinsertion will occur in all channels when the signaling reinsertion mode is enabled (RSRE = 1). How to control the operation of the RCHBLK output pin is covered in Section 10. In signaling reinsertion mode, the user has the option to replace all of the extracted robbed-bit signaling bit positions with 1s. This option is enabled via the RFSA1 control bit (CCR4.5) and it can be invoked on a per-channel basis by setting the RPCSI control bit (CCR4.6) high and then programming RCHBLK appropriately just like the per-channel signaling reinsertion operates.

The signaling data in the four-multiframe buffer will be frozen in a known good state upon either a loss of synchronization (OOF event), carrier loss, or frame slip. This action meets the requirements of BellCore TR-TSY-000170 for signaling freezing. To allow this freeze action to occur, the RFE control bit (CCR4.4) should be set high. The user can force a freeze by setting the RFF control bit (CCR4.3) high. The RSIGF output pin provides a hardware indication that a freeze is in effect. The four-multiframe buffer provides a three-multiframe delay in the signaling bits provided at the RSIG pin (and at the RSER pin if RSRE = 1). When freezing is enabled (RFE = 1), the signaling data will be held in the last known good state until the corrupting error condition subsides. When the error condition subsides, the signaling data will be held in the old state for at least an additional 9ms (or 4.5ms in D4 framing mode) before being allowed to be updated with new signaling data.

8.2.2 Transmit Side

Via the THSE control bit (CCR4.2), the DS2152 can be set up to take the signaling data presented at the TSIG pin and insert the signaling data into the PCM data stream that is being input at the TSER pin. The user can control which channels are to have signaling data from the TSIG pin inserted into them on a channel-by-channel basis by setting the TPCSI control bit (CCR4.1) high. When TPCSI is enabled, channels in which the TCHBLK output has been programmed to be set high in, will not have signaling data from the TSIG pin inserted into them. The hardware signaling insertion capabilities of the DS2152 are available whether the transmit side elastic store is enabled or disabled. If the elastic store is enabled, the backplane clock (TSYSCLK) can be either 1.544 MHz or 2.048 MHz.

9 PER-CHANNEL CODE (IDLE) GENERATION AND LOOPBACK

The DS2152 can replace data on a channel-by-channel basis in both the transmit and receive directions. The transmit direction is from the backplane to the T1 line and is covered in Section 9.1. The receive direction is from the T1 line to the backplane and is covered in Section 9.2.

9.1 Transmit Side Code Generation

In the transmit direction there are two methods by which channel data from the backplane can be overwritten with data generated by the DS2152. The first method, which is covered in Section 9.1.1, was a feature contained in the original DS2151 while the second method, which is covered in Section 9.1.2, is a new feature of the DS2152.

9.1.1 Simple Idle Code Insertion and Per-Channel Loopback

The first method involves using the Transmit Idle Registers (TIR1/2/3) to determine which of the 24 T1 channels should be overwritten with the code placed in the Transmit Idle Definition Register (TIDR). This method allows the same 8-bit code to be placed into any of the 24 T1 channels. If this method is used, then the CCR4.0 control bit must be set to 0.

Each of the bit positions in the Transmit Idle Registers (TIR1/TIR2/TIR3) represents a DS0 channel in the outgoing frame. When these bits are set to a 1, the corresponding channel will transmit the Idle Code contained in the Transmit Idle Definition Register (TIDR). Robbed-bit signaling and Bit 7 stuffing will occur over the programmed Idle Code unless the DS0 channel is made transparent by the Transmit Transparency Registers.

The Transmit Idle Registers (TIRs) have an alternate function that allows them to define a Per-Channel Loop-Back (PCLB). If the TIRFS control bit (CCR4.0) is set to 1, then the TIRs will determine which channels (if any) from the backplane should be replaced with the data from the receive side or, in other words, off of the T1 line. If this mode is enabled, then transmit and receive clocks and frame syncs must be synchronized. One method to accomplish this would be to tie RCLK to TCLK and RFSYNC to TSYNC.

TIR1/TIR2/TIR3: TRANSMIT IDLE REGISTERS (Address = 3C to 3E Hex)

(Also used for Per-Channel Loopback.)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TIR1 (3C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TIR2 (3D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TIR3 (3E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TIR3.7	**Transmit Idle Registers.** 0 = do not insert the Idle Code in the TIDR into this channel
CH1	TIR1.0	1 = insert the Idle Code in the TIDR into this channel

Note: *If CCR4.0 = 1, then a 0 in the TIRs implies that channel data is to be sourced from TSER and a 1 implies that channel data is to be sourced from the output of the receive side framer (i.e., Per-Channel Loopback; see Figure 1-1).*

TIDR: TRANSMIT IDLE DEFINITION REGISTER (Address = 3F Hex)

(MSB) **(LSB)**

TIDR7	TIDR6	TIDR5	TIDR4	TIDR3	TIDR2	TIDR1	TIDR0

SYMBOL	POSITION	NAME AND DESCRIPTION
TIDR7	TIDR.7	**MSB of the Idle Code (this bit is transmitted first).**
TIDR0	TIDR.0	**LSB of the Idle Code (this bit is transmitted last).**

9.1.2 Per-Channel Code Insertion

The second method involves using the Transmit Channel Control Registers (TCC1/2/3) to determine which of the 24 T1 channels should be overwritten with the code placed in the Transmit Channel Registers (TC1 to TC24). This method is more flexible than the first in that it allows a different 8-bit code to be placed into each of the 24 T1 channels.

TC1 TO TC24: TRANSMIT CHANNEL REGISTERS (Address = 40 to 4F and 50 to 57 Hex)

(For brevity, only channel 1 is shown; see Table 2-1 for other register address.)

(MSB) **(LSB)**

C7	C6	C5	C4	C3	C2	C1	C0	TC1 (50)

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	TC1.7	**MSB of the Code (this bit is transmitted first).**
C0	TC1.0	**LSB of the Code (this bit is transmitted last).**

TCC1/TCC2/TCC3: TRANSMIT CHANNEL CONTROL REGISTER (Address = 16 to 18 Hex)

(MSB) **(LSB)**

CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCC1 (16)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCC2 (17)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCC3 (18)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TCC3.7	**Transmit Channel 24 Code Insertion Control Bit** 0 = do not insert data from the TC1 register into the transmit data stream 1 = insert data from the TC1 register into the transmit data stream
CH1	TCC1.0	**Transmit Channel 1 Code Insertion Control Bit** 0 = do not insert data from the TC32 register into the transmit data stream 1 = insert data from the TC32 register into the transmit data stream

9.2 Receive Side Code Generation

In the receive direction there are also two methods by which channel data to the backplane can be overwritten with data generated by the DS2152. The first method, which is covered in Section 9.2.1, was a feature contained in the original DS2151, while the second method, which is covered in Section 9.2.2, is a new feature of the DS2152.

9.2.1 Simple Code Insertion

The first method on the receive side involves using the Receive Mark Registers (RMR1/2/3) to determine which of the 24 T1 channels should be overwritten with either a 7Fh idle code or with a digital milliwatt pattern. The RCR2.7 bit will determine which code is used. The digital milliwatt code is an 8-byte repeating pattern that represents a 1kHz sine wave (1E/0B/0B/1E/9E/8B/8B/9E). Each bit in the RMRs represents a particular channel. If a bit is set to a 1, then the receive data in that channel will be replaced with one of the two codes. If a bit is set to 0, no replacement occurs.

RMR1/RMR2/RMR3: RECEIVE MARK REGISTERS (Address = 2D to 2F Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RMR1(2D)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RMR2(2E)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RMR3(2F)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	RMR3.7	**Receive MARK Registers.** 0 = do not affect the receive data associated with this channel
CH1	RMR1.0	1 = replace the receive data associated with this channel with either the idle code or the digital milliwatt code (depends on the RCR2.7 bit)

9.2.2 Per-Channel Code Insertion

The second method involves using the Receive Channel Control Registers (RCC1/2/3) to determine which of the 24 T1 channels off the T1 line and going to the backplane should be overwritten with the code placed in the Receive Channel Registers (RC1 to RC24). This method is more flexible than the first in that it allows a different 8-bit code to be placed into each of the 24 T1 channels.

RC1 TO RC24: RECEIVE CHANNEL REGISTERS (Address = 58 to 5F and 80 to 8F Hex)

(For brevity, only channel 1 is shown; see Table 2-1 for other register address.)

(MSB)							(LSB)	
C7	C6	C5	C4	C3	C2	C1	C0	RC1 (58)

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	RC1.7	**MSB of the Code (this bit is sent first to the backplane)**
C0	RC1.0	**LSB of the Code (this bit is sent last to the backplane)**

RCC1/RCC2/RCC3: RECEIVE CHANNEL CONTROL REGISTER (Address = 1B to 1D Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCC1 (1B)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCC2 (1C)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCC3 (1D)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	RCC3.7	**Receive Channel 24 Code Insertion Control Bit** 0 = do not insert data from the RC24 register into the receive data stream 1 = insert data from the RC24 register into the receive data stream
CH1	RCC1.0	**Receive Channel 1 Code Insertion Control Bit** 0 = do not insert data from the RC1 register into the receive data stream 1 = insert data from the RC1 register into the receive data stream

10 CLOCK BLOCKING REGISTERS

The Receive Channel Blocking Registers (RCBR1/RCBR2/RCBR3) and the Transmit Channel Blocking Registers (TCBR1/TCBR2/TCBR3) control the RCHBLK and TCHBLK pins, respectively. The RCHBLK and TCHCLK pins are user-programmable outputs that can be forced either high or low during individual channels. These outputs can be used to block clocks to a USART or LAPD controller in Fractional T1 or ISDN-PRI applications. When the appropriate bits are set to 1, the RCHBLK and TCHCLK pins will be held high during the entire corresponding channel time. See the timing diagrams in Section 16 for an example.

RCBR1/RCBR2/RCBR3: RECEIVE CHANNEL BLOCKING REGISTERS (Address = 6C to 6E Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	RCBR1 (6C)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	RCBR2 (6D)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	RCBR3 (6E)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	RCBR3.7	**Receive Channel Blocking Registers.** 0 = force the RCHBLK pin to remain low during this channel time
CH1	RCBR1.0	1 = force the RCHBLK pin high during this channel time

TCBR1/TCBR2/TCBR3: TRANSMIT CHANNEL BLOCKING REGISTERS (Address = 32 to 34 Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TCBR1 (32)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TCBR1 (33)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TCBR1 (34)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TCBR3.7	**Transmit Channel Blocking Registers.** 0 = force the TCHBLK pin to remain low during this channel time
CH1	TCBR1.0	1 = force the TCHBLK pin high during this channel time

11 ELASTIC STORES OPERATION

The DS2152 contains dual two-frame (386 bits) elastic stores: one for the receive direction and one for the transmit direction. These elastic stores have two main purposes. First, they can be used to rate convert the T1 data stream to 2.048Mbps (or a multiple of 2.048Mbps), which is the E1 rate. Secondly, they can be used to absorb the differences in frequency and phase between the T1 data stream and an asynchronous (i.e., not frequency locked) backplane clock (which can be 1.544MHz or 2.048MHz). The backplane clock can burst at rates up to 8.192MHz. Both elastic stores contain fully controlled slip capability, which is necessary for this second purpose. The receive side elastic store can be enabled via CCR1.2 and the transmit side elastic store is enabled via CCR1.7. The elastic stores can be forced to a known depth via the Elastic Store Reset bit (CCR3.6). Toggling the CCR3.6 bit forces the read and write pointers into opposite frames. Both elastic stores within the DS2152 are fully independent and no restrictions apply to the sourcing of the various clocks that are applied to them. The transmit side elastic store can be enabled whether the receive elastic store is enabled or disabled and vice versa. Also, each elastic store can interface to either a 1.544MHz or 2.048MHz backplane without regard to the backplane rate the other elastic store is interfacing.

11.1 Receive Side

If the receive side elastic store is enabled (CCR1.2 = 1), then the user must provide either a 1.544MHz (CCR1.3 = 0) or 2.048MHz (CCR1.3 = 1) clock at the RSYSCLK pin. The user has the option of either providing a frame/multiframe sync at the RSYNC pin (RCR2.3 = 1) or having the RSYNC pin provide a pulse on frame boundaries (RCR2.3 = 0). If the user wishes to obtain pulses at the frame boundary, then RCR2.4 must be set to 0; if the user wishes to have pulses occur at the multiframe boundary, then RCR2.4 must be set to 1. The DS2152 always indicates frame boundaries via the RFSYNC output whether the elastic store is enabled or not. If the elastic store is enabled, then multiframe boundaries will be indicated via the RMSYNC output. If the user selects to apply a 2.048MHz clock to the RSYSCLK pin, then the data output at RSER will be forced to all 1s every fourth channel and the F-bit will be placed in the MSB bit position of channel 1. Hence, channels 1, 5, 9, 13, 17, 21, 25, and 29 (time slots 0, 4, 8, 12, 16, 20, 24, and 28) are forced to 1. Also, in 2.048MHz applications, the RCHBLK output is forced high during the same channels as the RSER pin. See Section 16 for more details. This is useful in T1 to CEPT (E1) conversion applications. If the 386-bit elastic buffer either fills or empties, a controlled slip occurs. If the buffer empties, a full frame of data (193 bits) is repeated at RSER, and the SR1.4 and RIR1.3 bits are set to 1, except the MSB of channel 1. See Figure 16-5. If the buffer fills, a full frame of data is deleted, and the SR1.4 and RIR1.4 bits are set to 1.

11.2 Transmit Side

The operation of the transmit elastic store is very similar to the receive side. The transmit side elastic store is enabled via CCR1.7. A 1.544MHz (CCR1.4 = 0) or 2.048MHz (CCR1.4 = 1) clock can be applied to the TSYSCLK input. If the user selects to apply a 2.048MHz clock to the TSYSCLK pin, then the data input at TSER will be ignored every fourth channel. Hence, channels 1, 5, 9, 13, 17, 21, 25, and 29 (time slots 0, 4, 8, 12, 16, 20, 24, and 28) are ignored. The F-bit may be sampled at the MSB of channel 1. See Figure 16-10. The user must supply an 8kHz frame sync pulse to the TSSYNC input. Also, in 2.048MHz applications the TCHBLK output is forced high during the channels ignored by the DS2152. See Section 16 for more details. Controlled slips in the transmit elastic store are reported in the RIR2.3 bit, and the direction of the slip is reported in the RIR2.5 and RIR2.4 bits.

11.3 Minimum Delay Synchronous RSYSCLK/TSYSCLK Mode

In applications where the DS2152 is connected to backplanes that are frequency-locked to the recovered T1 clock (i.e., the RCLK output), the full two-frame depth of the on-board elastic stores is really not needed. In fact, in some delay-sensitive applications the normal two-frame depth may be excessive. If the CCR3.7 bit is set to 1, then the receive elastic store (and also the transmit elastic store if it is enabled) will be forced to a maximum depth of 32 bits instead of the normal 386 bits. In this mode, RSYSCLK and TSYSCLK must be tied together and they must be frequency-locked to RCLK. All the slip contention logic in the DS2152 is disabled (since slips cannot occur). Also, since the buffer depth is no longer two frames deep, the DS2152 must be set up to source a frame pulse at the RSYNC pin and this output must be tied to the TSSYNC input. On power-up after the RSYSCLK and TSYSCLK signals have locked to the RCLK signal, the elastic store reset bit (CCR3.6) should be toggled from 0 to 1 to ensure proper operation.

12 FDL/FS EXTRACTION AND INSERTION

The DS2152 can extract/insert data from/into the Facility Data Link (FDL) in the ESF framing mode and from/into Fs-bit position in the D4 framing mode. Because SLC-96 uses the Fs-bit position, this capability can also be used in SLC-96 applications. The DS2152 contains a complete HDLC and BOC controller for the FDL. See Section 12.1 for this operation. To allow for backward compatibility between the DS2152 and earlier devices, the DS2152 maintains some legacy functionality for the FDL (see Section 12.2). Section 12.3 covers D4 and SLC-96 operation. Contact the factory for a copy of C language source code for implementing the FDL on the DS2152.

12.1 HDLC and BOC Controller for the FDL

The DS2152 contains a complete HDLC controller with 16-byte buffers in both the transmit and receive directions as well as separate dedicated hardware for Bit Oriented Codes (BOC). The HDLC controller performs all the necessary overhead for generating and receiving Performance Report Messages (PRM) as described in ANSI T1.403 and the messages as described in AT&T TR54016. The HDLC controller automatically generates and detects flags, generates and checks the CRC check sum, generates and detects abort sequences, stuffs and destuffs 0s (for transparency), and byte-aligns to the FDL data stream. The 16-byte buffers in the HDLC controller are large enough to allow a full PRM to be received or transmitted without host intervention. The BOC controller will automatically detect incoming BOC sequences and alert the host. When the BOC ceases, the DS2152 will also alert the host. The user can set the device up to send any of the possible 6-bit BOC codes.

There are nine registers that the host will use to operate and control the operation of the HDLC and BOC controllers. A brief description of the registers is shown in Table 12-1.

Table 12-1. HDLC/BOC Controller Register List

NAME	FUNCTION
FDL Control Register (FDLC) FDL Status Register (FDLS) FDL Interrupt Mask Register (FIMR)	General control over the HDLC and BOC controllers key status information for both transmit and receive directions allows/stops status bits to/from causing an interrupt.
Receive PRM Register (RPRM) Receive BOC Register (RBOC) Receive FDL FIFO Register (RFFR)	Status information on receive HDLC controller status information on receive BOC controller access to 16-byte HDLC FIFO in receive direction.
Transmit PRM Register (TPRM) Transmit BOC Register (TBOC) Transmit FDL FIFO Register (TFFR)	Status information on transmit HDLC controller enables/disables transmission of BOC codes access to 16-byte HDLC FIFO in transmit direction.

12.1.1 Status Register for the FDL

Four of the HDLC/BOC controller registers (FDLS, RPRM, RBOC, and TPRM) provide status information. When a particular event has occurred (or is occurring), the appropriate bit in one of these four registers will be set to a 1. Some of the bits in these four FDL status registers are latched and some are real-time bits that are not latched. Section 12 contains register descriptions that list which bits are latched and which are not. With the latched bits, when an event occurs and a bit is set to a 1, it will remain set until the user reads that bit. The bit will be cleared when it is read and it will not be set again until the event has occurred again. The real-time bits report the current instantaneous conditions that are occurring, and the history of these bits is not latched.

Like the other status registers in the DS2152, the user will always precede a read of any of the four registers with a write. The byte written to the register will inform the DS2152 which of the latched bits the user wishes to read and have cleared (the real-time bits are not affected by writing to the status register). The user will write a byte to one of these registers, with a 1 in the bit positions he or she wishes to read and a 0 in the bit positions he or she does not wish to obtain the latest information on. When a 1 is written to a bit location, the read register will be updated with current value and it will be cleared. When a 0 is written to a bit position, the read register will not be updated and the previous value will be held. A write to the status and information registers will be immediately followed by a read of the same register. The read result should be logically ANDed with the mask byte that was just written and this value should be written back into the same register to insure that bit does indeed clear. This second write step is necessary because the alarms and events in the status registers occur asynchronously in respect to their access via the parallel port. This write-read-write (for polled driven access) or write-read (for interrupt-driven access) scheme allows an external microcontroller or microprocessor to individually poll certain bits without disturbing the other bits in the register. This operation is key in controlling the DS2152 with higher-order software languages.

Like the SR1 and SR2 status registers, the FDLS register has the unique ability to initiate a hardware interrupt via the $\overline{\text{INT}}$ output pin. Each of the events in the FDLS can be either masked or unmasked from the interrupt pin via the FDL Interrupt Mask Register (FIMR). Interrupts will force the $\overline{\text{INT}}$ pin low when the event occurs. The $\overline{\text{INT}}$ pin will be allowed to return high (if no other interrupts are present) when the user reads the event bit that caused the interrupt to occur.

12.1.2 Basic Operation Details

To allow the DS2152 to properly source/receive data from/to the HDLC and BOC controller the legacy FDL circuitry (which is described in Section 12.2) should be disabled and the following bits should be programmed as shown:

TCR1.2 = 1 (source FDL data from the HDLC and BOC controller)
TBOC.6 = 1 (enable HDLC and BOC controller)
CCR2.5 = 0 (disable SLC-96 and D4 Fs-bit insertion)
CCR2.4 = 0 (disable legacy FDL 0 stuffer)
CCR2.1 = 0 (disable SLC-96 reception)
CCR2.0 = 0 (disable legacy FDL 0 stuffer)
IMR2.4 = 0 (disable legacy receive FDL buffer full interrupt)
IMR2.3 = 0 (disable legacy transmit FDL buffer empty interrupt)
IMR2.2 = 0 (disable legacy FDL match interrupt)
IMR2.1 = 0 (disable legacy FDL abort interrupt)

As a basic guideline for interpreting and sending both HDLC messages and BOC messages, the following sequences can be applied:

12.1.3 Receive an HDLC Message or a BOC

1) Enable RBOC and RPS interrupts.
2) Wait for interrupt to occur.
3) If RBOC = 1, then follow steps 5 and 6.
4) If RPS = 1, then follow steps 7 thru 12.
5) If LBD = 1, a BOC is present, then read the code from the RBOC register and take action as needed.
6) If BD = 0, a BOC has ceased, take action as needed and then return to step 1.
7) Disable RPS interrupt and enable either RPE, RNE, or RHALF interrupt.
8) Read RPRM to obtain REMPTY status.
   a. If REMPTY = 0, then record OBYTE, CBYTE, and POK bits and then read the FIFO .
      a1. If CBYTE = 0 then skip to step 9.
      a2. If CBYTE = 1 then skip to step 11.
   b. If REMPTY = 1, then skip to step 10.
9) Repeat step 8.
10) Wait for interrupt, skip to step 8.
11) If POK = 0, then discard whole packet, if POK = 1, accept the packet.
12) Disable RPE, RNE, or RHALF interrupt, enable RPS interrupt and return to step 1.

12.1.4 Transmit an HDLC Message

1) Make sure HDLC controller is finished sending any previous messages and is currently sending flags by checking that the FIFO is empty by reading the TEMPTY status bit in the TPRM register.
2) Enable either the THALF or TNF interrupt.
3) Read TPRM to obtain TFULL status.
   a. If TFULL = 0, then write a byte into the FIFO and skip to next step (special case occurs when the last byte is to be written, in this case set TEOM = 1 before writing the byte and then skip to step 6).
   b. If TFULL = 1, then skip to step 5.
4) Repeat step 3.
5) Wait for interrupt, skip to step 3.
6) Disable THALF or TNF interrupt and enable TMEND interrupt.
7) Wait for an interrupt, then read TUDR status bit to make sure packet was transmitted correctly.

12.1.5 Transmit a BOC

1) Write 6-bit code into TBOC.
2) Set SBOC bit in TBOC = 1.

12.1.6 HDLC/BOC Register Description

FDLC: FDL CONTROL REGISTER (Address = 00 Hex)

(MSB) … **(LSB)**

RBR	RHR	TFS	THR	TABT	TEOM	TZSD	TCRCF

SYMBOL	POSITION	NAME AND DESCRIPTION
RBR	FDLC.7	**Receive BOC Reset.** A 0 to 1 transition will reset the BOC circuitry. Must be cleared and set again for a subsequent reset.
RHR	FDLC.6	**Receive HDLC Reset.** A 0 to 1 transition will reset the HDLC controller. Must be cleared and set again for a subsequent reset.
TFS	FDLC.5	**Transmit Flag/Idle Select.** 0 = 7Eh 1 = FFh
THR	FDLC.4	**Transmit HDLC Reset.** A 0 to 1 transition will reset both the HDLC controller and the transmit BOC circuitry. Must be cleared and set again for a subsequent reset.
TABT	FDLC.3	**Transmit Abort.** A 0 to 1 transition will cause the FIFO contents to be dumped and one FEh abort to be sent followed by 7Eh or FFh flags/idle until a new packet is initiated by writing new data into the FIFO. Must be cleared and set again for a subsequent abort to be sent.
TEOM	FDLC.2	**Transmit End of Message.** Should be set to a 1 just before the last data byte of a HDLC packet is written into the transmit FIFO at TFFR. This bit will be cleared by the HDLC controller when the last byte has been transmitted.
TZSD	FDLC.1	**Transmit 0 Stuffer Defeat.** Overrides internal enable. 0 = enable the 0 stuffer (normal operation) 1 = disable the 0 stuffer
TCRCD	FDLC.0	**Transmit CRC Defeat.** 0 = enable CRC generation (normal operation) 1 = disable CRC generation

FDLS: FDL STATUS REGISTER (Address = 01 Hex)

(MSB)							(LSB)
RBOC	RPE	RPS	RHALF	RNE	THALF	TNF	TMEND

SYMBOL	POSITION	NAME AND DESCRIPTION
RBOC	FDLS.7	**Receive BOC Detector Change of State.** Set whenever the BOC detector sees a change of state from a BOC Detected to a No Valid Code seen or vice versa. The setting of this bit prompt the user to read the RBOC register for details.
RPE	FDLS.6	**Receive Packet End.** Set when the HDLC controller detects either the finish of a valid message (i.e., CRC check complete) or when the controller has experienced a message fault such as a CRC checking error, or an overrun condition, or an abort has been seen. The setting of this bit prompts the user to read the RPRM register for details.
RPS	FDLS.5	**Receive Packet Start.** Set when the HDLC controller detects an opening byte. The setting of this bit prompts the user to read the RPRM register for details.
RHALF	FDLS.4	**Receive FIFO Half Full.** Set when the receive 16-byte FIFO fills beyond the halfway point. The setting of this bit prompts the user to read the RPRM register for details.
RNE	FDLS.3	**Receive FIFO Not Empty.** Set when the receive 16-byte FIFO has at least 1 byte available for a read. The setting of this bit prompts the user to read the RPRM register for details.
THALF	FDLS.2	**Transmit FIFO Half Empty.** Set when the transmit 16-byte FIFO empties beyond the halfway point. The setting of this bit prompts the user to read the TPRM register for details.
TNF	FDLS.1	**Transmit FIFO Not Full.** Set when the transmit 16-byte FIFO has at least 1 byte available. The setting of this bit prompts the user to read the TPRM register for details.
TMEND	FDLS.0	**Transmit Message End.** Set when the transmit HDLC controller has finished sending a message. The setting of this bit prompts the user to read the TPRM register for details.

Note: *The RBOC, RPE, RPS, and TMEND bits are latched and will be cleared when read.*

FIMR: FDL INTERRUPT MASK REGISTER (Address = 02 Hex)

(MSB)							(LSB)
RBOC	RPE	RPS	RHALF	RNE	THALF	TNF	TMEND

SYMBOL	POSITION	NAME AND DESCRIPTION
RBOC	FIMR.7	**Receive BOC Detector Change of State.** 0 = interrupt masked 1 = interrupt enabled
RPE	FIMR.6	**Receive Packet End.** 0 = interrupt masked 1 = interrupt enabled
RPS	FIMR.5	**Receive Packet Start.** 0 = interrupt masked 1 = interrupt enabled
RHALF	FIMR.4	**Receive FIFO Half Full.** 0 = interrupt masked 1 = interrupt enabled
RNE	FIMR.3	**Receive FIFO Not Empty.** 0 = interrupt masked 1 = interrupt enabled
THALF	FIMR.2	**Transmit FIFO Half Empty.** 0 = interrupt masked 1 = interrupt enabled
TNF	FIMR.1	**Transmit FIFO Not Full.** 0 = interrupt masked 1 = interrupt enabled
TMEND	FIMR.0	**Transmit Message End.** 0 = interrupt masked 1 = interrupt enabled

RPRM: RECEIVE RPM REGISTER (Address = 03 Hex)

(MSB) **(LSB)**

RABT	RCRCE	ROVR	RVM	REMPTY	POK	CBYTE	OBYTE

SYMBOL	POSITION	NAME AND DESCRIPTION
RABT	RPRM.7	**Abort Sequence Detected.** Set whenever the HDLC controller sees seven or more 1s in a row.
RCRCE	RPRM.6	**CRC Error.** Set when the CRC checksum is in error.
ROVR	RPRM.5	**Overrun.** Set when the HDLC controller has attempted to write a byte into an already full receive FIFO.
RVM	RPRM.4	**Valid Message.** Set when the HDLC controller has detected and checked a complete HDLC packet.
REMPTY	RPRM.3	**Empty.** A real-time bit that is set high when the receive FIFO is empty.
POK	RPRM.2	**Packet OK.** Set when the byte available for reading in the receive FIFO at RFDL is the last byte of a valid message (and hence no abort was seen, no overrun occurred, and the CRC was correct).
CBYTE	RPRM.1	**Closing Byte.** Set when the byte available for reading in the receive FIFO at RFDL is the last byte of a message (whether the message was valid or not).
OBYTE	RPRM.0	**Opening Byte.** Set when the byte available for reading in the receive FIFO at RFDL is the first byte of a message.

Note: *The RABT, RCRCE, ROVR, and RVM bits are latched and will be cleared when read.*

RBOC: RECEIVE BOC REGISTER (Address = 04 Hex)

(MSB) **(LSB)**

LBD	BD	BOC5	BOC4	BOC3	BOC2	BOC1	BOC0

SYMBOL	POSITION	NAME AND DESCRIPTION
LBD	RBOC.7	**Latched BOC Detected.** A latched version of the BD status bit (RBOC.6). Will be cleared when read.
BD	RBOC.6	**BOC Detected.** A real-time bit that is set high when the BOC detector is presently seeing a valid sequence and set low when no BOC is currently being detected.
BOC5	RBOC.5	**BOC Bit 5.** Last bit received of the 6-bit codeword.
BOC4	RBOC.4	**BOC Bit 4.**
BOC3	RBOC.3	**BOC Bit 3.**
BOC2	RBOC.2	**BOC Bit 2.**
BOC1	RBOC.1	**BOC Bit 1.**
BOC0	RBOC.0	**BOC Bit 0.** First bit received of the 6-bit codeword.

Note 1: *The LBD bit is latched and will be cleared when read.*
Note 2: *The RBOC0 to RBOC5 bits display the last valid BOC code verified; these bits will be set to all 1s on reset.*

RFFR: RECEIVE FDL FIFO REGISTER (Address = 05 Hex)

(MSB) **(LSB)**

FDL7	FDL6	FDL5	FDL4	FDL3	FDL2	FDL1	FDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
FDL7	RFFR.7	**FDL Data Bit 7.** MSB of a HDLC packet data byte.
FDL6	RFFR.6	**FDL Data Bit 6.**
FDL5	RFFR.5	**FDL Data Bit 5.**
FDL4	RFFR.4	**FDL Data Bit 4.**
FDL3	RFFR.3	**FDL Data Bit 3.**
FDL2	RFFR.2	**FDL Data Bit 2.**
FDL1	RFFR.1	**FDL Data Bit 1.**
FDL0	RFFR.0	**FDL Data Bit 0.** LSB of a HDLC packet data byte.

TPRM: TRANSMIT PRM REGISTER (Address = 06 Hex)

(MSB) (LSB)

—	—	—	—	—	TEMPTY	TFULL	UDR

SYMBOL	POSITION	NAME AND DESCRIPTION
—	TPRM.7 to TPRM.3	**Not Assigned.** Could be any value when read.
TEMPTY	TPRM.2	**Transmit FIFO Empty.** A real-time bit that is set high when the FIFO is empty.
TFULL	TPRM.1	**Transmit FIFO Full.** A real-time bit that is set high when the FIFO is full.
UDR	TPRM.0	**Underrun.** Set when the transmit FIFO unwantedly empties out and an abort is automatically sent.

Note: *The UDR bit is latched and will be cleared when read.*

TBOC: TRANSMIT BOC REGISTER (Address = 07 Hex)

(MSB) (LSB)

SBOC	HBEN	BOC5	BOC4	BOC3	BOC2	BOC1	BOC0

SYMBOL	POSITION	NAME AND DESCRIPTION
SBOC	TBOC.7	**Send BOC.** Rising edge triggered. Must be transitioned from a 0 to a 1 transmit the BOC code placed in the BOC0 to BOC5 bits instead of data from the HDLC controller.
HBEN	TBOC.6	**Transmit HDLC & BOC Controller Enable.** 0 = source FDL data from the TLINK pin 1 = source FDL data from the on-board HDLC and BOC controller
BOC5	TBOC.5	**BOC Bit 5.** Last bit transmitted of the 6-bit codeword.
BOC4	TBOC.4	**BOC Bit 4.**
BOC3	TBOC.3	**BOC Bit 3.**
BOC2	TBOC.2	**BOC Bit 2.**
BOC1	TBOC.1	**BOC Bit 1.**
BOC0	TBOC.0	**BOC Bit 0.** First bit transmitted of the 6-bit codeword.

TFFR: TRANSMIT FDL FIFO REGISTER (Address = 08 Hex)

(MSB)							(LSB)
FDL7	FDL6	FDL5	FDL4	FDL3	FDL2	FDL1	FDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
FDL7	TFFR.7	**FDL Data Bit 7.** MSB of a HDLC packet data byte.
FDL6	TFFR.6	**FDL Data Bit 6.**
FDL5	TFFR.5	**FDL Data Bit 5.**
FDL4	TFFR.4	**FDL Data Bit 4.**
FDL3	TFFR.3	**FDL Data Bit 3.**
FDL2	TFFR.2	**FDL Data Bit 2.**
FDL1	TFFR.1	**FDL Data Bit 1.**
FDL0	TFFR.0	**FDL Data Bit 0.** LSB of a HDLC packet data byte.

12.2 Legacy FDL Support

In order to provide backward compatibility to the older DS2151 device, the DS2152 maintains the circuitry that existed in the previous generation of T1 single-chip transceivers. This section covers the circuitry and operation of this legacy functionality. In new applications, it is recommended that the HDLC controller and BOC controller described in Section 12.1 be used. On the receive side, it is possible to have both the new HDLC/BOC controller and the legacy hardware working at the same time. However, this is not possible on the transmit side since their can be only one source the of the FDL data internal to the device.

12.2.1 Receive Section

In the receive section, the recovered FDL bits or Fs bits are shifted bit-by-bit into the Receive FDL register (RFDL). Since the RFDL is 8 bits in length, it will fill up every 2ms (8 times 250µs). The DS2152 will signal an external microcontroller that the buffer has filled via the SR2.4 bit. If enabled via IMR2.4, the $\overline{INT}$ pin will toggle low indicating that the buffer has filled and needs to be read. The user has 2ms to read this data before it is lost. If the byte in the RFDL matches either of the bytes programmed into the RFDLM1 or RFDLM2 registers, then the SR2.2 bit will be set to a 1 and the $\overline{INT}$ pin will toggled low if enabled via IMR2.2. This feature allows an external microcontroller to ignore the FDL or Fs pattern until an important event occurs.

The DS2152 also contains a 0 destuffer which is controlled via the CCR2.0 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than five 1s should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.0, the DS2152 will automatically look for five 1s in a row, followed by a 0. If it finds such a pattern, it will automatically remove the 0. If the 0 destuffer sees six or more 1s in a row followed by a 0, the 0 is not removed. The CCR2.0 bit should always be set to a 1 when the DS2152 is extracting the FDL. More on how to use the DS2152 in FDL applications in this legacy support mode is covered in a separate application note.

RFDL: RECEIVE FDL REGISTER (Address = 28 Hex)

(MSB) **(LSB)**

RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
RFDL7	RFDL.7	**MSB of the Received FDL Code**
RFDL0	RFDL.0	**LSB of the Received FDL Code**

The Receive FDL Register (RFDL) reports the incoming Facility Data Link (FDL) or the incoming Fs bits. The LSB is received first.

RFDLM1: RECEIVE FDL MATCH REGISTER 1 (Address = 29 Hex)
RFDLM2: RECEIVE FDL MATCH REGISTER 2 (Address = 2A Hex)

(MSB)							(LSB)
RFDL7	RFDL6	RFDL5	RFDL4	RFDL3	RFDL2	RFDL1	RFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
RFDL7	RFDL.7	**MSB of the FDL Match Code**
RFDL0	RFDL.0	**LSB of the FDL Match Code**

When the byte in the Receive FDL Register matches either of the two Receive FDL Match Registers (RFDLM1/RFDLM2), RSR2.2 will be set to 1 and the $\overline{\text{INT}}$ will go active if enabled via IMR2.2.

12.2.2 Transmit Section

The transmit section will shift out into the T1 data stream either the FDL (in the ESF framing mode) or the Fs bits (in the D4 framing mode) contained in the Transmit FDL register (TFDL). When a new value is written to the TFDL, it will be multiplexed serially (LSB first) into the proper position in the outgoing T1 data stream. After the full 8 bits have been shifted out, the DS2152 will signal the host microcontroller that the buffer is empty and that more data is needed by setting the SR2.3 bit to 1. The $\overline{\text{INT}}$ will also toggle low if enabled via IMR2.3. The user has 2ms to update the TFDL with a new value. If the TFDL is not updated, the old value in the TFDL will be transmitted once again.

The DS2152 also contains a 0 stuffer which is controlled via the CCR2.4 bit. In both ANSI T1.403 and TR54016, communications on the FDL follows a subset of a LAPD protocol. The LAPD protocol states that no more than five 1s should be transmitted in a row so that the data does not resemble an opening or closing flag (01111110) or an abort signal (11111111). If enabled via CCR2.4, the DS2152 will automatically look for five 1s in a row. If it finds such a pattern, it will automatically insert a 0 after the five 1s. The CCR2.0 bit should always be set to a 1 when the DS2152 is inserting the FDL. More on how to use the DS2152 in FDL applications is covered in a separate application note.

TFDL: TRANSMIT FDL REGISTER (Address = 7E Hex)

(Also used to insert Fs framing pattern in D4 framing mode; see Section 12.3)

(MSB)							(LSB)
TFDL7	TFDL6	TFDL5	TFDL4	TFDL3	TFDL2	TFDL1	TFDL0

SYMBOL	POSITION	NAME AND DESCRIPTION
TFDL7	TFDL.7	**MSB of the FDL code to be transmitted.**
TFDL0	TFDL.0	**LSB of the FDL code to be transmitted.**

The Transmit FDL Register (TFDL) contains the Facility Data Link (FDL) information that is to be inserted on a byte basis into the outgoing T1 data stream. The LSB is transmitted first.

12.3 D4/SLC-96 OPERATION

In the D4 framing mode, the DS2152 uses the TFDL register to insert the Fs framing pattern. To allow the device to properly insert the Fs framing pattern, the TFDL register at address 7Eh must be programmed to 1Ch and the following bits must be programmed as shown:

TCR1.2 = 0 (source Fs data from the TFDL register)

CCR2.5 = 1 (allow the TFDL register to load on multiframe boundaries)

Since the SLC-96 message fields share the Fs-bit position, the user can access these message fields via the TFDL and RFDL registers. See the separate application note for a detailed description of how to implement an SLC-96 function.

13 PROGRAMMABLE IN-BAND CODE GENERATION AND DETECTION

The DS2152 can generate and detect a repeating bit pattern that is from 1 to 8 bits in length. To transmit a pattern, the user will load the pattern to be sent into the Transmit Code Definition (TCD) register and select the proper length of the pattern by setting the TC0 and TC1 bits in the In-Band Code Control (IBCC) register. Once this is accomplished, the pattern will be transmitted as long as the TLOOP control bit (CCR3.1) is enabled. Normally (unless the transmit formatter is programmed to not insert the F-bit position) the DS2152 will overwrite the repeating pattern once every 193 bits to allow the F-bit position to be sent. See Figure 16-11 for more details. As an example, if the user wished to transmit the standard "loop up" code for Channel Service Units which is a repeating pattern of ...10000100001... then 80h would be loaded into TDR and the length would set to 5 bits.

The DS2152 can detect two separate repeating patterns to allow for both a "loop up" code and a "loop down" code to be detected. The user will program the codes to be detected in the Receive Up Code Definition (RUPCD) register and the Receive Down Code Definition (RDNCD) register and the length of each pattern will be selected via the IBCC register. The DS2152 will detect repeating pattern codes in both framed and unframed circumstances with bit error rates as high as 10**-2. The code detector has a nominal integration period of 48ms. Hence, after about 48 ms of receiving either code, the proper status bit (LUP at SR1.7 and LDN at SR1.6) will be set to a 1. Normally codes are sent for a period of 5 seconds. It is recommend that the software poll the DS2152 every 100ms to 1000ms until 5 seconds has elapsed to insure that the code is continuously present.

IBCC: IN-BAND CODE CONTROL REGISTER (Address = 12 Hex)

(MSB)							(LSB)
TC1	TC0	RUP2	RUP1	RUP0	RDN2	RDN1	RDN0

SYMBOL	POSITION	NAME AND DESCRIPTION
TC1	IBCC.7	**Transmit Code Length Definition Bit 1.** See Table 13-1.
TC0	IBCC.6	**Transmit Code Length Definition Bit 0.** See Table 13-1.
RUP2	IBCC.5	**Receive Up Code Length Definition Bit 2.** See Table 13-2.
RUP1	IBCC.4	**Receive Up Code Length Definition Bit 1.** See Table 13-2.
RUP0	IBCC.3	**Receive Up Code Length Definition Bit 0.** See Table 13-2.
RDN2	IBCC.2	**Receive Down Code Length Definition Bit 2.** See Table 13-2.
RDN1	IBCC.1	**Receive Down Code Length Definition Bit 1.** See Table 13-2.
RDN0	IBCC.0	**Receive Down Code Length Definition Bit 0.** See Table 13-2.

Table 13-1. Transmit Code Length

TC1	TC0	LENGTH SELECTED (BITS)
0	0	5
0	1	6/3
1	0	7
1	1	8/4/2/1

Table 13-2. Receive Code Length

RUP2/ RDN2	RUP1/ RDN1	RUP0/ RDN0	LENGTH SELECTED (BITS)
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

TCD: TRANSMIT CODE DEFINITION REGISTER (Address = 13 Hex)

(MSB)							(LSB)
C7	C6	C5	C4	C3	C2	C1	C0

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	TCD.7	**Transmit Code Definition Bit 7.** First bit of the repeating pattern.
C6	TCD.6	**Transmit Code Definition Bit 6.**
C5	TCD.5	**Transmit Code Definition Bit 5.**
C4	TCD.4	**Transmit Code Definition Bit 4.**
C3	TCD.3	**Transmit Code Definition Bit 3.**
C2	TCD.2	**Transmit Code Definition Bit 2.** A Don’t Care if a 5-bit length is selected.
C1	TCD.1	**Transmit Code Definition Bit 1.** A Don’t Care if a 5 or 6-bit length is selected.
C0	TCD.0	**Transmit Code Definition Bit 0.** A Don’t Care if a 5, 6 or 7-bit length is selected.

RUPCD: RECEIVE UP CODE DEFINITION REGISTER (Address = 14 Hex)

(MSB)							(LSB)
C7	C6	C5	C4	C3	C2	C1	C0

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	RUPCD.7	**Receive Up Code Definition Bit 7.** First bit of the repeating pattern.
C6	RUPCD.6	**Receive Up Code Definition Bit 6.** A Don't Care if a 1-bit length is selected.
C5	RUPCD.5	**Receive Up Code Definition Bit 5.** A Don't Care if a 1 or 2-bit length is selected.
C4	RUPCD.4	**Receive Up Code Definition Bit 4.** A Don't Care if a 1 to 3-bit length is selected.
C3	RUPCD.3	**Receive Up Code Definition Bit 3.** A Don't Care if a 1 to 4-bit length is selected.
C2	RUPCD.2	**Receive Up Code Definition Bit 2.** A Don't Care if a 1 to 5-bit length is selected.
C1	RUPCD.1	**Receive Up Code Definition Bit 1.** A Don't Care if a 1 to 6-bit length is selected.
C0	RUPCD.0	**Receive Up Code Definition Bit 0.** A Don't Care if a 1 to 7-bit length is selected.

RDNCD: RECEIVE DOWN CODE DEFINITION REGISTER (Address = 15 Hex)

(MSB)							(LSB)
C7	C6	C5	C4	C3	C2	C1	C0

SYMBOL	POSITION	NAME AND DESCRIPTION
C7	RDNCD.7	**Receive Down Code Definition Bit 7.** First bit of the repeating pattern.
C6	RDNCD.6	**Receive Down Code Definition Bit 6.** A Don't Care if a 1-bit length is selected.
C5	RDNCD.5	**Receive Down Code Definition Bit 5.** A Don't Care if a 1 or 2-bit length is selected.
C4	RDNCD.4	**Receive Down Code Definition Bit 4.** A Don't Care if a 1 to 3-bit length is selected.
C3	RDNCD.3	**Receive Down Code Definition Bit 3.** A Don't Care if a 1 to 4-bit length is selected.
C2	RDNCD.2	**Receive Down Code Definition Bit 2.** A Don't Care if a 1 to 5-bit length is selected.
C1	RDNCD.1	**Receive Down Code Definition Bit 1.** A Don't Care if a 1 to 6-bit length is selected.
C0	RDNCD.0	**Receive Down Code Definition Bit 0.** A Don't Care if a 1 to 7-bit length is selected.

14 TRANSMIT TRANSPARENCY

Each of the 24 T1 channels in the transmit direction of the DS2152 can be either forced to be transparent or, in other words, can be forced to stop Bit 7 Stuffing and/or Robbed Signaling from overwriting the data in the channels. Transparency can be invoked on a channel-by-channel basis by properly setting the TTR1, TTR2, and TTR3 registers.

TTR1/TTR2/TTR3: TRANSMIT TRANSPARENCY REGISTER (Address = 39 to 3B Hex)

(MSB)							(LSB)	
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1	TTR1 (39)
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	TTR2 (3A)
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17	TTR3 (3B)

SYMBOL	POSITION	NAME AND DESCRIPTION
CH24	TTR3.7	**Transmit Transparency Registers.** 0 = this DS0 channel is not transparent
CH1	TTR1.0	1 = this DS0 channel is transparent

Each of the bit positions in the Transmit Transparency Registers (TTR1/TTR2/TTR3) represents a DS0 channel in the outgoing frame. When these bits are set to a 1, the corresponding channel is transparent (or clear). If a DS0 is programmed to be clear, no robbed-bit signaling will be inserted nor will the channel have Bit 7 stuffing performed. However, in the D4 framing mode, bit 2 will be overwritten by a 0 when a Yellow Alarm is transmitted. Also, the user has the option to prevent the TTR registers from determining which channels are to have Bit 7 stuffing performed. If the TCR2.0 and TCR1.3 bits are set to 1, then all 24 T1 channels will have Bit 7 stuffing performed on them regardless of how the TTR registers are programmed. In this manner, the TTR registers are only affecting which channels are to have robbed-bit signaling inserted into them. See Figure 16-11 for more details.

15 LINE INTERFACE FUNCTION

The line interface function in the DS2152 contains three sections: the receiver, which handles clock and data recovery; the transmitter, which waveshapes and drives the T1 line; and the jitter attenuator. Each of these three sections is controlled by the Line Interface Control Register (LICR), which is described below.

LICR: LINE INTERFACE CONTROL REGISTER (Address = 7C Hex)

(MSB)							(LSB)	
L2	L1	L0	EGL	JAS	JABDS	DJA	TPD	LICR

SYMBOL	POSITION	NAME AND DESCRIPTION
L2	LICR.7	**Line Build-Out Select Bit 2.** Sets the transmitter build out; see the Table 15-2.
L1	LICR.6	**Line Build-Out Select Bit 1.** Sets the transmitter build out; see the Table 15-2.
L0	LICR.5	**Line Build-Out Select Bit 0.** Sets the transmitter build out; see the Table 15-2.
EGL	LICR.4	**Receive Equalizer Gain Limit.** 0 = -36dB 1 = -30dB
JAS	LICR.3	**Jitter Attenuator Select.** 0 = place the jitter attenuator on the receive side 1 = place the jitter attenuator on the transmit side
JABDS	LICR.2	**Jitter Attenuator Buffer Depth Select** 0 = 128 bits 1 = 32 bits (use for delay sensitive applications)
DJA	LICR.1	**Disable Jitter Attenuator.** 0 = jitter attenuator enabled 1 = jitter attenuator disabled
TPD	LICR.0	**Transmit Power Down.** 0 = normal transmitter operation 1 = powers down the transmitter and tri-states the TTIP and TRING pins

15.1 Receive Clock and Data Recovery

The DS2152 contains a digital clock recovery system. See Figure 1-1 and Figure 15-1 for more details. The DS2152 couples to the receive T1 twisted pair via a 1:1 transformer. See Table 15-2 for transformer details. The 1.544MHz clock attached at the MCLK pin is internally multiplied by 16 via an internal PLL and fed to the clock recovery system. The clock recovery system uses the clock from the PLL circuit to form a 16 times oversampler which is used to recover the clock and data. This oversampling technique offers outstanding jitter tolerance (see Figure 15-2).

Normally, the clock that is output at the RCLKO pin is the recovered clock from the T1 AMI/B8ZS waveform presented at the RTIP and RRING inputs. When no AMI signal is present at RTIP and RRING, a Receive Carrier Loss (LRCL) condition will occur and the RCLKO will be sourced from the clock applied at the MCLK pin. If the jitter attenuator is either placed in the transmit path or is disabled, the RCLKO output can exhibit slightly shorter high cycles of the clock. This is due to the highly over-sampled digital clock recovery circuitry. If the jitter attenuator is placed in the receive path (as is the case in most applications), the jitter attenuator restores the RCLK to being close to 50% duty cycle. See the Receive AC Timing Characteristics in Section 18 for more details.

15.2 Transmit Waveshaping and Line Driving

The DS2152 uses a set of laser-trimmed delay lines along with a precision Digital-to-Analog Converter (DAC) to create the waveforms that are transmitted onto the T1 line. The waveforms created by the DS2152 meet the latest ANSI, AT&T, and ITU specifications. See Figure 15-3. The user will select which waveform is to be generated by properly programming the L2/L1/L0 bits in the Line Interface Control Register (LICR). The DS2152 can set up in a number of various configurations depending on the application. See Table 15-1 and Figure 15-1.

Table 15-1. Line Build-Out Select in LICR

L2	L1	L0	LINE BUILD-OUT	APPLICATION
0	0	0	0 to 133ft/0dB	DSX-1/CSU
0	0	1	133ft to 266ft	DSX-1
0	1	0	266ft to 399ft	DSX-1
0	1	1	399ft to 533ft	DSX-1
1	0	0	533ft to 655ft	DSX-1
1	0	1	-7.5dB	CSU
1	1	0	-15dB	CSU
1	1	1	-22.5dB	CSU

Due to the nature of the design of the transmitter in the DS2152, very little jitter (less than $0.005UI_{P-P}$ broadband from 10Hz to 100kHz) is added to the jitter present on TCLKI. Also, the waveforms that they create are independent of the duty cycle of TCLK. The transmitter in the DS2152 couples to the T1 transmit twisted pair via a 1:1.15 or 1:1.36 step-up transformer as shown in Figure 15-1. For the devices to create the proper waveforms, this transformer used must meet the specifications listed in Table 15-2.

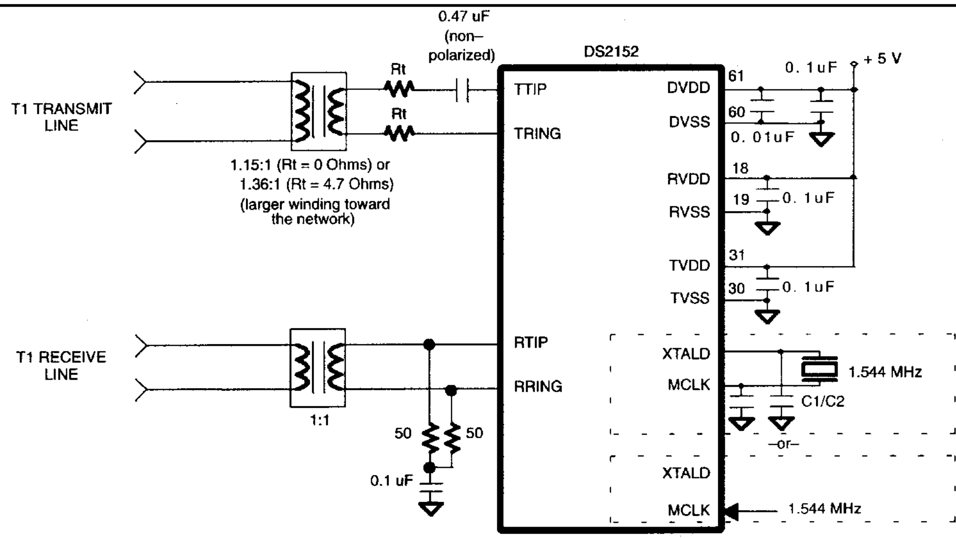
Table 15-2. Transformer Specifications

SPECIFICATION	RECOMMENDED VALUE
Turns Ratio	1:1 (receive) and 1:1.15 or 1:1.36 (transmit) ±5%
Primary Inductance	600µH minimum
Leakage Inductance	1.0µH maximum
Intertwining Capacitance	40pF maximum
DC Resistance	1.2Ω maximum

15.3 Jitter Attenuator

The DS2152 contains an on-board jitter attenuator that can be set to a depth of either 32 or 128 bits via the JABDS bit in the Line Interface Control Register (LICR). The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay sensitive applications. The characteristics of the attenuation are shown in Figure 15-4. The jitter attenuator can be placed in either the receive path or the transmit path by appropriately setting or clearing the JAS bit in the LICR. Also, the jitter attenuator can be disabled (in effect, removed) by setting the DJA bit in the LICR. In order for the jitter attenuator to operate properly, a 1.544MHz clock (±50ppm) must be applied at the MCLK pin or a crystal with similar characteristics must be applied across the MCLK and XTALD pins. If a crystal is applied across the MCLK and XTALD pins, then capacitors should be placed from each leg of the crystal to the local ground plane as shown in Figure 15-1. On-board circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLKI pin to create a smooth jitter-free clock that is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLKI pin if the jitter attenuator is placed on the transmit side. If the incoming jitter exceeds either $120UI_{P-P}$ (buffer depth is 128 bits) or $28UI_{P-P}$ (buffer depth is 32 bits), then the DS2152 will divide the internal nominal 24.704MHz clock by either 15 or 17 instead of the normal 16 to keep the buffer from overflowing. When the device divides by either 15 or 17, it also sets the Jitter Attenuator Limit Trip (JALT) bit in the Receive Information Register (RIR3.5).

Figure 15-1. External Analog Connections



NOTE 1: RESISTOR VALUES ARE ±1%.
NOTE 2: THE R_T RESISTORS ARE USED TO PROTECT THE DEVICE FROM OVERVOLTAGE.
NOTE 3: SEE THE SEPARATE APPLICATION NOTE FOR DETAILS ON HOW TO CONSTRUCT A PROTECTED INTERFACE.
NOTE 4: EITHER A CRYSTAL CAN BE APPLIED ACROSS THE MCLK AND XTALD PINS OR A TTL LEVEL CLOCK CAN BE APPLIED TO JUST MCLK.
NOTE 5: C1 AND C2 SHOULD BE 5PF LOWER THAN 2 TIMES THE NOMINAL LOADING CAPACITANCE OF THE CRYSTAL TO ADJUST FOR THE INPUT CAPACITANCE OF THE DS2152.

Figure 15-2. Jitter Tolerance

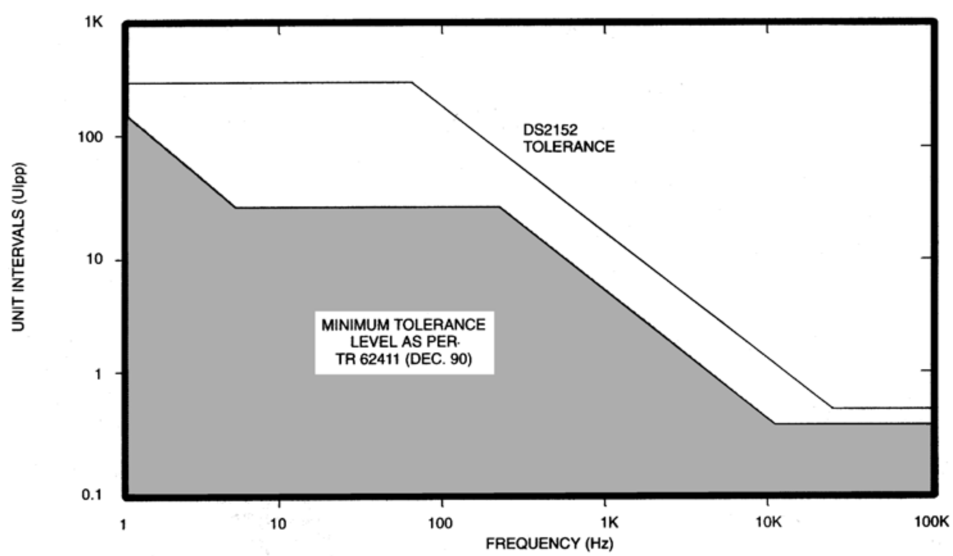


Figure 15-3. Transmit Waveform Template

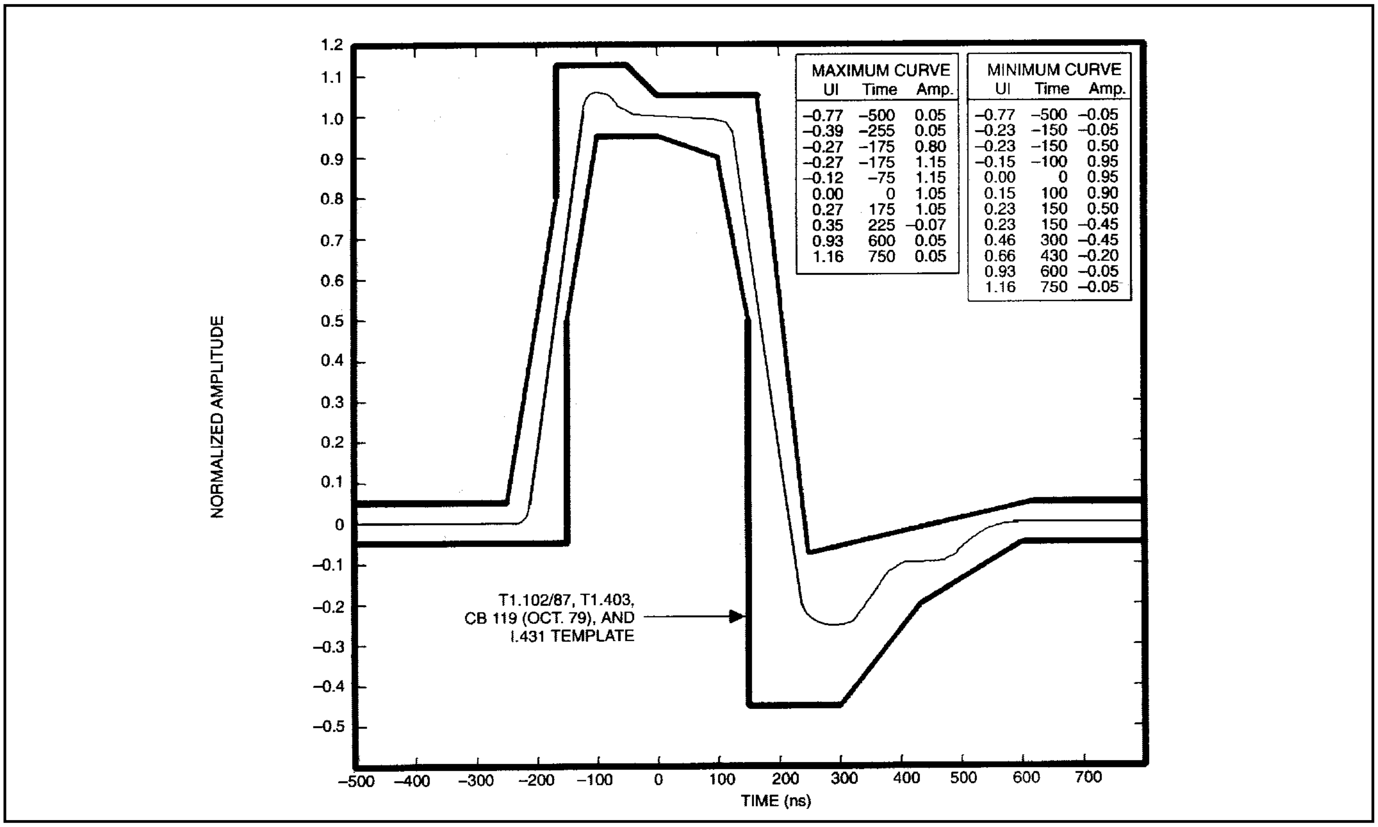
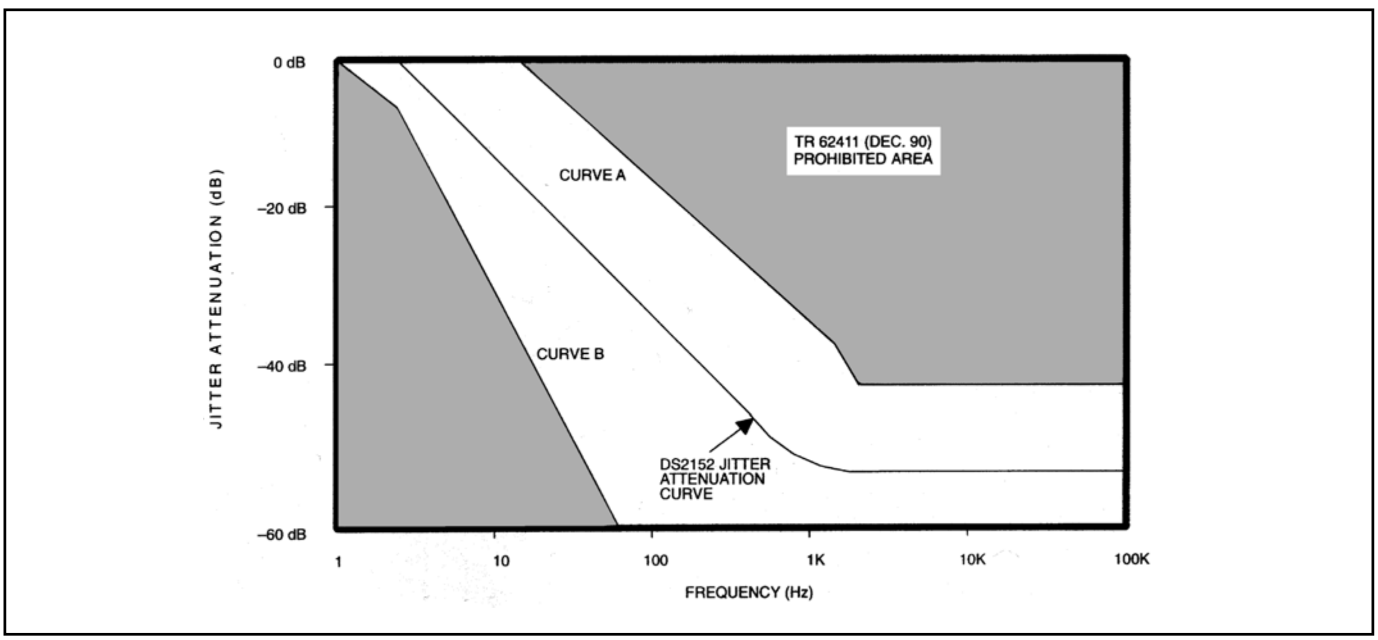
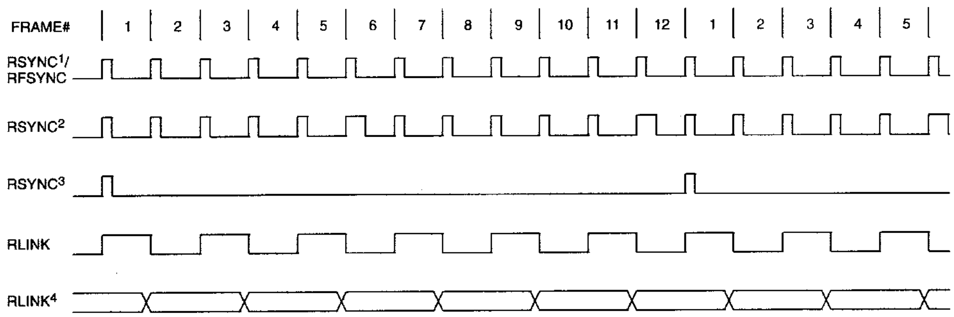


Figure 15-4. Jitter Attenuation



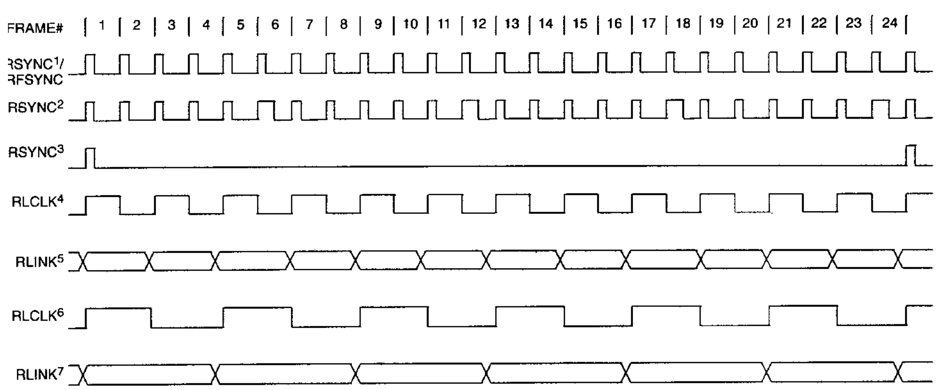
16 TIMING DIAGRAMS

Figure 16-1. Receive Side D4 Timing



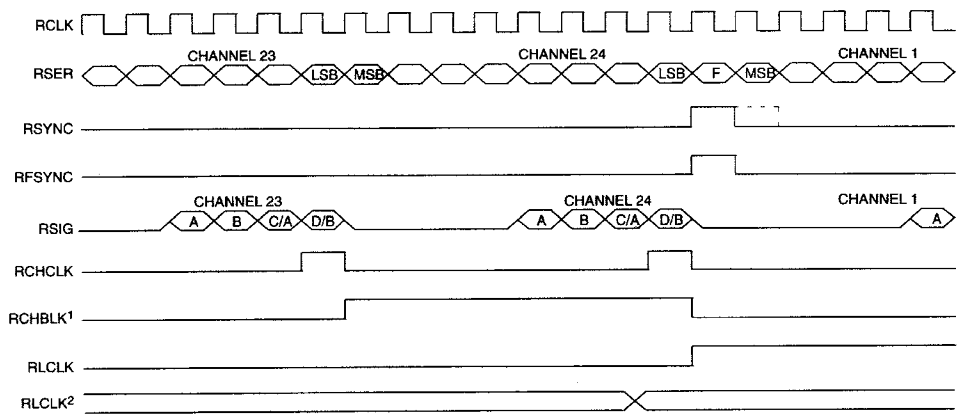
NOTE 1: RSYNC IN THE FRAME MODE (RCR2.4 = 0) AND DOUBLE-WIDE FRAME SYNC IS NOT ENABLED (RCR2.5 = 0).
NOTE 2: RSYNC IN THE FRAME MODE (RCR2.4 = 0) AND DOUBLE-WIDE FRAME SYNC IS ENABLED (RCR2.5 = 1).
NOTE 3: RSYNC IN THE MULTIFRAME MODE (RCR2.4 = 1).
NOTE 4: RLINK DATA (FS BITS) IS UPDATED 1 BIT PRIOR TO EVEN FRAMES AND HELD FOR TWO FRAMES.
NOTE 5: RLINK AND RLCLK ARE NOT SYNCHRONOUS WITH RSYNC WHEN THE RECEIVE SIDE ELASTIC STORE IS ENABLED.

Figure 16-2. Receive Side Boundary Timing (with Elastic Store Disabled)



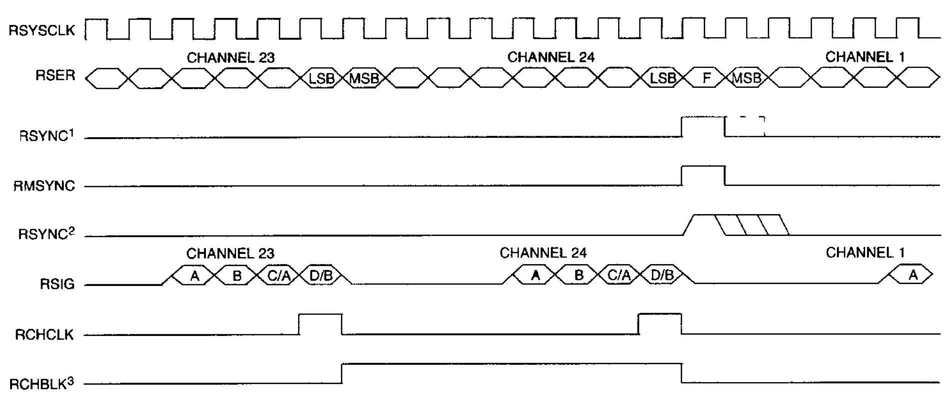
NOTE 1: RSYNC IN THE FRAME MODE (RCR2.4 = 0) AND DOUBLE-WIDE FRAME SYNC IS NOT ENABLED (RCR2.5 = 0).
NOTE 2: RSYNC IN THE FRAME MODE (RCR2.4 = 0) AND DOUBLE-WIDE FRAME SYNC IS ENABLED (RCR2.5 = 1).
NOTE 3: RSYNC IN THE MULTIFRAME MODE (RCR2.4 = 1).
NOTE 4: ZBTSI MODE DISABLED (RCR2.6 = 0).
NOTE 5: RLINK DATA (FDL BITS) IS UPDATED 1 BIT-TIME BEFORE ODD FRAMES AND HELD FOR TWO FRAMES.
NOTE 6: ZBTSI MODE IS ENABLED (RCR2.6 = 1).
NOTE 7: RLINK DATA (Z BITS) IS UPDATED 1 BIT-TIME BEFORE ODD FRAMES AND HELD FOR FOUR FRAMES.
NOTE 8: RLINK AND RLCLK ARE NOT SYNCHRONOUS WITH RSYNC WHEN THE RECEIVE SIDE ELASTIC STORE IS ENABLED.

Figure 16-3. Receive Side Boundary Timing (with Elastic Store Disabled)



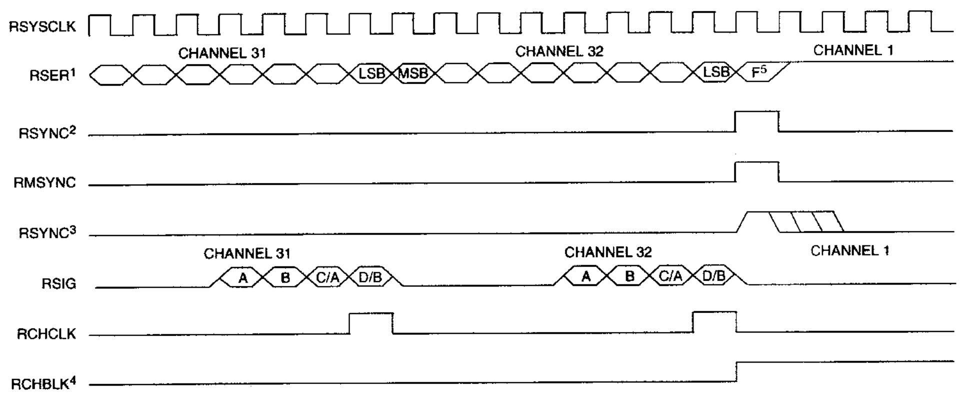
NOTE 1: RCHBLK IS PROGRAMMED TO BLOCK CHANNEL 24.
NOTE 2: SHOWN IS RLINK/RLCLK IN THE ESF FRAMING MODE.

Figure 16-4. Receive Side 1.544MHz Boundary Timing (with Elastic Store Enabled)



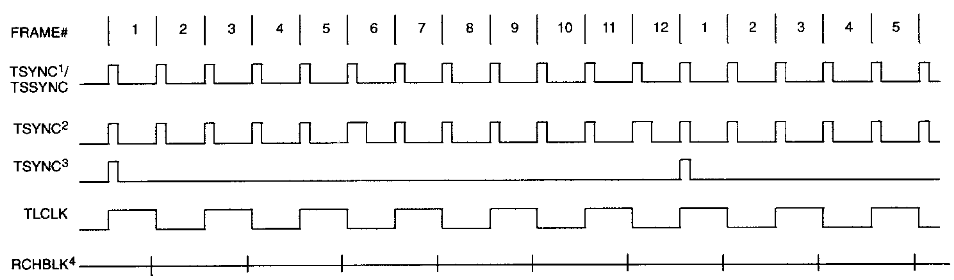
NOTE 1: RSYNC IS IN THE OUTPUT MODE (RCR2.3 = 0).
NOTE 2: RSYNC IS IN THE INPUT MODE (RCR2.3 = 1).
NOTE 3: RCHBLK IS PROGRAMMED TO BLOCK CHANNEL 24.

Figure 16-5. Receive Side 2.048MHz Boundary Timing (with Elastic Store Enabled)



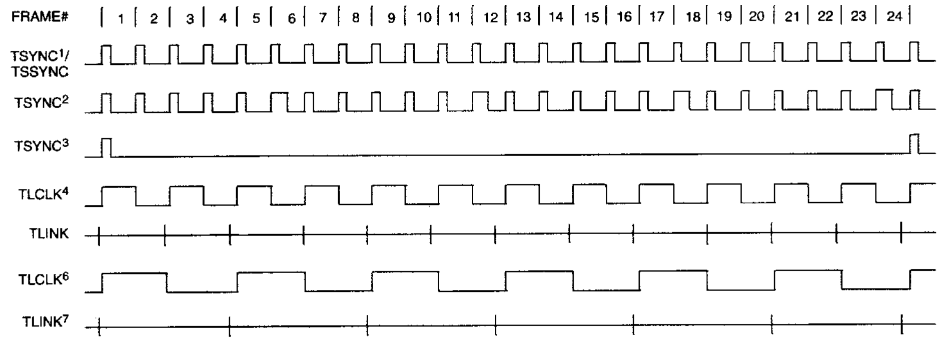
NOTE 1: RSER DATA IN CHANNELS 1, 5, 9, 13, 17, 21, 25, AND 29 ARE FORCED TO 1.
NOTE 2: RSYNC IS IN THE OUTPUT MODE (RCR2.3 = 0).
NOTE 3: RSYNC IS IN THE INPUT MODE (RCR2.3 = 1).
NOTE 4: RCHBLK IS FORCED TO 1 IN THE SAME CHANNELS AS RSER (SEE NOTE 1).
NOTE 5: THE F-BIT POSITION IS PASSED THROUGH THE RECEIVE SIDE ELASTIC STORE.
NOTE 6: RCHCLK DOES NOT TRANSITION HIGH IN THE CHANNELS IN WHICH THE RSER DATA IS FORCED TO 1 (SEE NOTE 1).

Figure 16-6. Transmit Side D4 Timing



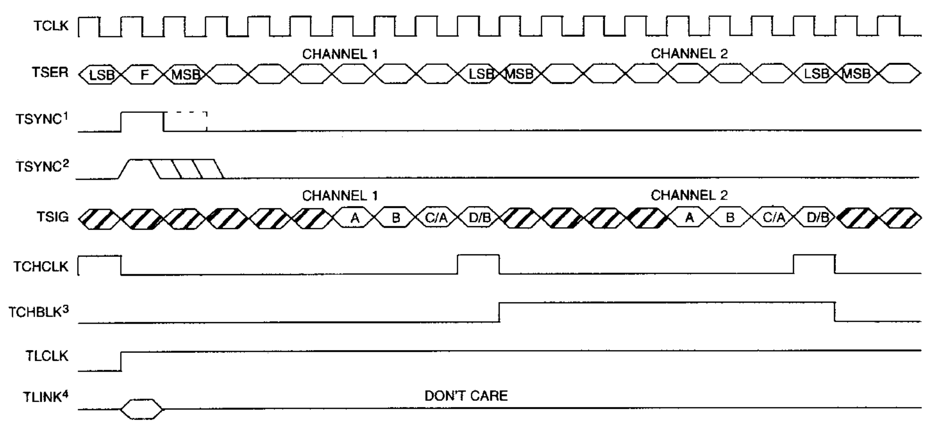
NOTE 1: TSYNC IN THE FRAME MODE (TCR2.3 = 0) AND DOUBLE-WIDE FRAME SYNC IS NOT ENABLED (TCR2.4 = 0).
NOTE 2: TSYNC IN THE FRAME MODE (TCR2.3 = 0) AND DOUBLE-WIDE FRAME SYNC IS ENABLED (TCR2.4 = 1).
NOTE 3: TSYNC IN THE MULTIFRAME MODE (TCR2.3 = 1).
NOTE 4: TLINK DATA (FS BITS) IS SAMPLED DURING THE F-BIT POSITION OF EVEN FRAMES FOR INSERTION INTO THE OUTGOING T1 STREAM WHEN ENABLED VIA TCR1.2.
NOTE 5: TLINK AND TLCLK ARE NOT SYNCHRONOUS WITH TSSYNC.

Figure 16-7. Transmit Side Timing



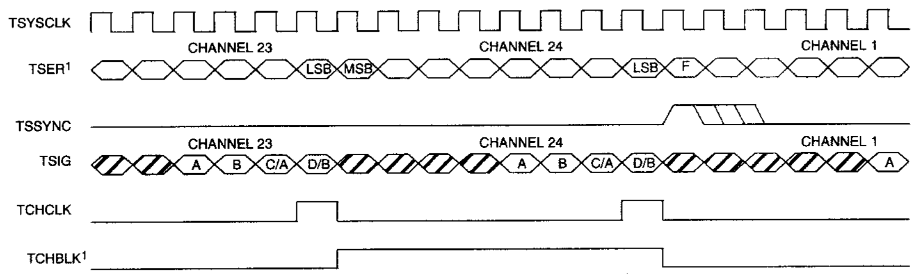
NOTE 1: TSYNC IN THE FRAME MODE (TCR2.3 = 0) AND DOUBLE-WIDE FRAME SYNC IS NOT ENABLED (TCR2.4 = 0).
NOTE 2: TSYNC IN THE FRAME MODE (TCR2.3=0) AND DOUBLE-WIDE FRAME SYNC IS ENABLED (TCR2.4 = 1).
NOTE 3: TSYNC IN THE MULTIFRAME MODE (TCR2.3 = 1).
NOTE 4: ZBTSI MODE DISABLED (TCR2.5 = 0).
NOTE 5: TLINK DATA (FDL BITS) IS SAMPLED DURING THE F-BIT TIME OF ODD FRAME AND INSERTED INTO THE OUTGOING T1 STREAM IF ENABLED VIA TCR1.2.
NOTE 6: ZBTSI MODE IS ENABLED (TCR2.5 = 1).
NOTE 7: TLINK DATA (Z BITS) IS SAMPLED DURING THE F-BIT TIME OF FRAMES 1, 5, 9, 13, 17, AND 21 AND INSERTED INTO THE OUTGOING STREAM IF ENABLED VIA TCR1.2.
NOTE 8: TLINK AND TLCLK ARE NOT SYNCHRONOUS WITH TSSYNC.

Figure 16-8. Transmit Side Boundary Timing



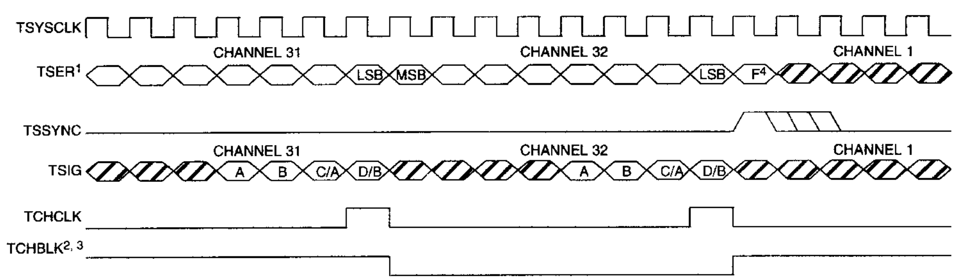
NOTE 1: TSYNC IS IN THE OUTPUT MODE (TCR2.2 = 1).
NOTE 2: TSYNC IS IN THE INPUT MODE (TCR2.2 = 0).
NOTE 3: TCHBLK IS PROGRAMMED TO BLOCK CHANNEL 2.
NOTE 4: SHOWN IS TLINK/TLCLK IN THE ESF FRAMING MODE.

Figure 16-9. Transmit Side 1.544MHz Boundary Timing (with Elastic Store Enabled)



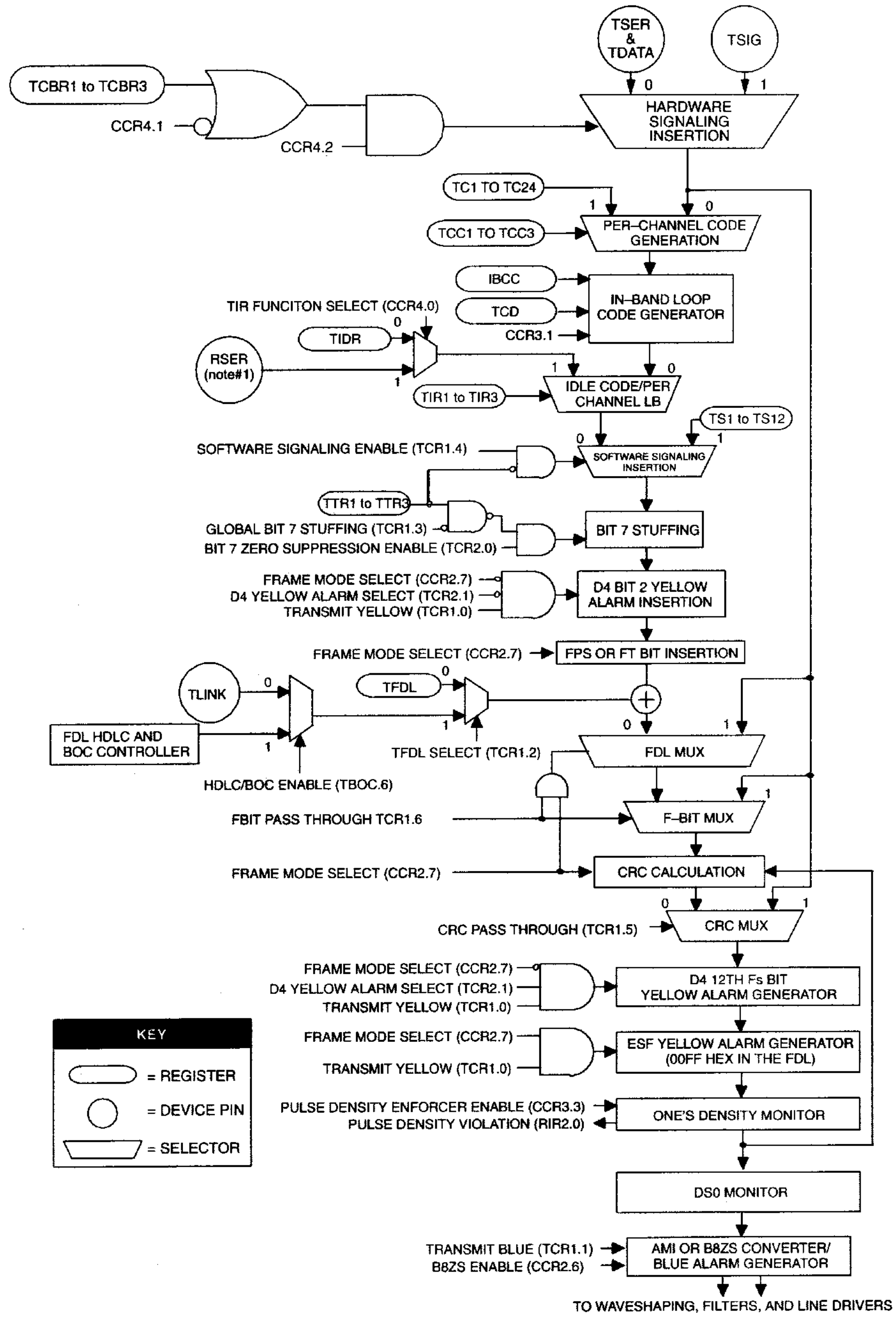
NOTE 1: TCHBLK IS PROGRAMMED TO BLOCK CHANNEL 24 (IF THE TPCSI BIT IS SET, THEN THE SIGNALING DATA AT TSIG WILL BE IGNORED DURING CHANNEL 24).

Figure 16-10. Transmit Side 2.048MHz Boundary Timing (with Elastic Store Enabled)



NOTE 1: TSER DATA IN CHANNELS 1, 5, 9, 13, 17, 21, 25, AND 29 IS IGNORED.
NOTE 2: TCHBLK IS PROGRAMMED TO BLOCK CHANNEL 31 (IF THE TPCSI BIT IS SET, THEN THE SIGNALING DATA AT TSIG IS IGNORED).
NOTE 3: TCHBLK IS FORCED TO 1 IN THE SAME CHANNELS WHERE TSER IS IGNORED (SEE NOTE 1).
NOTE 4: THE F-BIT POSITION FOR THE T1 FRAME IS SAMPLED AND PASSED THROUGH THE TRANSMIT SIDE ELASTIC STORE (NORMALLY THE TRANSMIT SIDE FORMATTER OVERWRITES THE F-BIT POSITION UNLESS THE FORMATTER IS PROGRAMMED TO PASS-THROUGH THE F-BIT POSITION).
NOTE 5: TCHCLK DOES NOT TRANSITION HIGH IN THE CHANNEL IN WHICH THE DATA AT TSER IS IGNORED (SEE NOTE 1).

Figure 16-11. Transmit Data Flow



NOTE 1: TCLK SHOULD BE TIED TO RCLK AND TSYNC SHOULD BE TIED TO RFSYNC FOR DATA TO BE PROPERLY SOURCED FROM RSER.

17 DC CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground…………………………………………..-1.0V to +7.0V
Operating Temperature Range
Commercial……………………………………………………………………0°C to +70°C
Industrial……………………………………………………………………….-40°C to +85°C
Storage Temperature……………………………………………………………….-55°C to +125°C
Soldering Temperature……………………………………………See IPC/JEDEC STD-020 Specification

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Table 17-1. Recommended DC Operating Conditions

(T_A = 0°C to +70°C for DS2152L, T_A = -40°C to +85°C for DS2152LN.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Logic 1	V_{IH}	2.0		V_{DD} + 0.3	V	
Logic 0	V_{IL}	-0.3		+0.8	V	
Supply	V_{DD}	4.75		5.25	V	1

Table 17-2. Capacitance

(T_A = +25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}		5		pF	
Output Capacitance	C_{OUT}		7		pF	

Table 17-3. DC Characteristics

(V_{DD} = 5V ±5%, T_A = 0°C to +70°C for DS2152L, T_A = -40°C to +85°C for DS2152LN.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current at 5V	I_{DD}		75		mA	2
Input Leakage	I_{IL}	-1.0		+1.0	µA	3
Output Leakage	I_{LO}			1.0	µA	4
Output Current (2.4V)	I_{OH}	-1.0			mA	
Output Current (0.4V)	I_{OL}	+4.0			mA	

NOTES:

1. Applies to RVDD, TVDD, and DVDD.
2. TCLK = RCLK = TSYSCLK = RSYSCLK = 1.544MHz; outputs open circuited.
3. 0V < V_{IN} < V_{DD}.
4. Applied to $\overline{INT}$ when tri-stated.

18 AC CHARACTERISTICS

Table 18-1. AC Characteristics—Multiplexed Parallel Port (MUX = 1)

(V_{DD} = 5V ±5%, T_A = 0°C to +70°C for DS2152L, T_A = -40°C to +85°C for DS2152LN.)
(See Figure 18-1, Figure 18-2, and Figure 18-3.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Cycle Time	t_{CYC}	200			ns	
Pulse Width, DS Low or $\overline{RD}$ High	PW_{EL}	100			ns	
Pulse Width, DS High or $\overline{RD}$ Low	PW_{EH}	100			ns	
Input Rise/Fall Times	t_R, t_F			20	ns	
R/$\overline{W}$ Hold Time	t_{RWH}	10			ns	
R/$\overline{W}$ Setup Time Before DS High	t_{RWS}	50			ns	
$\overline{CS}$ Setup Time Before DS, $\overline{WR}$ or $\overline{RD}$ active	t_{CS}	20			ns	
$\overline{CS}$ Hold Time	t_{CH}	0			ns	
Read Data Hold Time	t_{DHR}	10		50	ns	
Write Data Hold Time	t_{DHW}	0			ns	
Muxed Address Valid to AS or ALE Fall	t_{ASL}	15			ns	
Muxed Address Hold Time	t_{AHL}	10			ns	
Delay Time, DS, $\overline{WR}$ or $\overline{RD}$ to AS or ALE Rise	t_{ASD}	20			ns	
Pulse Width AS or ALE High	PW_{ASH}	30			ns	
Delay Time, AS or ALE to DS, $\overline{WR}$ or $\overline{RD}$	t_{ASED}	10			ns	
Output Data Delay Time from DS or $\overline{RD}$	t_{DDR}	20		80	ns	
Data Setup Time	t_{DSW}	50			ns	

Figure 18-1. Intel Bus Read AC Timing (BTS = 0/MUX = 1)

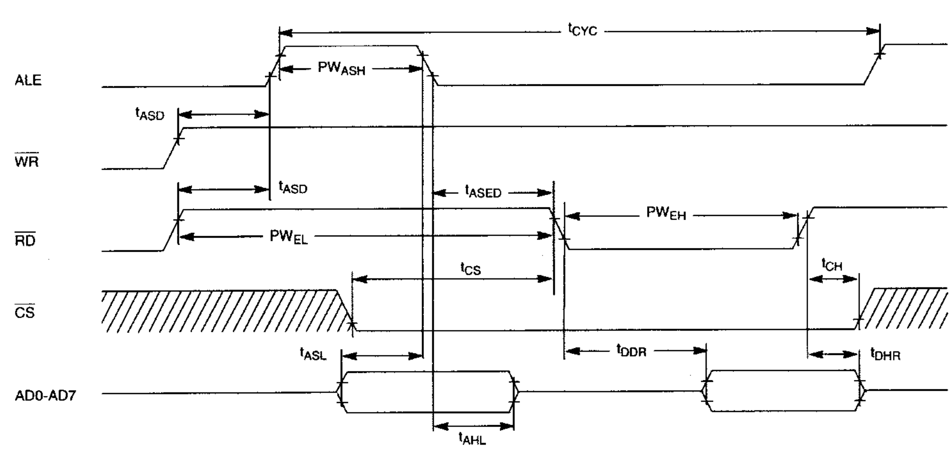


Figure 18-2. Intel Bus Write AC Timing (BTS = 0/MUX = 1)

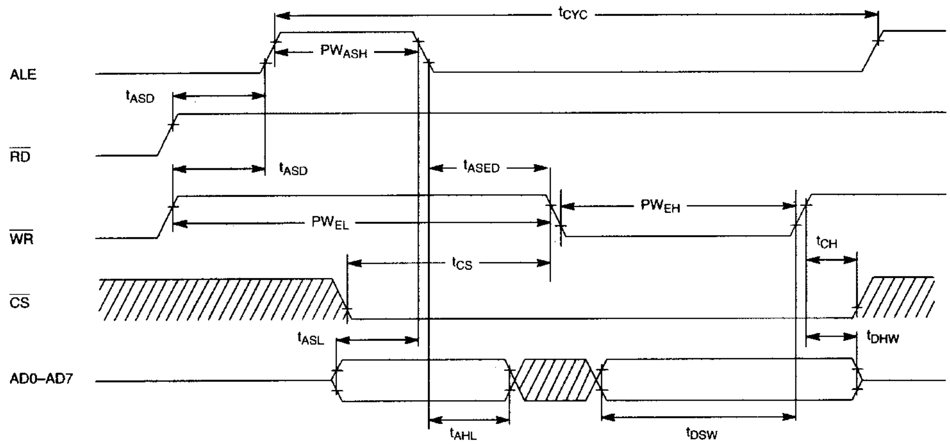


Figure 18-3. Motorola Bus AC Timing (BTS = 1/MUX = 1)

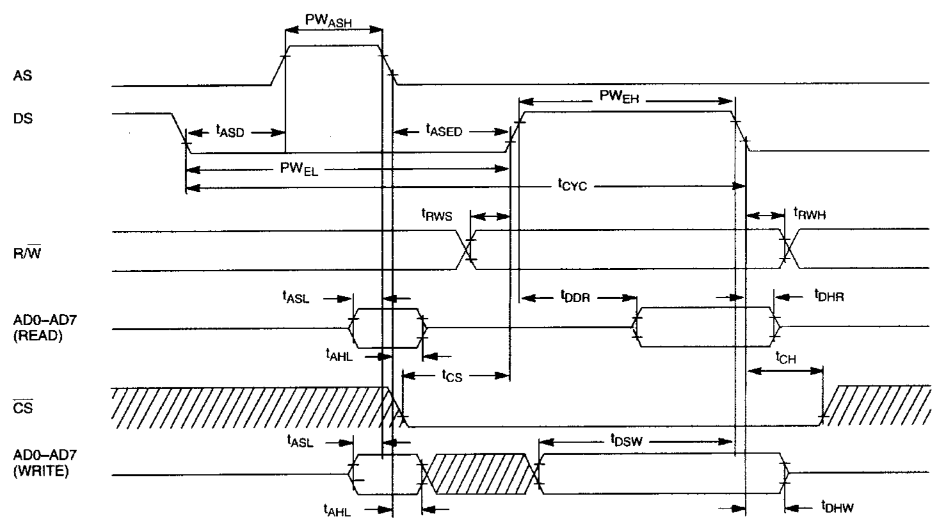


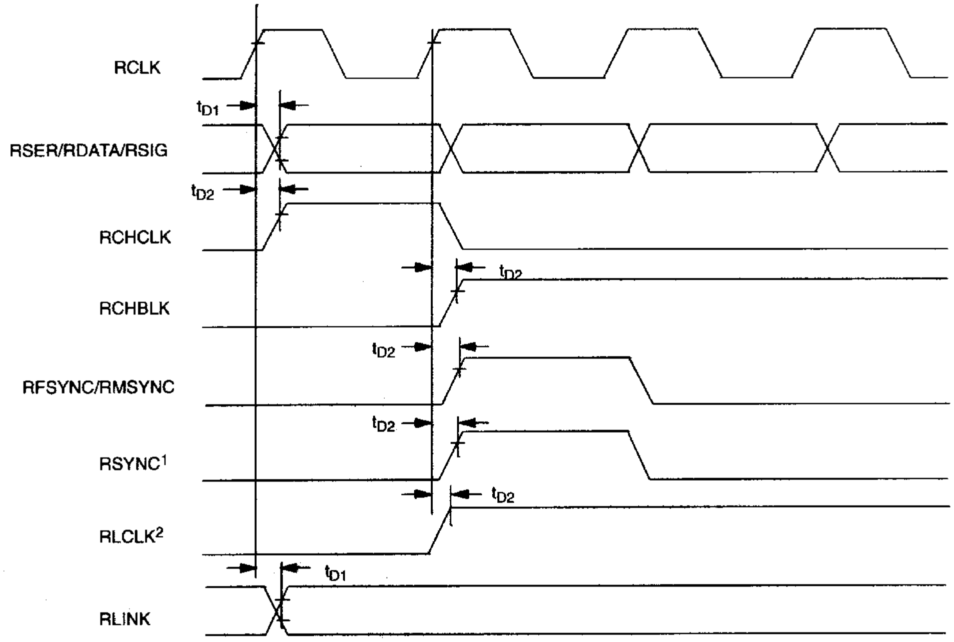
Table 18-2. AC Characteristics—Receive Side

(V_{DD} = 5V ±5%, T_A = 0°C to +70°C for DS2152L, T_A = -40°C to +85°C for DS2152LN.)
(See Figure 18-4, Figure 18-5, and Figure 18-6.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
RCLKO Period	t_{LP}		648		ns	
RCLKO Pulse Width	t_{LH}	250	324		ns	1
	t_{LL}	250	324		ns	1
RCLKO Pulse Width	t_{LH}	200	324		ns	2
	t_{CL}	200	324		ns	2
RCLKI Period	t_{CP}		648		ns	
RCLKI Pulse Width	t_{CH}	75			ns	
	t_{CL}	75			ns	
RSYSCLK Period	t_{SP}	122	648		ns	3
	t_{SP}	122	488		ns	4
RSYSCLK Pulse Width	t_{SH}	50			ns	
	t_{SL}	50			ns	
RSYNC Setup to RSYSCLK Falling	t_{SU}	20		t_{SH}-5	ns	
RSYNC Pulse Width	t_{PW}	50			ns	
RPOSI/RNEGI Setup to RCLKI Falling	t_{SU}	20			ns	
RPOSI/RNEGI Hold From RCLKI Falling	t_{HD}	20			ns	
RSYSCLK/RCLKI Rise and Fall Times	t_R, t_F			25	ns	
Delay RCLKO to RPOSO, RNEGO Valid	t_{DD}			50	ns	
Delay RCLK to RSER, RDATA, RSIG, RLINK Valid	t_{D1}			50	ns	
Delay RCLK to RCHCLK, RSYNC, RCHBLK, RFSYNC, RLCLK	t_{D2}			50	ns	
Delay RSYSCLK to RSER, RSIG Valid	t_{D3}			50	ns	
Delay RSYSCLK to RCHCLK, RCHBLK, RMSYNC, RSYNC	t_{D4}			50	ns	

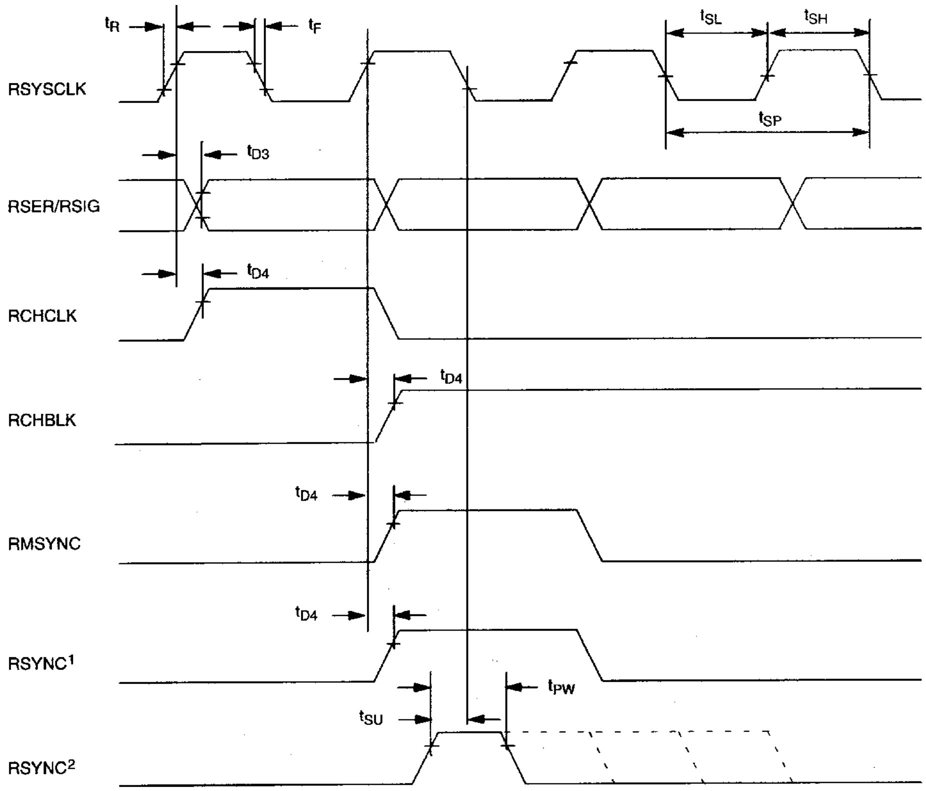
NOTES:
1) Jitter attenuator enabled in the receive path.
2) Jitter attenuator disabled or enabled in the transmit path.
3) RSYSCLK = 1.544MHz.
4) RSYSCLK = 2.048MHz.

Figure 18-4. Receive Side AC Timing



NOTE 1: RSYNC IS IN THE OUTPUT MODE (RCR2.3 = 0).
NOTE 2: SHOWN IS RLINK/RLCLK IN THE ESF FRAMING MODE.
NOTE 3: NO RELATIONSHIP BETWEEN RCHCLK AND RCHBLK AND THE OTHER SIGNALS IS IMPLIED.

Figure 18-5. Receive System Side AC Timing



NOTE 1: RSYNC IS IN THE OUTPUT MODE (RCR2.3 = 0).
NOTE 2: RSYNC IS IN THE INPUT MODE (RCR2.3 = 1).

Figure 18-6. Receive Line Interface AC Timing

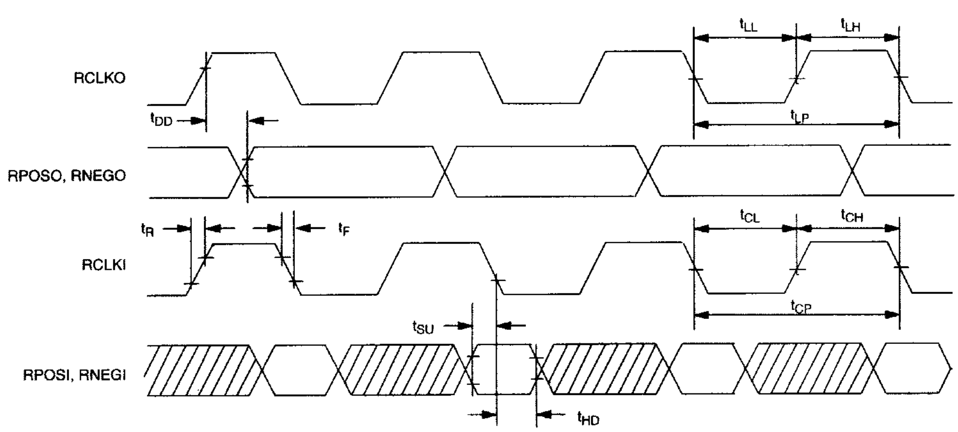


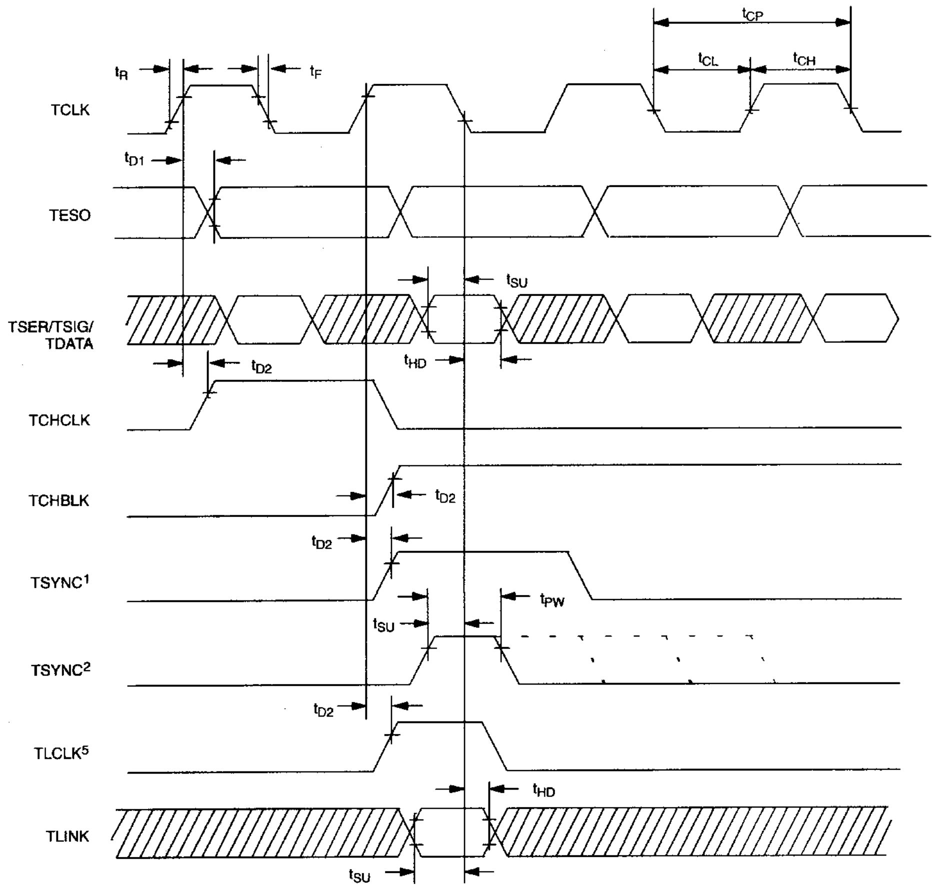
Table 18-3. AC Characteristics—Transmit Side

(V_{DD} = 5V ±5%, T_A = 0°C to +70°C for DS2152L, T_A = -40°C to +85°C for DS2152LN.)
(See Figure 18-7, Figure 18-8, and Figure 18-9.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
TCLK Period	t_{CP}		648		ns	
TCLK Pulse Width	t_{CH}	75			ns	
	t_{CL}	75			ns	
TCLKI Period	t_{LP}		648		ns	
TCLKI Pulse Width	t_{LH}	75			ns	
	t_{LL}	75			ns	
TSYSCLK Period	t_{SP}	122	648		ns	1
	t_{SP}	122	448		ns	2
TSYSCLK Pulse Width	t_{SH}	50			ns	
	t_{SL}	50			ns	
TSYNC or TSSYNC Setup to TCLK or TSYSCLK Falling	t_{SU}	20		t_{CH}-5 or t_{SH}-5	ns	
TSYNC or TSSYNC Pulse Width	t_{PW}	50			ns	
TSER, TSIG, TDATA, TLINK, TPOSI, TNEGI Setup to TCLK, TSYSCLK, TCLKI Falling	t_{SU}	20			ns	
TSER, TSIG, TDATA, TLINK, TPOSI, TNEGI Hold from TCLK, TSYSCLK, TCLKI Falling	t_{HD}	20			ns	
TCLK, TCLKI, or TSYSCLK Rise and Fall Times	t_R, t_F			25	ns	
Delay TCLKO to TPOSO, TNEGO Valid	t_{DD}			50	ns	
Delay TCLK to TESO Valid	t_{D1}			50	ns	
Delay TCLK to TCHBLK, TCHBLK, TSYNC, TLCLK	t_{D2}			50	ns	
Delay TSYSCLK to TCHCLK, TCHBLK	t_{D3}			75	ns	

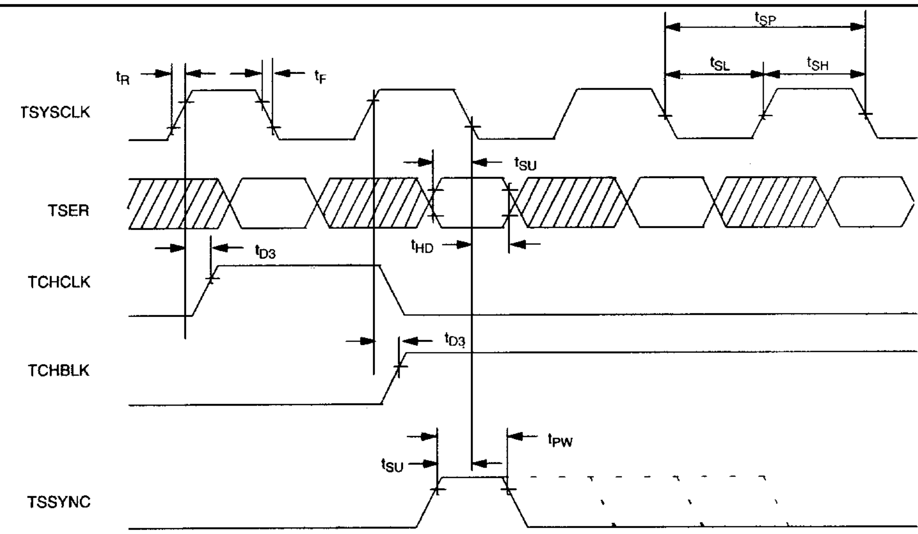
NOTES:
1) TSYSCLK = 1.544MHz.
2) TSYSCLK = 2.048MHz.

Figure 18-7. Transmit Side AC Timing



NOTE 1: TSYNC IS IN THE OUTPUT MODE (TCR2.2 = 1).
NOTE 2: TSYNC IS IN THE INPUT MODE (TCR2.2 = 0).
NOTE 3: TSER IS SAMPLED ON THE FALLING EDGE OF TCLK WHEN THE TRANSMIT SIDE ELASTIC STORE IS DISABLED.
NOTE 4: TCHCLK AND TCHBLK ARE SYNCHRONOUS WITH TCLK WHEN THE TRANSMIT SIDE ELASTIC STORE IS DISABLED.
NOTE 5: TLINK IS ONLY SAMPLED DURING F-BIT LOCATIONS.
NOTE 6: NO RELATIONSHIP BETWEEN TCHCLK AND TCHBLK AND THE OTHER SIGNALS IS IMPLIED.

Figure 18-8. Transmit System Side AC Timing



NOTE 1: TSER IS ONLY SAMPLED ON THE FALLING EDGE OF TSYSCLK WHEN THE TRANSMIT SIDE ELASTIC STORE IS ENABLED.
NOTE 2: TCHCLK AND TCHBLK ARE SYNCHRONOUS WITH TSYSCLK WHEN THE TRANSMIT SIDE ELASTIC STORE IS ENABLED.

Figure 18-9. Transmit Line Interface Side AC Timing

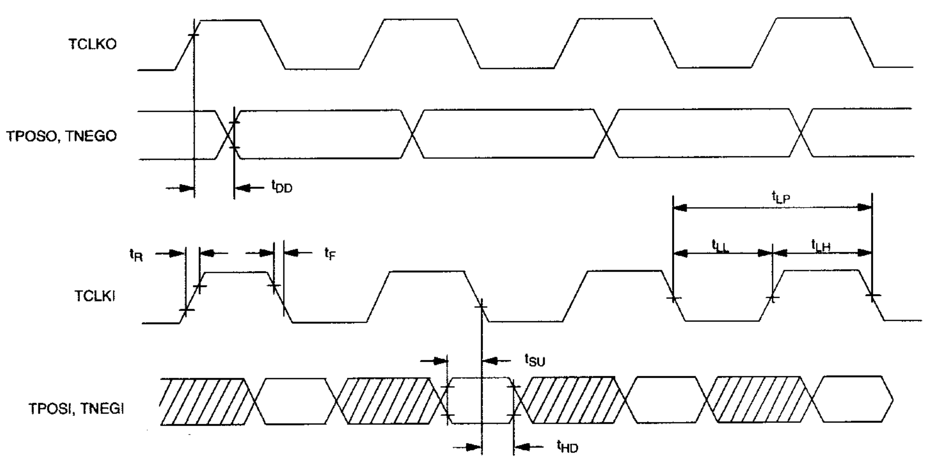


Table 18-4. AC Characteristics—Nonmultiplexed Parallel Port (MUX = 0)

(V_{DD} = 5V ±5%, T_A = 0°C to +70°C for DS2152L, T_A = -40°C to +85°C for DS2152LN.)
(See Figure 18-10, Figure 18-11, Figure 18-12, and Figure 18-13.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Setup Time for A0 to A7 Valid to $\overline{CS}$ Active	t1	0			ns	
Setup Time for $\overline{CS}$ Active to Either $\overline{RD}$, $\overline{WR}$, or $\overline{DS}$ Active	t2	0			ns	
Delay Time from Either $\overline{RD}$ or $\overline{DS}$ Active to Data Valid	t3			75	ns	
Hold Time from Either $\overline{RD}$, $\overline{WR}$, or $\overline{DS}$ Inactive to $\overline{CS}$ Inactive	t4	0			ns	
Hold Time from $\overline{CS}$ Inactive to Data Bus Tri-State	t5	5		20	ns	
Wait Time from Either $\overline{WR}$ or $\overline{DS}$ Active to Latch Data	t6	75			ns	
Data Setup Time to Either $\overline{WR}$ or $\overline{DS}$ Inactive	t7	10			ns	
Data Hold Time to Either $\overline{WR}$ or $\overline{DS}$ Inactive	t8	0			ns	
Address Hold from Either $\overline{WR}$ or $\overline{DS}$ Inactive	t_9	10			ns	

Figure 18-10. Intel Bus Read AC Timing (BTS = 0/MUX = 0)

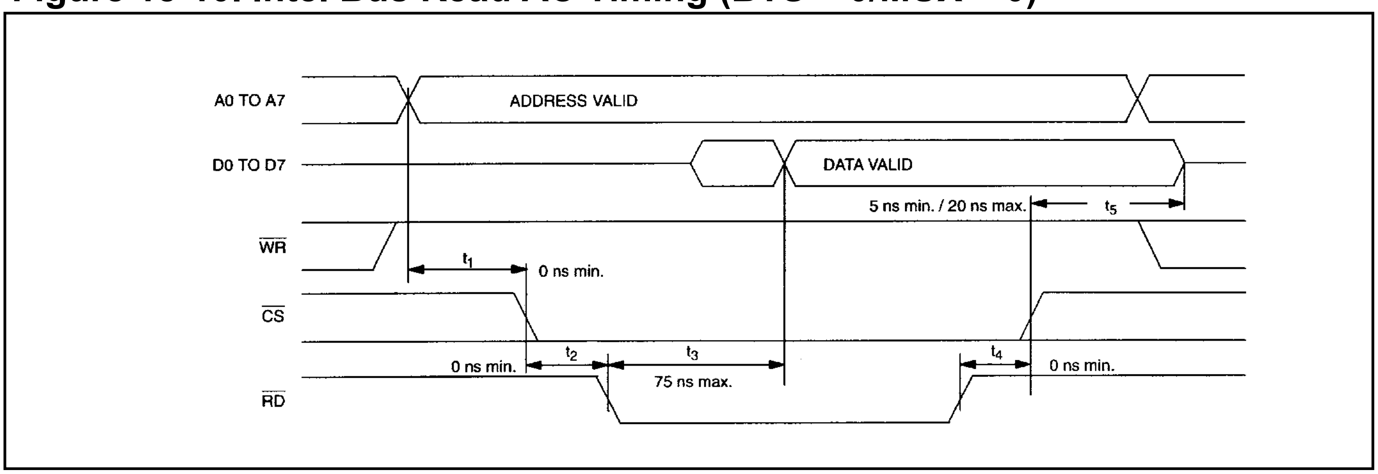


Figure 18-11. Intel Bus Write AC Timing (BTS=0/MUX=0)

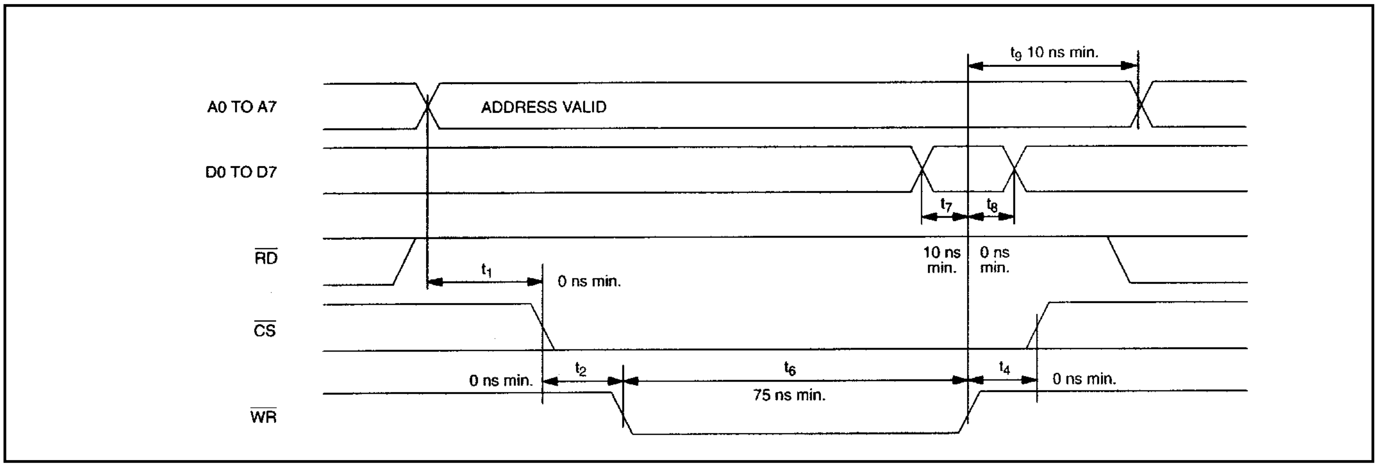


Figure 18-12. Motorola Bus Read AC Timing (BTS = 1/MUX = 0)

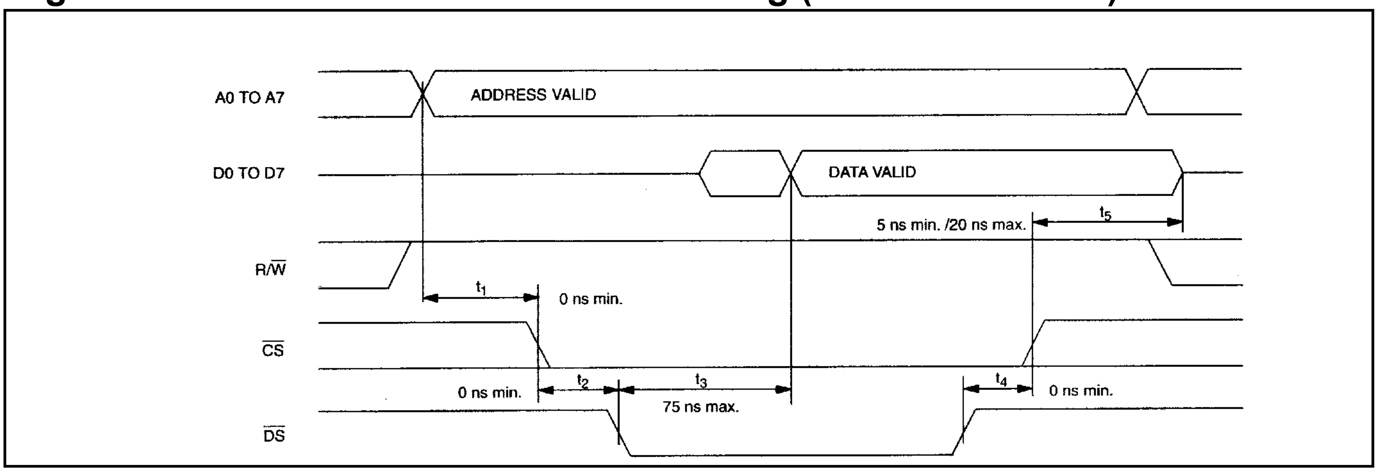
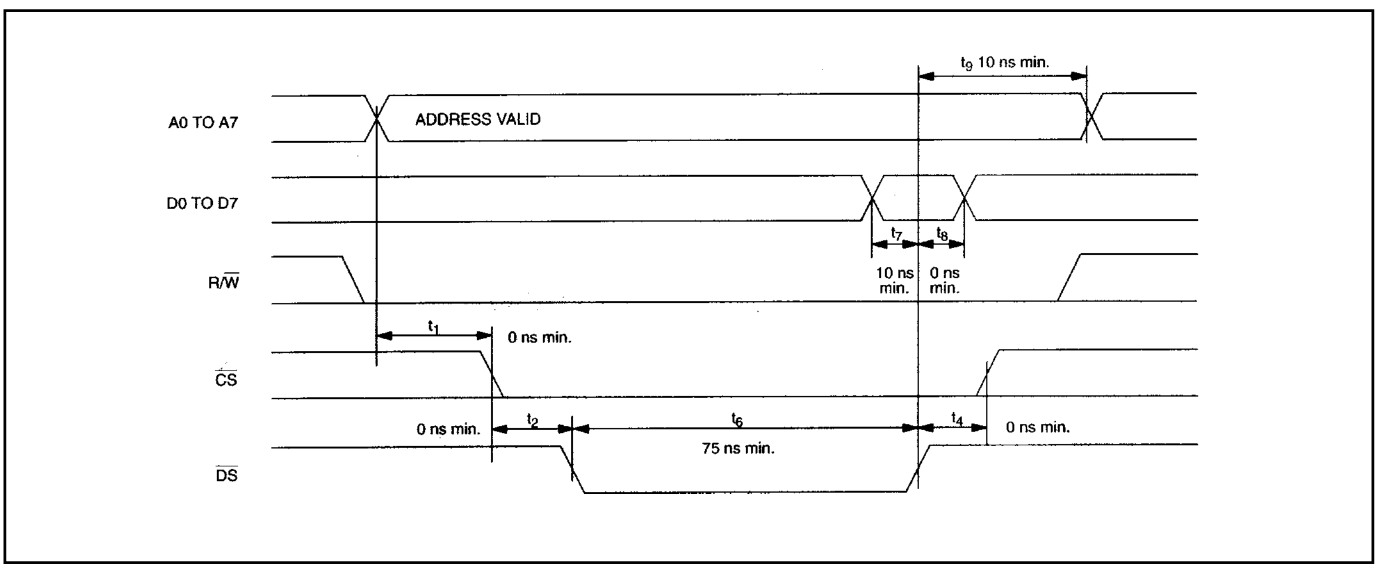


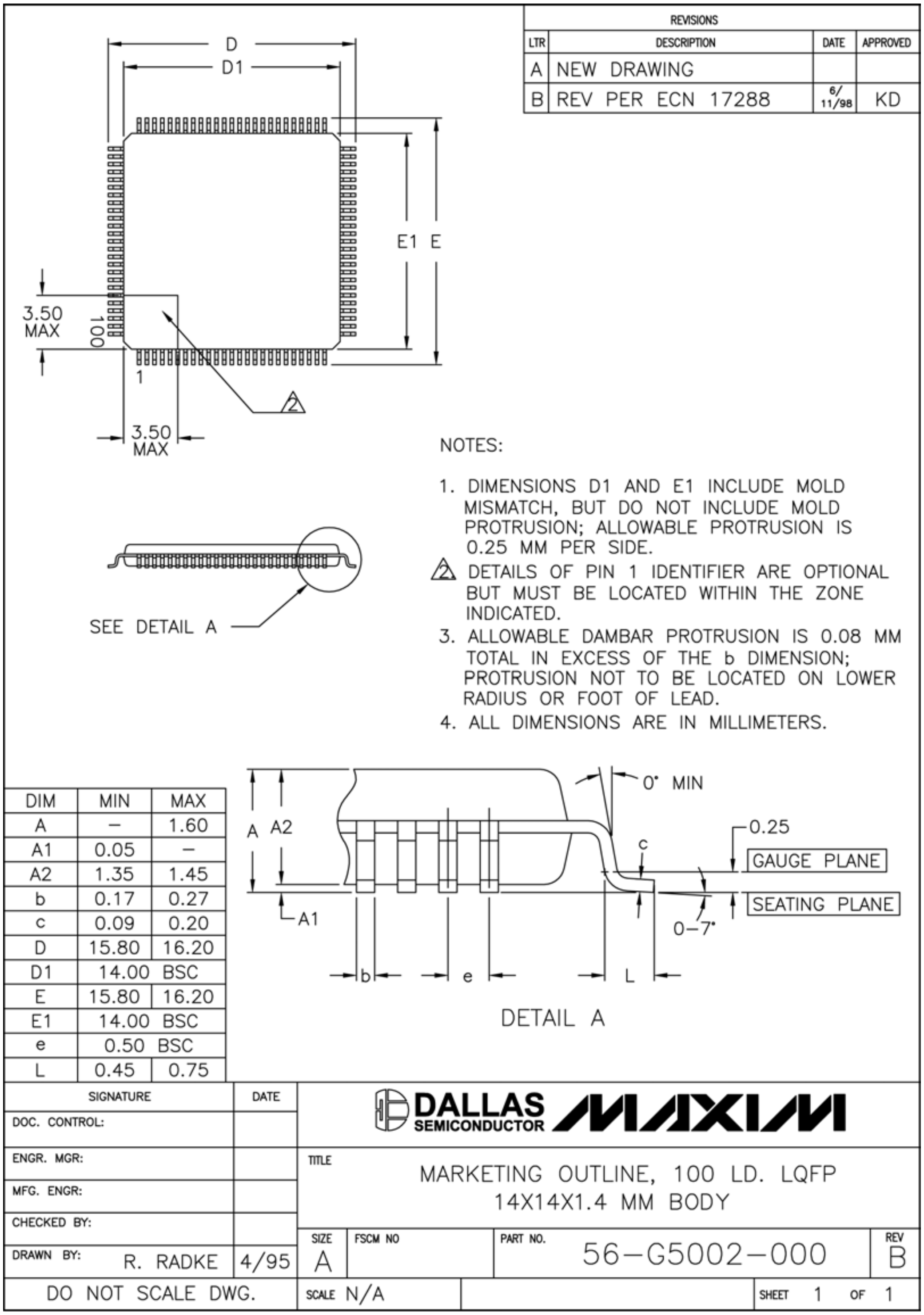
Figure 18-13. Motorola Bus Write AC Timing (BTS = 1/MUX = 0)



19 PACKAGE INFORMATION

(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information.)

19.1 100-Pin LQFP (56-G5002-000)



DIM	MIN	MAX
A	–	1.60
A1	0.05	–
A2	1.35	1.45
b	0.17	0.27
c	0.09	0.20
D	15.80	16.20
D1	14.00 BSC	
E	15.80	16.20
E1	14.00 BSC	
e	0.50 BSC	
L	0.45	0.75

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