



# STB18N65M5, STD18N65M5

N-channel 650 V, 0.198  $\Omega$  typ., 15 A MDmesh™ V Power MOSFET in D<sup>2</sup>PAK and DPAK packages

Datasheet — production data

## Features

Order codes	V <sub>DSS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STB18N65M5	710 V	< 0.22 $\Omega$	15 A
STD18N65M5			

- Worldwide best R<sub>DS(on)</sub> \* area
- Higher V<sub>DSS</sub> rating and high dv/dt capability
- Excellent switching performance
- 100% avalanche tested

## Applications

- Switching applications

## Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

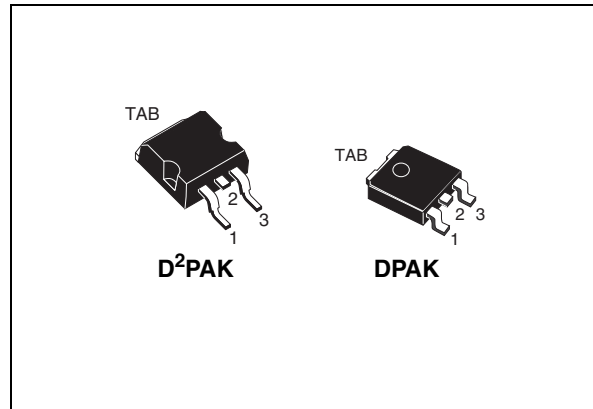


Figure 1. Internal schematic diagram

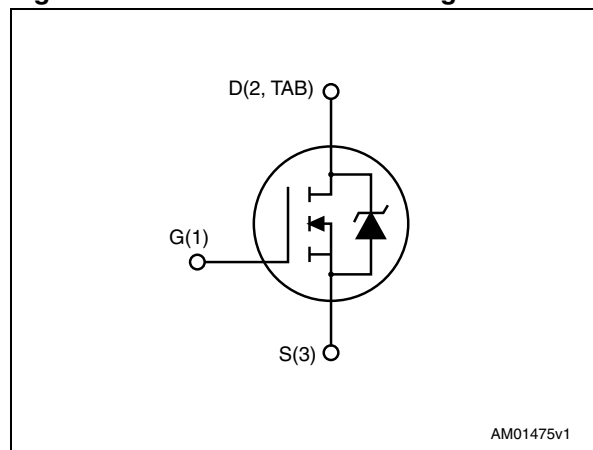


Table 1. Device summary

Order codes	Marking	Package	Packaging
STB18N65M5	18N65M5	D <sup>2</sup> PAK	Tape and reel
STD18N65M5		DPAK	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK	DPAK	
V <sub>GS</sub>	Gate-source voltage	± 25		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	15		A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	9.4		A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	60		A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	110		W
dv/dt <sup>(1)</sup>	Peak diode recovery voltage slope	15		V/ns
T <sub>stg</sub>	Storage temperature	- 55 to 150		°C
T <sub>j</sub>	Max. operating junction temperature	150		°C

1. I<sub>SD</sub> ≤ 15 A, di/dt ≤ 400 A/μs; V<sub>DSPeak</sub> < V<sub>(BR)DSS</sub>, V<sub>DD</sub> = 400 V

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK	DPAK	
R <sub>thj-case</sub>	Thermal resistance junction-case max	1.14		°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb max	30	50	°C/W

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board.

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not repetitive (pulse width limited by T <sub>jmax</sub> )	4	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> ; V <sub>DD</sub> = 50 V)	210	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 7.5\text{ A}$		0.198	0.22	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	1240	-	pF
$C_{oss}$	Output capacitance			32		
$C_{rss}$	Reverse transfer capacitance			3.2		
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0$	-	99	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			30		
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	3	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 7.5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 18</a> )	-	31	-	nC
$Q_{gs}$	Gate-source charge			8		
$Q_{gd}$	Gate-drain charge			14		

1. Time related is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_d$ (V)	Voltage delay time	$V_{DD} = 400$ V, $I_D = 9.5$ A,		36		ns
$t_r$ (V)	Voltage rise time	$R_G = 4.7$ $\Omega$ , $V_{GS} = 10$ V	-	7	-	ns
$t_{f(i)}$	Current fall time	(see <a href="#">Figure 19</a> and		9		ns
$t_{c(off)}$	Crossing time	<a href="#">Figure 22</a> )		11		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		15	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		60	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 15$ A, $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 15$ A, $di/dt = 100$ A/ $\mu$ s	-	290		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100$ V (see <a href="#">Figure 22</a> )		3.4		$\mu$ C
$I_{RRM}$	Reverse recovery current			23.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 15$ A, $di/dt = 100$ A/ $\mu$ s	-	352		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100$ V, $T_j = 150$ °C		4		$\mu$ C
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 22</a> )		24		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300  $\mu$ s, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D<sup>2</sup>PAK

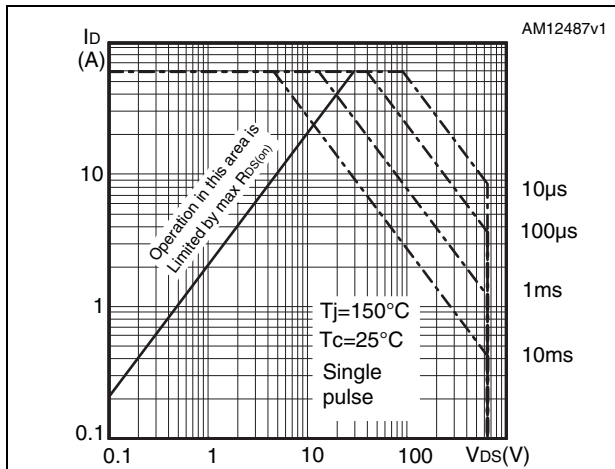


Figure 3. Thermal impedance for D<sup>2</sup>PAK

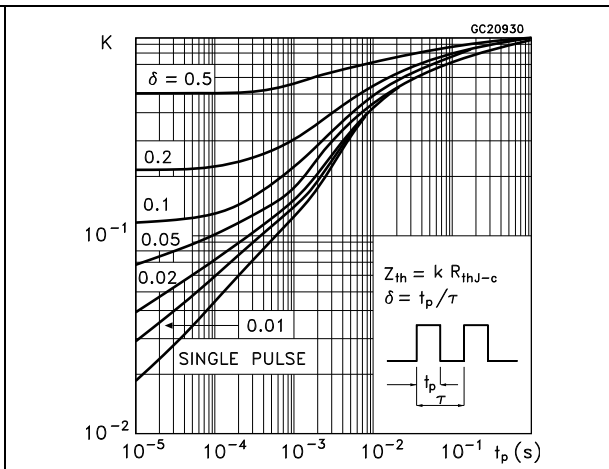


Figure 4. Safe operating area for DPAK

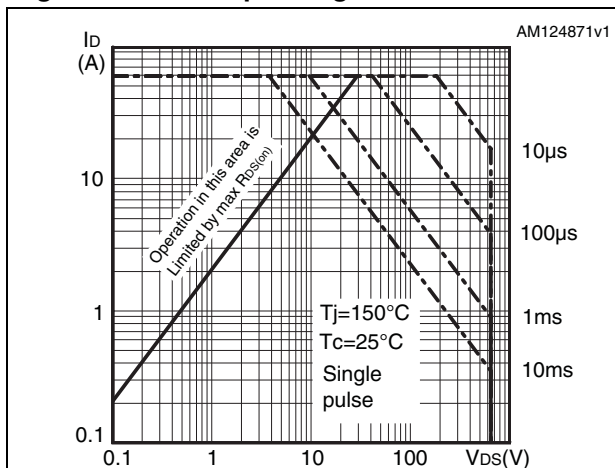


Figure 5. Thermal impedance for DPAK

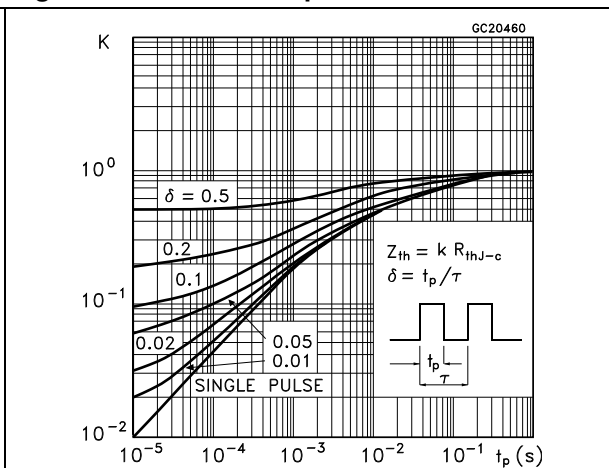


Figure 6. Output characteristics

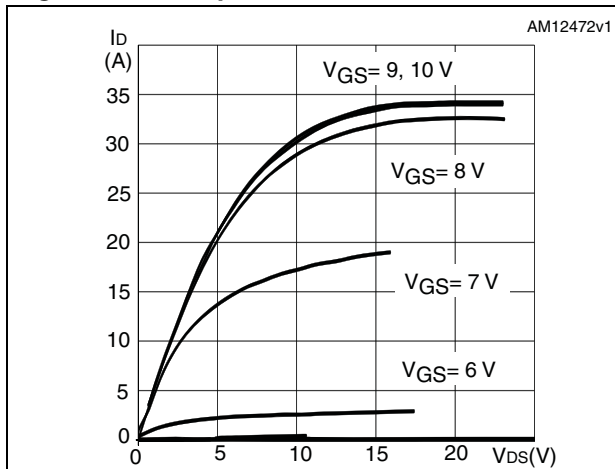


Figure 7. Transfer characteristics

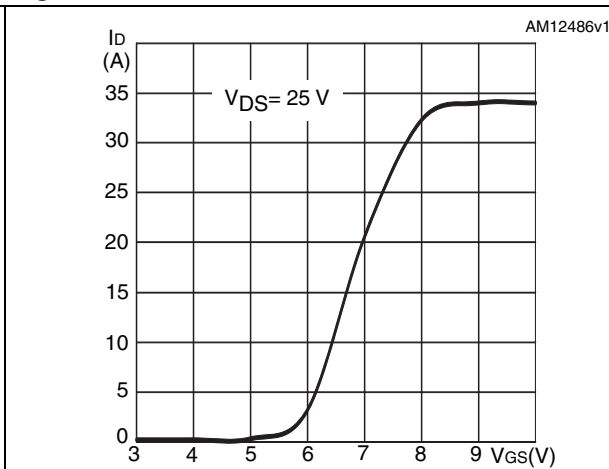


Figure 8. Gate charge vs gate-source voltage Figure 9. Static drain-source on-resistance

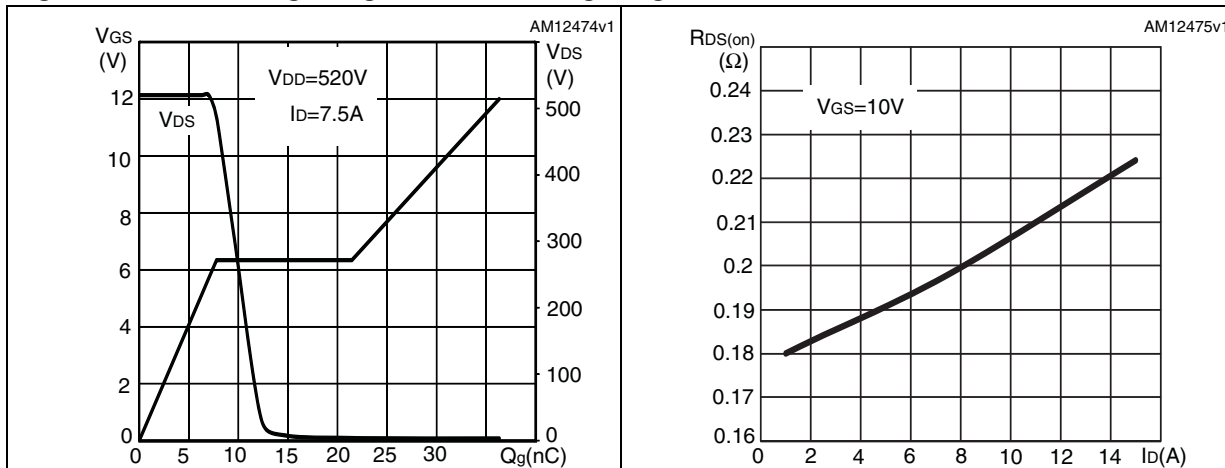


Figure 10. Capacitance variations Figure 11. Output capacitance stored energy

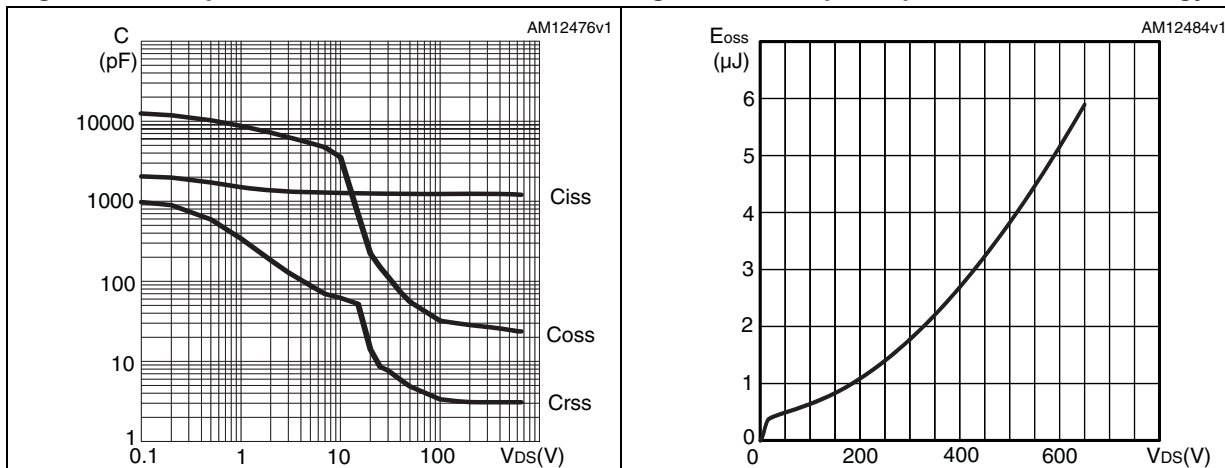


Figure 12. Normalized gate threshold voltage vs temperature Figure 13. Normalized on-resistance vs temperature

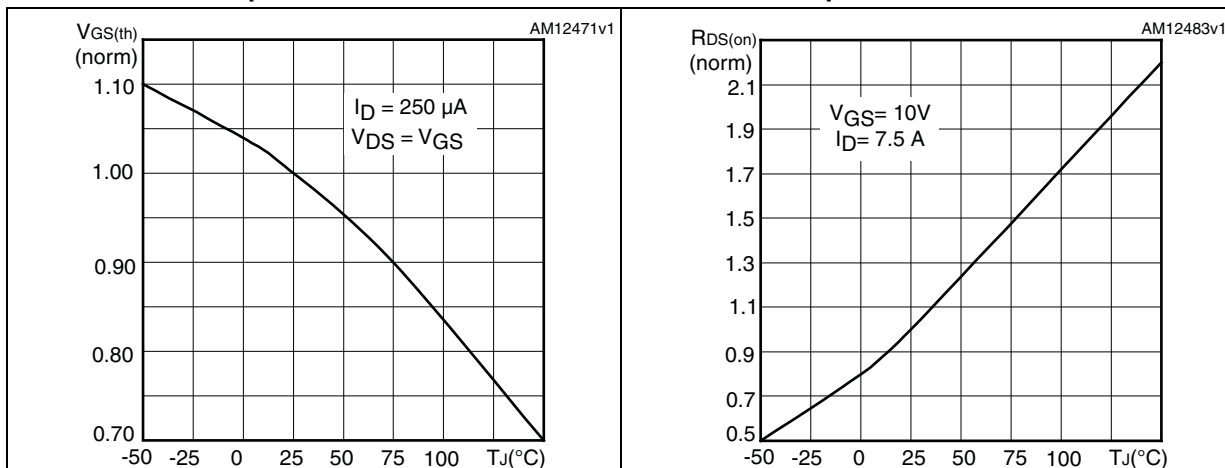


Figure 14. Drain-source diode forward characteristics

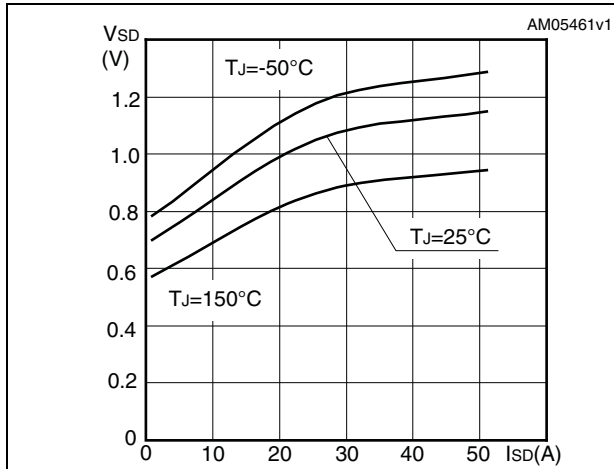


Figure 15. Normalized  $B_{VDSS}$  vs temperature

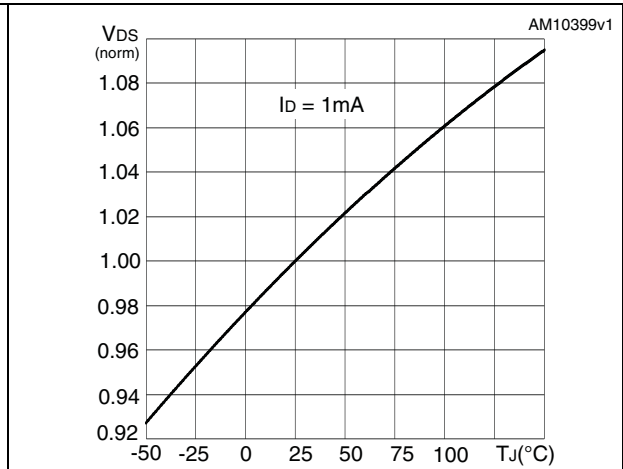
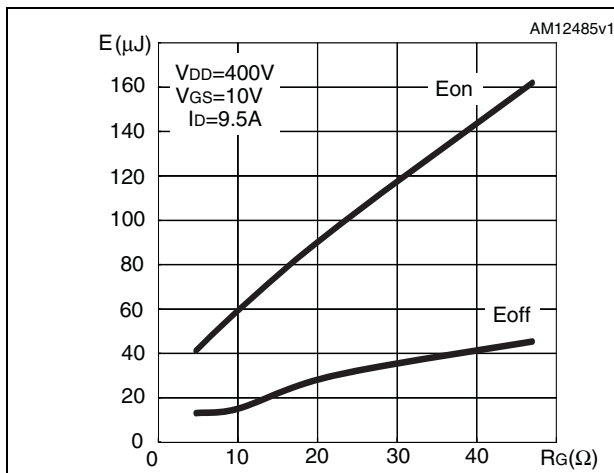


Figure 16. Switching losses vs gate resistance (1)



1. Eon including reverse recovery of a SiC diode





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 9. D<sup>2</sup>PAK (TO-263) mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D<sup>2</sup>PAK (TO-263) drawing



Figure 24. D<sup>2</sup>PAK footprint<sup>(a)</sup>



a. All dimensions are in millimeters

Table 10. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 25. DPAK (TO-252) drawing

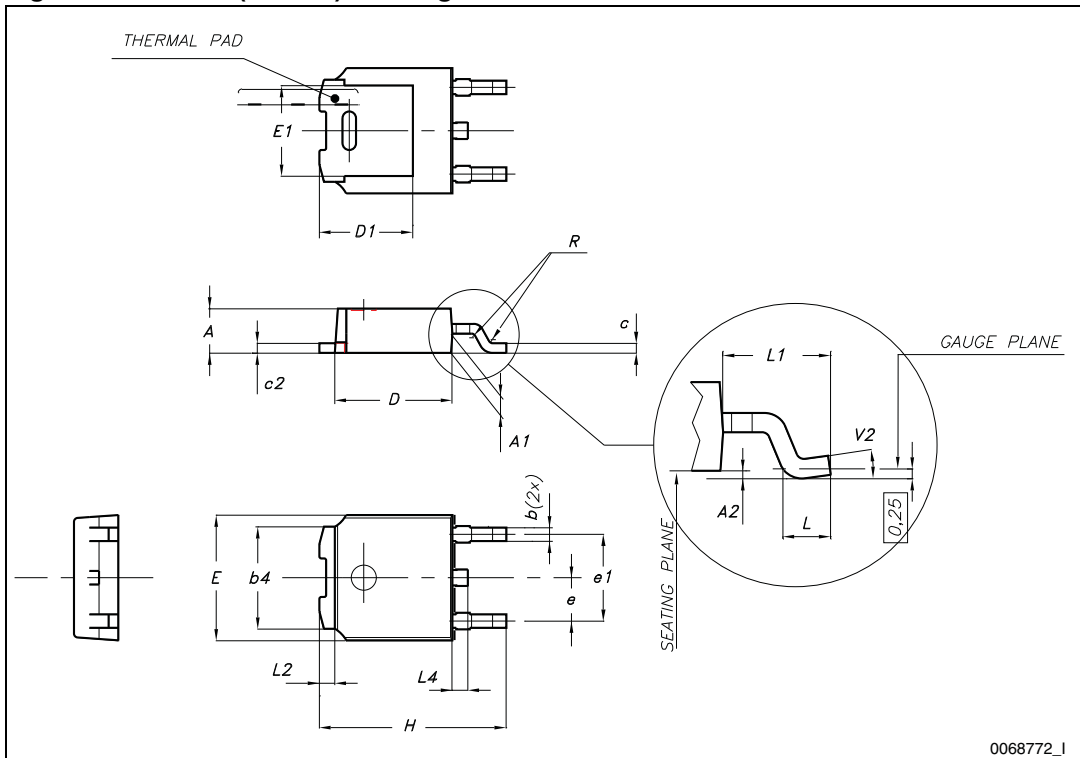
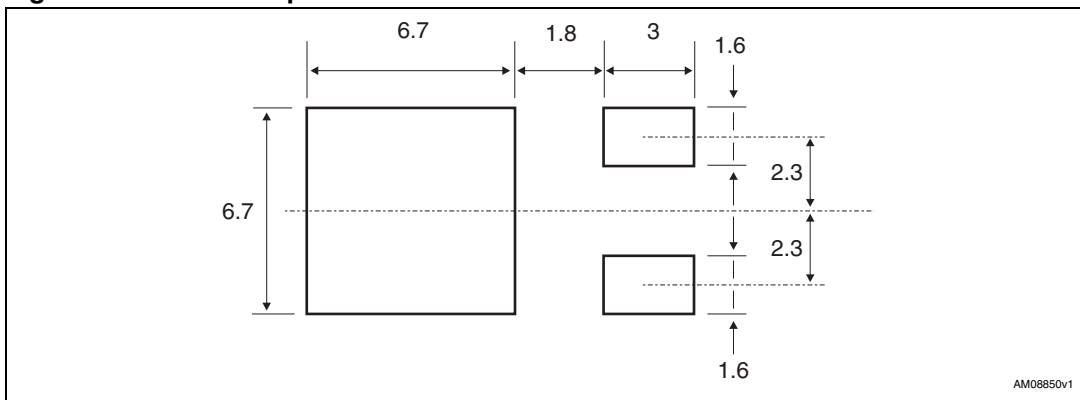


Figure 26. DPAK footprint<sup>(b)</sup>



b. All dimensions are in millimeters

## 5 Packaging mechanical data

**Table 11. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

**Table 12. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000

Table 12. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data (continued)

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
R	50				
T	0.25	0.35			
W	23.7	24.3			

Figure 27. Tape for D<sup>2</sup>PAK (TO-263) and DPAK (TO-252)

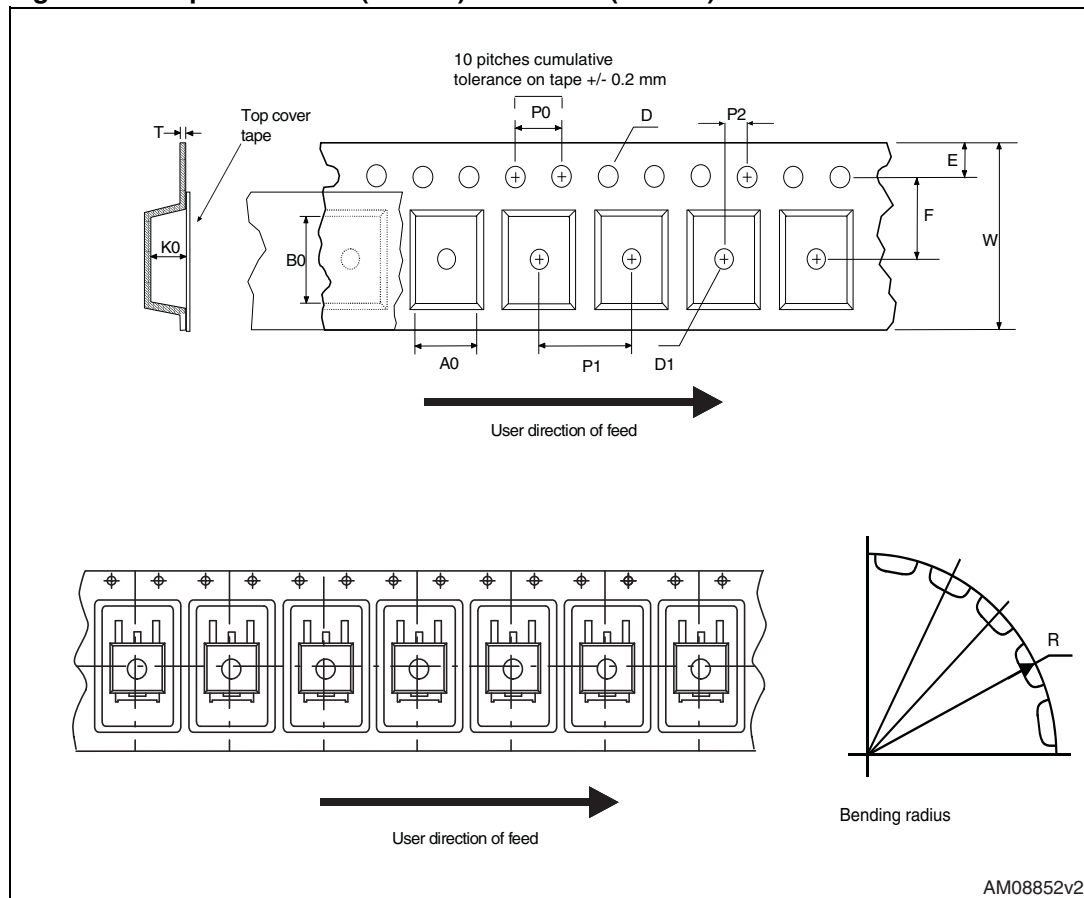
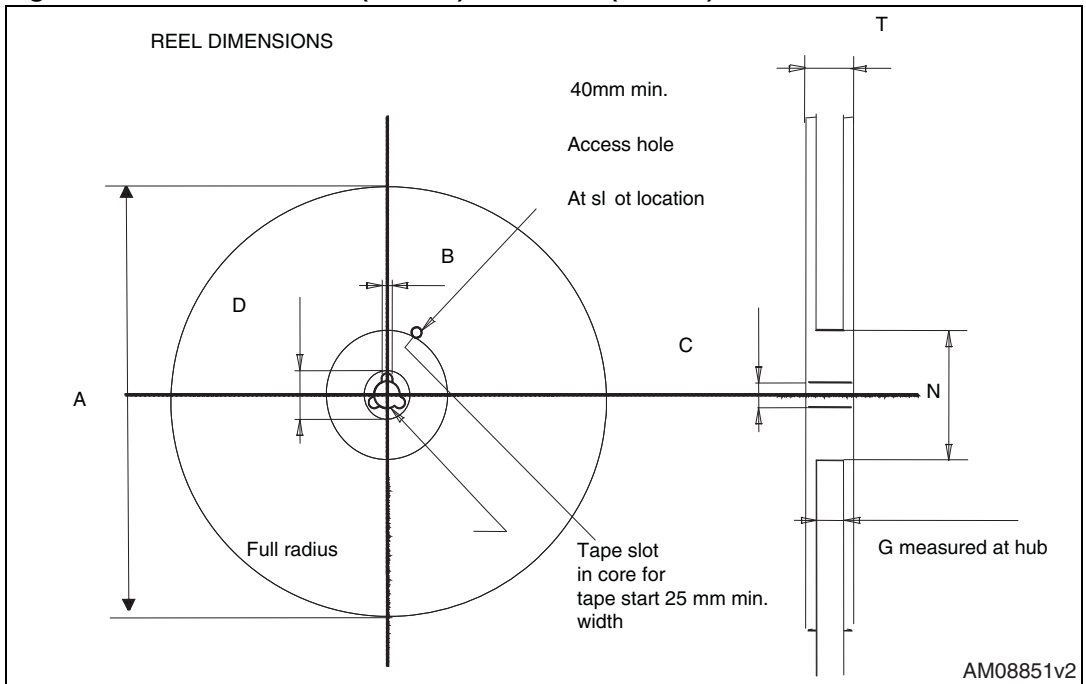


Figure 28. Reel for D<sup>2</sup>PAK (TO-263) and DPAK (TO-252)





## 6 Revision history

Table 13. Document revision history

Date	Revision	Changes
18-Jul-2012	1	First release.

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