# Isolated Half-Bridge Driver with Integrated High-Side Supply

# ADuM5230

## FEATURES

Integrated, isolated high-side supply
150 mW of secondary side power
Isolated high-side and low-side outputs
100 mA output source current, 300 mA output sink current
High common-mode transient immunity: >25 kV/μs
High temperature operation: 105°C
Adjustable power level
Wide body, 16-lead SOIC package
**Safety and regulatory approvals**
    UL recognition: 2500 V rms for 1 minute per UL1577
Qualified for automotive applications

## APPLICATIONS

MOSFET/IGBT gate drives
Automotive
Motor drives
Power supplies

## FUNCTIONAL BLOCK DIAGRAM



DNC = DO NOT CONNECT. DO NOT CONNECT TO THIS PIN.

*Figure 1.*

## GENERAL DESCRIPTION

The ADuM5230[1] is an isolated half-bridge gate driver that employs Analog Devices, Inc., *i*Coupler® technology to provide independent and isolated high-side and low-side outputs. Combining CMOS and microtransformer technologies, this isolation component contains an integrated dc-to-dc converter providing an isolated high-side supply. This eliminates the cost, space, and performance difficulties associated with external supply configurations such as bootstrap circuitry. This high-side isolated supply powers not only the ADuM5230 high-side output but also any external buffer circuitry used with the ADuM5230.
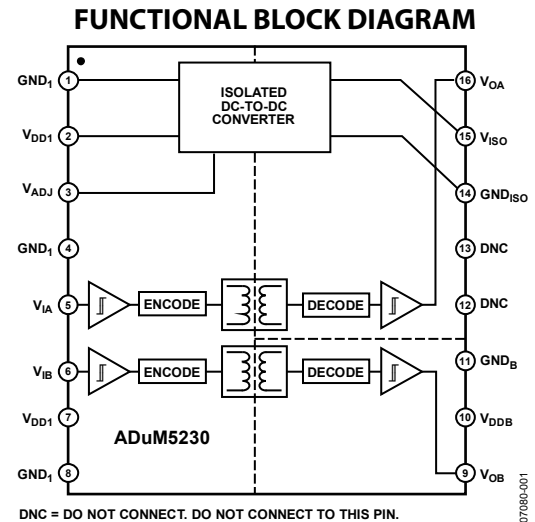
In comparison to gate drivers employing high voltage level translation methodologies, the ADuM5230 offers the benefit of true, galvanic isolation between the input and each output. Each output can operate up to ±700 $V_P$ relative to the input, thereby supporting low-side switching to negative voltages. The differential voltage between the high side and low side may be as high as 700 $V_P$.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; 7,075,329; other pending patents.

# ADUM5230* PRODUCT PAGE QUICK LINKS

**Last Content Update: 02/23/2017**

## COMPARABLE PARTS 🗖

View a parametric search of comparable parts.

## EVALUATION KITS 🗖

- AD-FMCMOTCON2-EBZ Evaluation Board

## DOCUMENTATION 🗖

**Application Notes**

- AN-0971: Recommendations for Control of Radiated Emissions with isoPower Devices
- AN-727: iCoupler® Isolation in RS-485 Applications
- AN-740: iCoupler® Isolation in RS-232 Applications
- AN-770: iCoupler® Isolation in CAN Bus Applications
- AN-793: ESD/Latch-Up Considerations with iCoupler® Isolation Products
- AN-825: Power Supply Considerations in iCoupler® Isolation Products
- AN-913: Isolating I2C Interfaces

**Data Sheet**

- ADuM5230: Isolated Half-Bridge Driver with Integrated High-Side Supply Data Sheet

## REFERENCE MATERIALS 🗖

**Press**

- Analog Devices Achieves Major Milestone by Shipping 1 Billionth Channel of iCoupler Digital Isolation

**Product Selection Guide**

- Digital Isolator Product Selection and Resource Guide

**Technical Articles**

- *i*Coupler® Products with *iso*Power™ Technology: Signal and Power Transfer Across Isolation Barrier Using Microtransformers
- High Speed Digital Isolators Using Microscale On-Chip Transformers
- Inside iCoupler® Technology:ADuM347x PWM Controller and Transformer Driver with Quad-Channel Isolators Design Summary
- Micro-Transformers Provide Signal and Power Isolation for Hybrid Electric Vehicles
- Microtransformer Isolation Benefits Digital Control
- MS-2663-1: Powering the Isolated Side of Your Half-Bridge Configuration
- N*App*kin Note: Lowering the Power of the ADuM524x

## DESIGN RESOURCES 🗖

- ADUM5230 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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# TABLE OF CONTENTS

## REVISION HISTORY

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

All voltages are relative to their respective ground. 4.5 V ≤ $V_{DD1}$ ≤ 5.5 V, 12.0 ≤ $V_{DDB}$ ≤ 18.0 V. All min/max specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_A$ = 25°C, $V_{DD1}$ = 5.0 V, $V_{DDB}$ = 15 V.

**Table 1.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| DC SPECIFICATIONS | | | | | | |
| Input Supply Current, Quiescent | $I_{DD1 (Q)}$ | | | 125 | mA | $I_{ISO}$ = 0 mA, dc signal inputs, $V_{ADJ}$ = open |
| Channel B Supply Current, Quiescent | $I_{DDB (Q)}$ | | | 1.6 | mA | |
| Channel A Output Supply Voltage | $V_{ISO}$ | 12 | 15 | 18.5 | V | |
| At 0 kHz Switching Frequency | | | | | | |
| Maximum Channel A Output Supply Current | $I_{ISO (MAX, 0)}$ | 10 | | | mA | |
| At 100 kHz Switching Frequency | | | | | | |
| Maximum Channel A Output Supply Current | $I_{ISO (MAX, 100)}$ | 7.5 | | | mA | $C_L$ = 200 pF |
| Input Supply Current | $I_{DD1}$ | | | 200 | mA | $I_{ISO}$ = $I_{ISO (MAX, 100)}$ |
| Channel B Supply Current | $I_{DDB}$ | | | 1.8 | mA | $C_L$ = 200 pF |
| At 1000 kHz Switching Frequency | | | | | | |
| Maximum Channel A Output Supply Current | $I_{ISO (MAX, 1000)}$ | 5.0 | | | mA | $C_L$ = 200 pF |
| Input Supply Current | $I_{DD1}$ | | | 200 | mA | $I_{ISO}$ = $I_{ISO (MAX, 1000)}$ |
| Channel B Supply Current | $I_{DDB}$ | | | 7.5 | mA | $C_L$ = 200 pF |
| Input Currents | $I_{IA}$, $I_{IB}$ | −10 | +0.01 | +10 | µA | 0 ≤ $V_{IA}$, $V_{IB}$ ≤ 5.5 V |
| Logic High Input Voltage | $V_{ATH}$, $V_{BTH}$ | 0.7 × $V_{DD1}$ | | | V | |
| Logic Low Input Voltage | $V_{ATL}$, $V_{BTL}$ | | | 0.3 × $V_{DD1}$ | V | |
| Logic High Output Voltages | $V_{OAH}$, $V_{OBH}$ | $V_{ISO}$ − 0.1, $V_{DDB}$ − 0.1 | | $V_{ISO}$, $V_{DDB}$ | V | $I_{OA}$, $I_{OB}$ = −1 mA |
| Logic Low Output Voltages | $V_{OAL}$, $V_{OBL}$ | | | 0.1 | V | $I_{OA}$, $I_{OB}$ = 1 mA |
| Undervoltage Lockout, $V_{ISO}$ and $V_{DDB}$ Supply | | | | | | |
| Positive-Going Threshold | $V_{DDBUV+}$ | 8.0 | | 10.1 | V | |
| Negative-Going Threshold | $V_{DDBUV−}$ | 7.4 | | 9.0 | V | |
| Hysteresis | $V_{DDBUVH}$ | | 0.9 | | V | |
| Undervoltage Lockout, $V_{DD1}$ Supply | | | | | | |
| Positive-Going Threshold | $V_{DD1UV+}$ | 3.5 | | 4.2 | V | |
| Negative-Going Threshold | $V_{DD1UV−}$ | 3.0 | | 3.9 | V | |
| Hysteresis | $V_{DD1UVH}$ | | 0.4 | | V | |
| Output Short-Circuit Pulsed Current, Sourcing[1] | $I_{OA}$, $I_{OB}$ | 100 | | | mA | |
| Output Short-Circuit Pulsed Current, Sinking[1] | $I_{OA}$, $I_{OB}$ | 300 | | | mA | |
| SWITCHING SPECIFICATIONS | | | | | | |
| Minimum Pulse Width[2] | PW | | | 100 | ns | $C_L$ = 200 pF |
| Maximum Switching Frequency[3] | | 1 | | | MHz | $C_L$ = 200 pF |
| Propagation Delay[4] | $t_{PHL}$, $t_{PLH}$ | | | 100 | ns | $C_L$ = 200 pF |
| Change vs. Temperature | | | 100 | | ps/°C | |
| Pulse Width Distortion, $\lvert t_{PLH} − t_{PHL} \rvert$ | PWD | | | 8 | ns | $C_L$ = 200 pF |
| Channel-to-Channel Matching, Rising or Falling Matching Edge Polarity[5] | $t_{M2}$ | | | 8 | ns | $C_L$ = 200 pF |
| Channel-to-Channel Matching, Rising vs. Falling Opposite Edge Polarity[6] | $t_{M1}$ | | | 10 | ns | $C_L$ = 200 pF |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| Part to Part Matching, Rising or Falling Edges[7] | | | | 55 | ns | $C_L$ = 200 pF |
| Part to Part Matching, Rising vs. Falling Edges[8] | | | | 63 | ns | $C_L$ = 200 pF |
| Common-Mode Transient Immunity at Logic High Output | $\|CM_H\|$ | 25 | 35 | | kV/µs | $V_{Ix}$ = $V_{DD1}$, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output | $\|CM_L\|$ | 25 | 35 | | kV/µs | $V_{Ix}$ = 0 V, $V_{CM}$ = 1000 V, transient magnitude = 800 V |
| Output Rise Time (10% to 90%) | $t_R$ | | | 25 | ns | $C_L$ = 200 pF, $I_{ISO}$ = 10 mA, 100 kHz switching frequency |
| Output Fall Time (10% to 90%) | $t_F$ | | | 10 | ns | $C_L$ = 200 pF, $I_{ISO}$ = 10 mA, 100 kHz switching frequency |

[1] Short-circuit duration is less than 1 sec. Average output current must conform to the limit shown under the Absolute Maximum Ratings section.

[2] The minimum pulse width is the shortest pulse width at which the specified timing parameters are guaranteed. Operation below the minimum pulse width is strongly discouraged because in some instances pulse stretching to 1 µs may occur.

[3] The maximum switching frequency is the maximum signal frequency at which the specified timing and power conversion parameters are guaranteed. Operation above the maximum frequency is strongly discouraged.

[4] $t_{PHL}$ propagation delay is measured from the 50% level of the falling edge of the $V_{Ix}$ signal to the 50% level of the falling edge of the $V_{Ox}$ signal. $t_{PLH}$ propagation delay is measured from the 50% level of the rising edge of the $V_{Ix}$ signal to the 50% level of the rising edge of the $V_{Ox}$ signal.

[5] In channel-to-channel matching, the rising or falling matching edge polarity is the magnitude of the propagation delay difference between two channels of the same part when both inputs are either both rising or falling edges. The loads on each channel are equal.

[6] In channel-to-channel matching, the rising vs. falling opposite edge polarity is the magnitude of the propagation delay difference between two channels of the same part when one input is a rising edge and one input is a falling edge. The loads on each channel are equal.

[7] Part-to-part matching, rising or falling edges, is the magnitude of the propagation delay difference between the same channels of two different parts when the inputs are either both rising or falling edges. The supply voltages, temperatures, and loads of each part are equal.

[8] Part-to-part matching, rising vs. falling edges, is the magnitude of the propagation delay difference between the same channels of two different parts when one input is a rising edge and the other input is a falling edge. The supply voltages, temperatures, and loads of each part are equal.

## PACKAGE CHARACTERISTICS

**Table 2.**

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| Resistance (Input to Output)[1] | $R_{I-O}$ | | $10^{12}$ | | Ω | |
| Capacitance (Input to Output)[1] | $C_{I-O}$ | | 2.0 | | pF | f = 1 MHz |
| Input Capacitance | $C_I$ | | 4.0 | | pF | |
| IC Junction-to-Ambient Thermal Resistance | $θ_{JA}$ | | 48 | | °C/W | |

[1] The device is considered a two-terminal device: Pin 1 to Pin 8 are shorted together, and Pin 9 to Pin 16 are shorted together.

## REGULATORY INFORMATION

The ADuM5230 is approved by the organization listed in Table 3.

**Table 3.**

| UL[1] |
|---|
| Recognized under 1577 component recognition program, File E214100 |

[1] In accordance with UL1577, each ADuM5230 is proof-tested by applying an insulation test voltage ≥ 3000 V rms for 1 sec (current leakage detection limit = 5 μA).

## INSULATION AND SAFETY-RELATED SPECIFICATIONS

**Table 4.**

| Parameter | Symbol | Value | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| Rated Dielectric Insulation Voltage | | 2500 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance) | L(I01) | 3.5 min | mm | Measured from input conductors to output conductors, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 3.5 min | mm | Measured from input conductors to output conductors, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 0.017 min | mm | Distance through the insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | IIIa | | Material Group (DIN VDE 0110, 1/89, Table 1) |
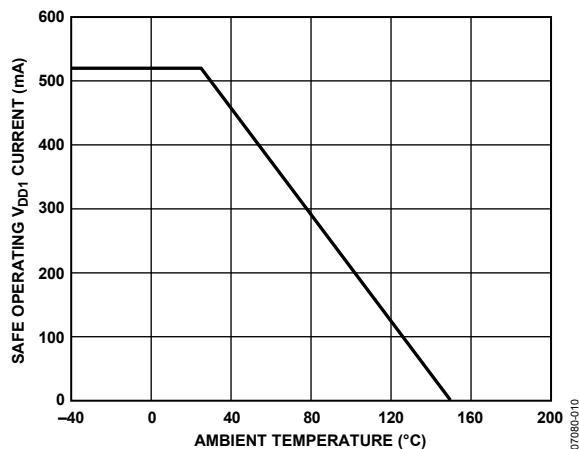


*Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2*

## RECOMMENDED OPERATING CONDITIONS

**Table 5.**

| Parameter | Value |
|---|---|
| Operating Temperature ($T_A$) | −40°C to +105°C |
| Input Supply Voltage[1] ($V_{DD1}$) | 4.5 V to 5.5 V |
| Channel B Supply Voltage[1] ($V_{DDB}$) | 12 V to 18.5 V |
| Input Signal Rise and Fall Times | 1 ms |

[1] All voltages are relative to their respective ground.

# ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

**Table 6.**

| Parameter | Rating |
|---|---|
| Storage Temperature ($T_{ST}$) | −55°C to +150°C |
| Ambient Operating Temperature ($T_A$) | −40°C to +105°C |
| Input Supply Voltage ($V_{DD1}$)[1] | −0.5 V to +7.0 V |
| Channel B Supply Voltage ($V_{DDB}$)[1] | −0.5 V to +27 V |
| Input Voltage ($V_{IA}$, $V_{IB}$)[1] | −0.5 V to $V_{DDI}$ + 0.5 V |
| Output Voltage ($V_{OA}$, $V_{OB}$)[1] | −0.5 V to $V_{ISO}$ + 0.5 V, −0.5 V to $V_{DDB}$ + 0.5 V |
| Input-Output Voltage[2] | −700 $V_{PEAK}$ to +700 $V_{PEAK}$ |
| Output Differential Voltage[3] | 700 $V_{PEAK}$ |
| Output DC Current ($I_{OA}$, $I_{OB}$) | −20 mA to +20 mA |
| Common-Mode Transients[4] | −100 kV/μs to +100 kV/μs |

[1] All voltages are relative to their respective ground.
[2] Input-to-output voltage is defined as $GND_{ISO}$ − $GND_1$ or $GND_B$ − $GND_1$.
[3] Output differential voltage is defined as $GND_{ISO}$ − $GND_B$.
[4] Refers to common-mode transients across any insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

**Table 7. Maximum Continuous Working Voltage[1]**

| Parameter | Max | Unit | Constraint |
|---|---|---|---|
| AC Voltage | | | |
|    Bipolar Waveform | 424 | V peak | 50-year minimum lifetime |
|    Unipolar Waveform | | | |
|       Basic Insulation | 600 | V peak | 50-year minimum lifetime |
| DC Voltage | | | |
|    Basic Insulation | 600 | V peak | 50-year minimum lifetime |

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
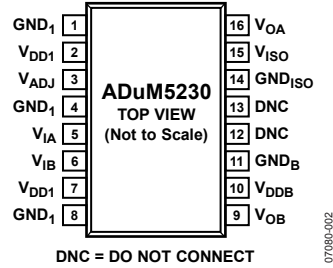
# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



*Figure 3. Pin Configuration*

**Table 8. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | $GND_1$ | Ground Reference for Input Logic Signals. |
| 2 | $V_{DD1}$ | Input Supply Voltage, 4.5 V to 5.5 V. |
| 3 | $V_{ADJ}$ | Adjusts Internal DC-to-DC Converter Duty Cycle (Normally Left Unconnected). |
| 4 | $GND_1$ | Ground Reference for Input Logic Signals. |
| 5 | $V_{IA}$ | Logic Input A. |
| 6 | $V_{IB}$ | Logic Input B. |
| 7 | $V_{DD1}$ | Input Supply Voltage, 4.5 V to 5.5 V. |
| 8 | $GND_1$ | Ground Reference for Input Logic Signals. |
| 9 | $V_{OB}$ | Output B Signal. |
| 10 | $V_{DDB}$ | Output B Supply Voltage, 12 V to 18 V. |
| 11 | $GND_B$ | Ground Reference for Output B Signal. |
| 12 | DNC | Do Not Connect. |
| 13 | DNC | Do Not Connect. |
| 14 | $GND_{ISO}$ | Ground Reference for Output A Signal and Isolated Output Supply Voltage. |
| 15 | $V_{ISO}$ | Isolated Output Supply Voltage. |
| 16 | $V_{OA}$ | Output A Signal. |

For specific layout guidelines, refer to the AN-0971 Application Note, *Recommendations for Control of Radiated Emissions with isoPower Devices.*

**Table 9. Truth Table (Positive Logic)**

| $V_{IA}$ Input[1] | $V_{IB}$ Input[1] | $V_{DD1}$ State[2] | $V_{ISO}$ State[2] | $V_{DDB}$ State[1, 2] | $V_{OA}$ Output | $V_{OB}$ Output | Notes |
|---|---|---|---|---|---|---|---|
| High | High | Powered | Powered | Powered | High | High | |
| High | Low | Powered | Powered | Powered | High | Low | |
| Low | High | Powered | Powered | Powered | Low | High | |
| Low | Low | Powered | Powered | Powered | Low | Low | |
| X | X | UVLO | Unpowered | X | Low | Low | Output returns to input state within 1 µs of $V_{DD1}$ power restoration. |
| X | X | Powered | UVLO | Unpowered | Low | Low | Output returns to input state within 1 µs of $V_{ISO}$ and $V_{DDB}$ power restoration. |
| X | High | Powered | UVLO | Powered | Low | High | Output returns to input state within 1 µs of $V_{ISO}$ power restoration. |
| X | Low | Powered | UVLO | Powered | Low | Low | Output returns to input state within 1 µs of $V_{ISO}$ power restoration. |
| High | X | Powered | Powered | UVLO | High | Low | $V_{OB}$ output returns to input state within 1 µs of $V_{DDB}$ power restoration. |
| Low | X | Powered | Powered | UVLO | Low | Low | $V_{OB}$ output returns to input state within 1 µs of $V_{DDB}$ power restoration. |

[1] X means don't care.
[2] UVLO represents either a voltage below the UVLO threshold for that supply or absence of power.
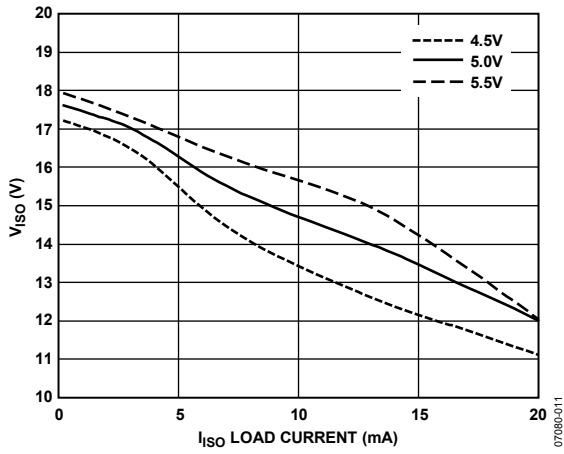
# TYPICAL PERFOMANCE CHARACTERISTICS



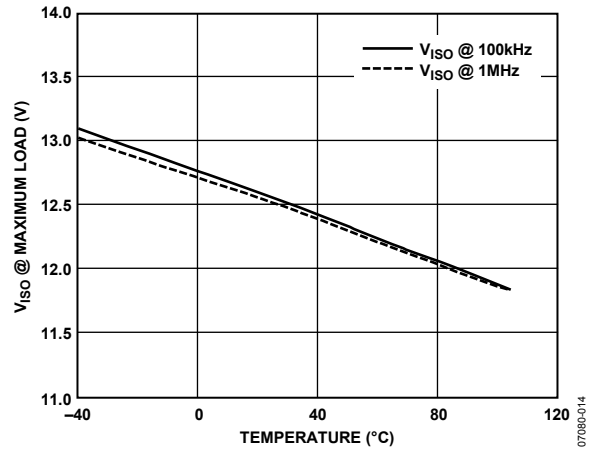Figure 4. Typical $V_{ISO}$ Supply Voltage vs. $I_{ISO}$ External Load Current



Figure 5. Typical $V_{DD1}$ Supply Current vs. $V_{ISO}$ External Load Current



Figure 6. Typical $V_{ISO}$ Supply Efficiency vs. $V_{ISO}$ External Load Current



Figure 7. Typical $V_{ISO}$ Output Voltage at Maximum Combined Load over Temperature
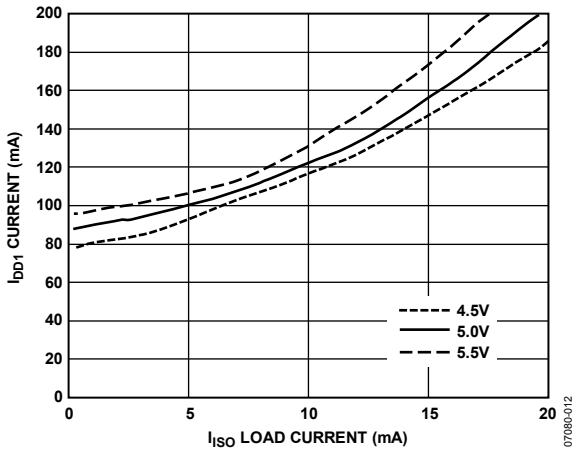


Figure 8. Typical Current Consumption for $V_{OA}$ or $V_{OB}$ Outputs, $C_L$ = 200 pF
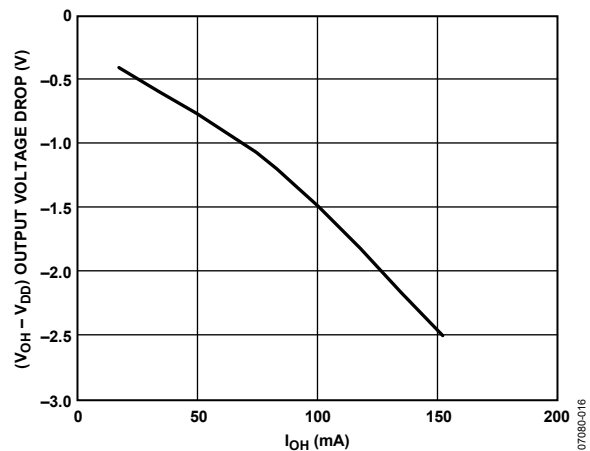


Figure 9. Typical $V_{OH}$ Drop vs. $I_{OH}$ ($V_{DD1}$ = 5 V, $V_{DDB}$, $V_{ISO}$ = 12 V to 18 V)
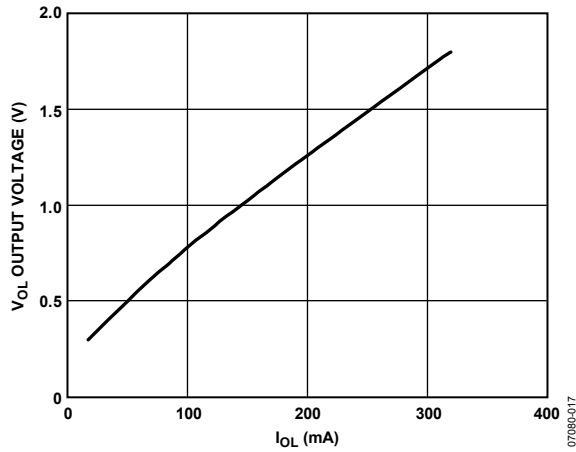
Figure 10. Typical $V_{OL}$ vs. $I_{OL}$ ($V_{DD1}$ = 5 V, $V_{DDB}$, $V_{ISO}$ = 12 V to 18 V)



Figure 11. Typical Propagation Delay vs. Temperature



Figure 12. Power Dissipation vs. Load Impedance for Fault Conditions



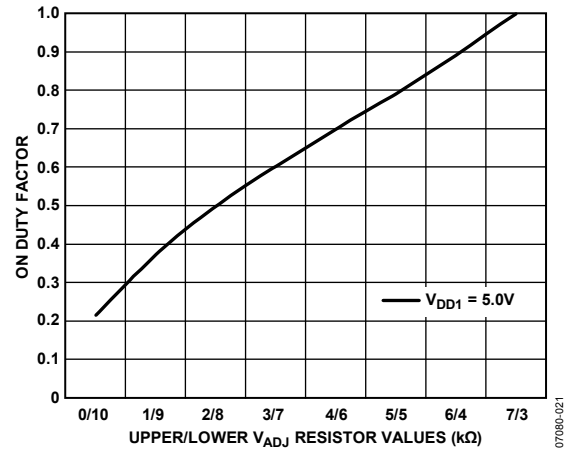Figure 13. Current Available at the Output vs. PWM Duty Factor for $V_{DD1}$ = 5 V



Figure 14. Upper/Lower $V_{ADJ}$ Voltage Divider Resistor Values
to Determine PWM Duty Factor for $V_{DD1}$ = 5 V

# APPLICATIONS INFORMATION

## THEORY OF OPERATION

The dc-to-dc converter section of the ADuM5230 works on principles that are common to most modern power supply designs. It is implemented as an open-loop PWM controller, which sets the power level being transferred to the secondary. $V_{DD1}$ power is supplied to an oscillating circuit that switches current into a chip-scale air core transformer. On the secondary side, power is rectified to a dc voltage. The voltage is then clamped to approximately 18 V and provided to the secondary side $V_{OA}$ data channel and to the $V_{ISO}$ pin for external use. The output voltage is unregulated and varies with load.

The PWM duty cycle is set by internal bias elements, but can be controlled externally through the $V_{ADJ}$ pin with an external resistor network. This feature allows the user to boost the available power at the secondary, or reduce excess power if it is not required for the application (see the Power Consumption section).

Undervoltage lockouts are provided on the $V_{DD1}$, $V_{DDB}$, and $V_{ISO}$ supply lines to interlock the data channels from low supply voltages.

## PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM5230 digital isolator with a 150 mW *iso*Power® integrated dc-to-dc converter requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 15). The power supply section of the ADuM5230 uses a very high oscillator frequency to pass power efficiently through its chip scale transformers. In addition, the normal operation of the data section of the *i*Coupler® introduces switching transients on the power supply pins. Bypass capacitors are required for several operating frequencies. Noise suppression requires a low inductance high frequency capacitor; ripple suppression and proper regulation require a large value capacitor. These are most conveniently connected between Pin 1 and Pin 2 for $V_{DD1}$ and between Pin 15 and Pin 14 for $V_{ISO}$. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0.1 µF and 10 µF. It is strongly recommended that a very low inductance ceramic or equivalent capacitor be used for the smaller value. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing with noise suppression and stiffening capacitors is recommended between Pin 1 and Pin 2, a bypass capacitor is recommended between Pin 7 and Pin 8. Bypassing with noise suppression and stiffening capacitors is recommended between Pin 14 and Pin 15.

See the AN-0971 Application Note for board layout guidelines and reduction of radiated emissions.
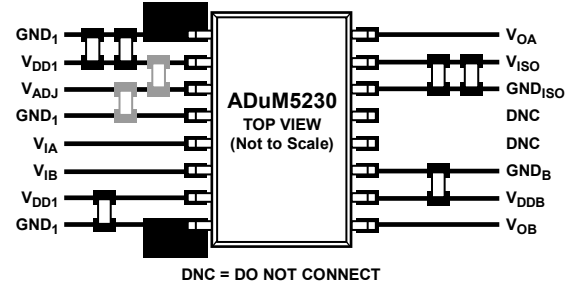


*Figure 15. Recommended Printed Circuit Board Layout*

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this may cause voltage differentials between pins exceeding the absolute maximum ratings specified in Table 6, leading to latch-up and/or permanent damage.

The ADuM5230 is a power device that dissipates about 1 W of power when fully loaded and run at maximum speed. Because it is not possible to apply a heat sink to an isolation device, the device primarily depends on heat dissipation into the PCB through the GND pins. If the device is used at high ambient temperatures, care should be taken to provide a thermal path from the GND pins to the PCB ground plane. The board layout in Figure 15 shows enlarged pads for Pin 1 and Pin 8. Implement multiple vias from the pad to the ground plane, which significantly reduce the temperatures inside the chip. The dimensions of the expanded pads are left to the discretion of the designer and the available board space.

## THERMAL ANALYSIS

The ADuM5230 part consists of several internal die attached to three lead frames, each with a die attach paddle. For the purposes of thermal analysis, the device is treated as a thermal unit with the highest junction temperature reflected in the $\theta_{JA}$ parameter shown in Table 2. The value of $\theta_{JA}$ is based on measurements taken with the part mounted on a JEDEC standard four-layer board with fine width traces and still air. Under normal operating conditions, the ADuM5230 operates at full load across the full temperature range without derating the output current. However, following the recommendations in the Printed Circuit Board (PCB) Layout section decreases the thermal resistance to the PCB, allowing increased thermal margin in high ambient temperatures.

Under output short-circuit conditions, as shown in Figure 12, the package power dissipation is within safe operating limits; however, if the load is in the 100 Ω range, power dissipation is high enough to cause thermal damage when the ambient temperature is above 80°C. Care should be taken to avoid excessive nonshort loads if the part is to be operated at high temperatures.

## PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high.
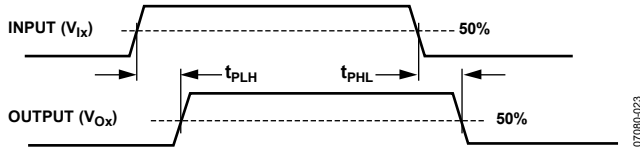


*Figure 16. Propagation Delay Parameters*

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM5230 component.

## DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1 μs, a periodic set of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5 μs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 9) by the watchdog timer circuit.

The limitation on the ADuM5230 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2; \; n = 1, 2, \ldots, N$$

where:
$\beta$ is the magnetic flux density (gauss).
$r_n$ is the radius of the $n^{th}$ turn in the receiving coil (cm).
$N$ is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM5230 and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 17.
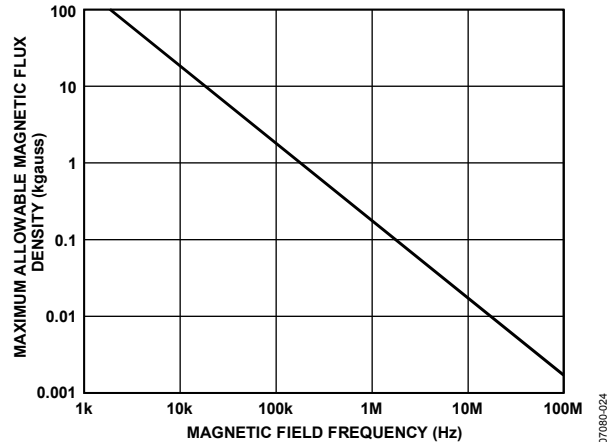


*Figure 17. Maximum Allowable External Magnetic Flux Density*

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM5230 transformers. Figure 18 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM5230 is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, the user would have to place a 0.5 kA current 5 mm away from the ADuM5230 to affect the operation of the component.
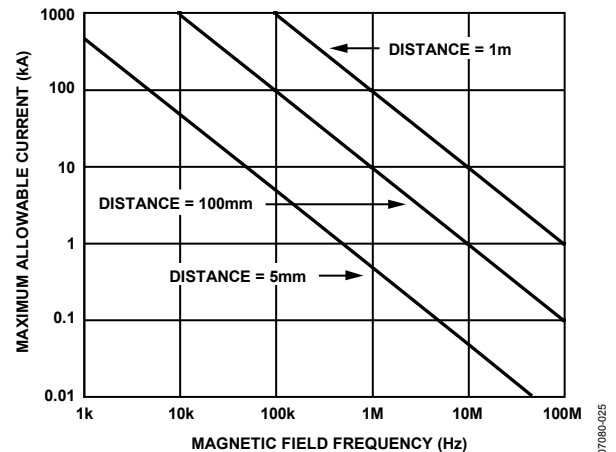


*Figure 18. Maximum Allowable Current
for Various Current-to-ADuM5230 Spacings*

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces may induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility.

## POWER CONSUMPTION

The power converter in the ADuM5230 provides 13 mA of power to the secondary in its default configuration. Power is provided to both the data channel, $V_{OA}$, and the $V_{ISO}$ pin for off-chip use. Current consumption of $V_{OA}$ varies with frequency as shown in Figure 8. The maximum available power for external use decreases as the frequency of the data channel increases to stay within the total available current.

## INCREASING AND DECREASING AVAILABLE POWER

The $V_{ADJ}$ pin is used to increase or decrease the available power at the $V_{ISO}$ pin. This allows the increase of the $V_{ISO}$ voltage for a given load or the increase of the maximum $V_{ISO}$ load. Alternatively, power can also be reduced when it is not required at the output, lowering the quiescent current and saving power.

Power adjustment is accomplished by adding a voltage divider between $V_{ADJ}$, $V_{DD1}$, and GND, as shown in Figure 25. Under normal operation, the $V_{ADJ}$ pin is left open, allowing the internal bias network to set the duty factor of the internal PWM. If the $V_{ADJ}$ pin is connected via a resistor divider, a duty factor other than the default can be chosen. The relationship between the duty factor of the internal PWM and the available power under

load is shown in Figure 13. When the desired duty factor is chosen, the values of the upper and lower divider resistors can be chosen as shown in Figure 14, which assumes a 10 kΩ total divider resistance.

## COMMON-MODE TRANSIENT IMMUNITY

In general, common-mode transients consist of linear and sinusoidal components. The linear component of a common-mode transient is given by

$$V_{CM, linear} = (\Delta V/\Delta t)\, t$$

where $\Delta V/\Delta t$ is the slope of the transient shown in Figure 19 and Figure 20.

The transient of the linear component is given by

$$dV_{CM}/dt = \Delta V/\Delta t$$

The ability of the ADuM5230 to operate correctly in the presence of linear transients is characterized by the data in Figure 22. The data is based on design simulation and is the maximum linear transient magnitude that the ADuM5230 can tolerate without an operational error. This data shows a higher level of robustness than what is shown in Table 1 because the transient immunity values obtained in Table 1 use measured data and apply allowances for measurement error and margin.
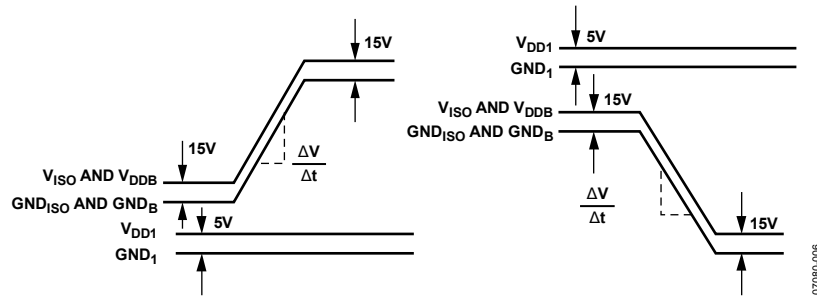


Figure 19. Common-Mode Transient Immunity Waveforms, Input to Output
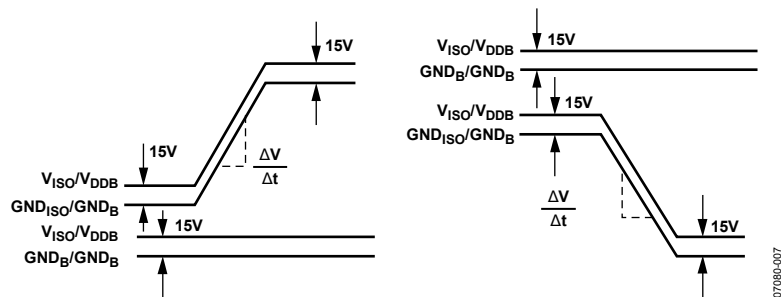


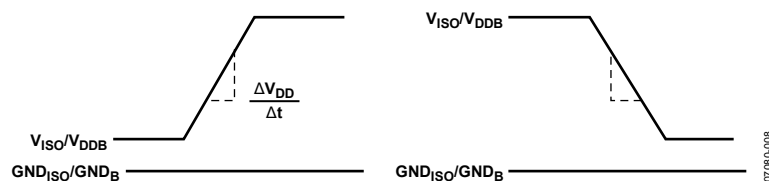Figure 20. Common-Mode Transient Immunity Waveforms Between Outputs



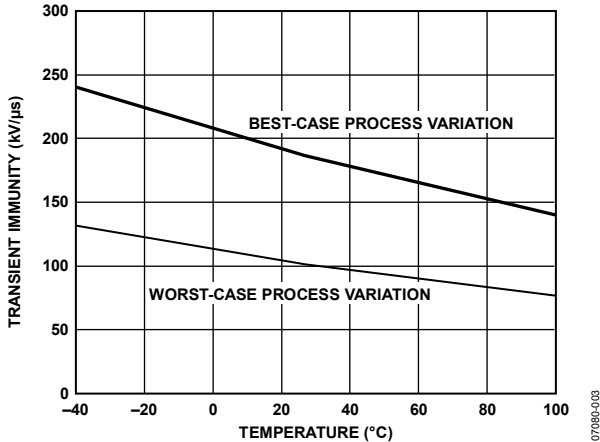Figure 21. Transient Immunity Waveforms, Output Supplies

Figure 22. Transient Immunity (Linear Transients) vs. Temperature

The sinusoidal component (at a given frequency) is given by

$$V_{CM, sinusoidal} = V_0 \sin(2\pi ft)$$

where:
$V_0$ is the magnitude of the sinusoidal.
$f$ is the frequency of the sinusoidal.

The transient magnitude of the sinusoidal component is given by

$$dV_{CM}/dt = 2\pi f \, V_0$$

The ability of the ADuM5230 to operate correctly in the presence of sinusoidal transients is characterized by the data in Figure 23 and Figure 24. The data is based on design simulation and is the maximum sinusoidal transient magnitude ($2\pi f \, V_0$) that the ADuM5230 can tolerate without an operational error. Values for immunity against sinusoidal transients are not included in Table 1 because measurements to obtain such values have not been possible.
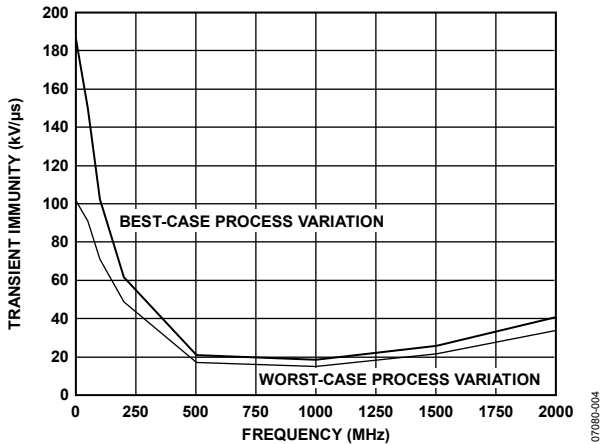


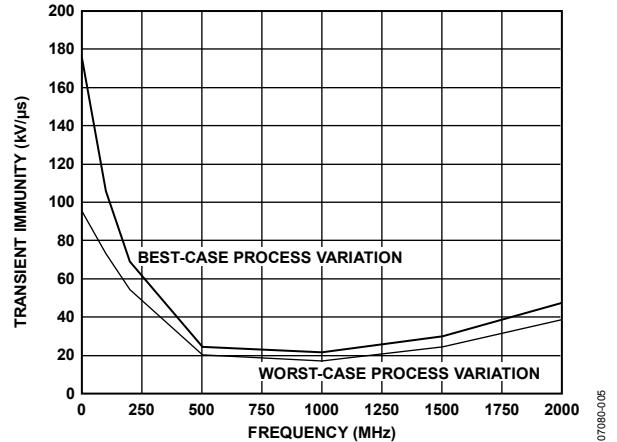Figure 23. Transient Immunity (Sinusoidal Transients), 27°C Ambient Temperature



Figure 24. Transient Immunity (Sinusoidal Transients), 100°C Ambient Temperature

## TYPICAL APPLICATION USAGE

The ADuM5230 is intended for driving low gate capacitance transistors (200 pF typically). Most high voltage applications involve larger transistors than this. To accommodate these applications, users can implement a buffer configuration with the ADuM5230, as shown in Figure 25. In many cases, the buffer configuration is the least expensive option and provides the greatest amount of design flexibility. The precise buffer/high voltage transistor combination can be selected to fit the needs of the application.
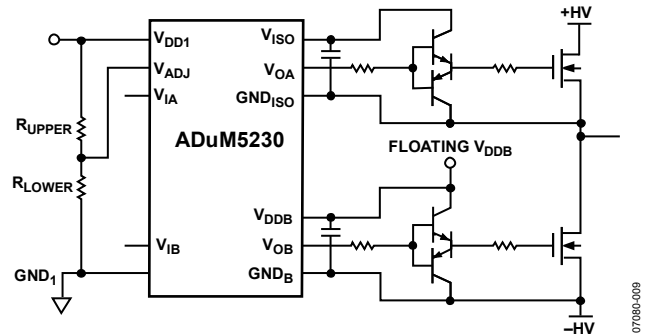


Figure 25. Application Circuit

## INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation depends on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM5230.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. Table 7 summarizes the peak voltages for 50 years of service life for a bipolar ac operating condition and the maximum Analog Devices recommended working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM5230 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 26, Figure 27, and Figure 28 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 7 can be applied while maintaining the 50-year minimum lifetime, provided the voltage conforms to either the unipolar ac or dc voltage cases. Treat any cross-insulation voltage waveform that does not conform to Figure 27 or Figure 28 as a bipolar ac waveform, and limit its peak voltage to the 50-year lifetime voltage value listed in Table 7. Note that the voltage presented in Figure 27 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.
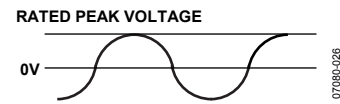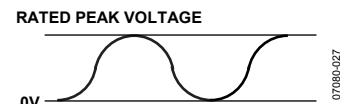


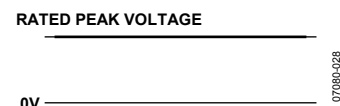*Figure 26. Bipolar AC Waveform*
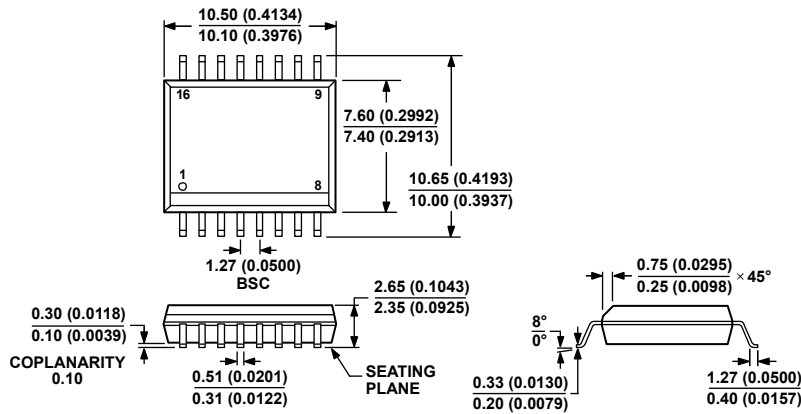


*Figure 27. Unipolar AC Waveform*



*Figure 28. DC Waveform*

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

*Figure 29. 16-Lead Standard Small Outline Package [SOIC_W]*
*Wide Body*
*(RW-16)*
*Dimensions shown in millimeters and (inches)*

## ORDERING GUIDE

| Model[1, 2] | No. of Channels | Output Peak Current (A)[3] | Output Voltage (V) | Temperature Range | Package Description | Package Option |
|---|---|---|---|---|---|---|
| ADuM5230ARWZ | 2 | 0.1/0.3 | 15 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM5230ARWZ-RL | 2 | 0.1/0.3 | 15 | −40°C to +105°C | 16-Lead SOIC_W, 13-Inch Tape and Reel Option (1,000 Units) | RW-16 |
| ADuM5230WARWZ | 2 | 0.1/0.3 | 15 | −40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM5230WARWZ-RL | 2 | 0.1/0.3 | 15 | −40°C to +105°C | 16-Lead SOIC_W, 13-Inch Tape and Reel Option (1,000 Units) | RW-16 |

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] Sourcing/sinking.

## AUTOMOTIVE PRODUCTS

The ADuM5230W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

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