

## DESCRIPTION

The MPQ6400 family is the microprocessor ( $\mu$ P) supervisory circuit which can monitor and provide reset function for system voltages from 0.4V. When either the SENSE voltage falls below its threshold ( $V_{IT}$ ) or the voltage of manual reset ( $\overline{MR}$ ) is pulled to a logic low, the  $\overline{RESET}$  signal will be asserted. The reset voltage can be factory-set for standard voltage rails from 0.9V to 5V, while the MPQ6400DG-01 reset voltage is adjustable with an external resistor divider. When SENSE voltage and  $\overline{MR}$  exceed their thresholds,  $\overline{RESET}$  is driven to a logic high after a user-programmable delay time.

The MPQ6400 has a very low quiescent current of 1.6 $\mu$ A typically, which makes it ideal suitable for battery-powered applications. It provides a precision reference to achieve  $\pm 1\%$  threshold accuracy. The reset delay time can be selected by a capacitor which is connected between  $C_{DELAY}$  and GND, allowing the user to select any delay time from 2.1ms to 10s. 380ms delay time is selected by connecting the  $C_{DELAY}$  pin to  $V_{CC}$ , while 24ms delay time by leaving the  $C_{DELAY}$  pin float. MPQ6400 is available in 2mm $\times$ 2mm 6-pin QFN package.

## FEATURES

- Guaranteed Industrial/Automotive Temp Range Limits
- Fixed Threshold Voltages for Standard Voltage Rails From 0.9V to 5V and Adjustable Voltage From 0.4V are Available
- Low Quiescent Current: 1.6 $\mu$ A Typ
- Power-On Reset Generator with Adjustable Delay Time: 2.1ms to 10s
- High Threshold Accuracy:  $\pm 1\%$  Typ
- Manual Reset ( $\overline{MR}$ ) Input
- Open-Drain  $\overline{RESET}$  Output
- Immune to Short Negative SENSE Voltage
- Guaranteed Reset Valid to  $V_{CC}=0.8V$
- 2 $\times$ 2mm QFN
- AEC-Q100 Qualified

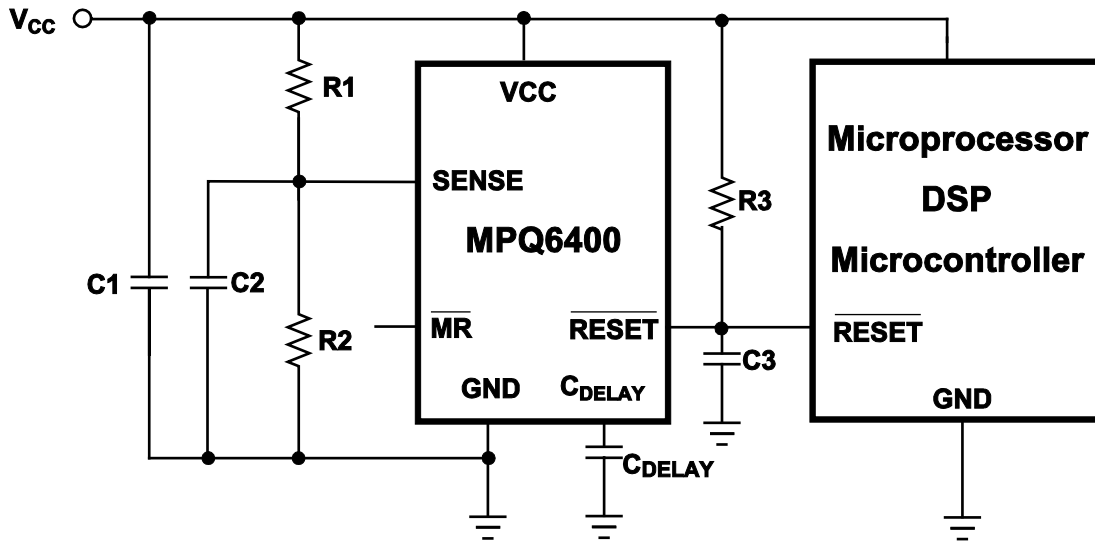
## APPLICATIONS

- DSP or Micro controller Applications
- Laptop/Desktop Computers
- PDAs/Hand-Held Products
- Portable/Battery-Powered Products
- FPGA/ASIC Applications

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## TYPICAL APPLICATION



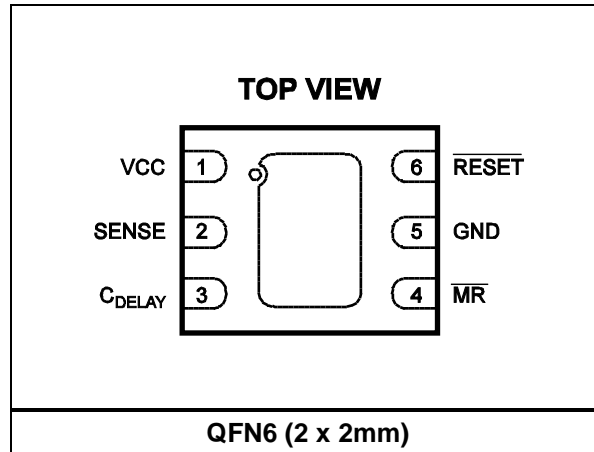
## ORDERING INFORMATION

Part Number*	Package	T <sub>J</sub>
MPQ6400DG-33**	QFN6 (2x2mm)	-40°C to +125°C
MPQ6400DG-33-AEC1	QFN6 (2x2mm)	-40°C to +125°C

\*For Tape & Reel, add suffix -Z (e.g. MPQ6400DG-XX-Z);  
 For RoHS compliant packaging, add suffix -LF (e.g. MPQ6400DG-XX-LF-Z).

\*\* Check factory for availability in other options.

## PACKAGE REFERENCE



### ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

Supply Voltage V <sub>CC</sub> .....	-0.3 to 6.0V
C <sub>DELAY</sub> Voltage V <sub>CDELAY</sub> .....	-0.3V to V <sub>CC</sub> + 0.3V
SENSE Voltage V <sub>SENSE</sub> .....	-0.3V to 6V
All Other Pins.....	-0.3V to +6.0V
RESET Current I <sub>RESET</sub> .....	5mA
Continuous Power Dissipation (T <sub>A</sub> = +25°C) <sup>(2)</sup>	
QFN6 (2mmx2mm) .....	2.5W
Junction Temperature .....	150°C
Lead Temperature .....	260°C
Storage Temperature.....	-65°C to +150°C

### Recommended Operating Conditions <sup>(3)</sup>

Supply Voltage V <sub>CC</sub> .....	1.8V to 5.5V
Maximum Junction Temp. (T <sub>J</sub> ) .....	+125°C

Thermal Resistance <sup>(4)</sup>	$\theta_{JA}$	$\theta_{JC}$
QFN6 (2x2mm) .....	50	12 ... °C/W

#### Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub>(MAX), the junction-to-ambient thermal resistance  $\theta_{JA}$ , and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub>(MAX)=(T<sub>J</sub>(MAX)-T<sub>A</sub>)/ $\theta_{JA}$ . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- The device is not guaranteed to function outside of its operating conditions.
- Measured on JESD51-7 4-layer board.

## ELECTRICAL CHARACTERISTICS

1.8V ≤ V<sub>CC</sub> ≤ 5.5V, R<sub>3</sub> = 100kΩ, C<sub>3</sub> = 47pF, T<sub>J</sub> = -40°C to +125°C, Typical values are at T<sub>J</sub> = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply Range	V <sub>CC</sub>		1.8		5.5	V
Supply Current (current into V <sub>CC</sub> pin)	I <sub>CC</sub>	V <sub>CC</sub> = 3.3V, $\overline{\text{RESET}}$ not asserted, $\overline{\text{MR}}$ , $\overline{\text{RESET}}$ , C <sub>DELAY</sub> open		1.6	5	μA
		V <sub>CC</sub> = 5.5V, $\overline{\text{RESET}}$ not asserted, $\overline{\text{MR}}$ , $\overline{\text{RESET}}$ , C <sub>DELAY</sub> open		1.85	15	μA
Low-level Output Voltage	V <sub>OL</sub>	1.3V ≤ V <sub>CC</sub> < 1.8V, I <sub>OL</sub> = 0.4mA			0.3	V
		1.8V ≤ V <sub>CC</sub> ≤ 5.5V, I <sub>OL</sub> = 1.0mA			0.4	V
Power-up Reset Voltage <sup>(5)</sup>		V <sub>OL</sub> (max) = 0.2V, I <sub>RESET</sub> = 15μA, T <sub>rise(V<sub>CC</sub>)</sub> ≥ 15μs/V			0.8	V
Negative-going Input Threshold Accuracy <sup>(7)</sup>	V <sub>IT</sub>	-40°C to +85°C	-2.5	±1.0	1.5	%
		-40°C to +125°C	-3		1.7	
Hysteresis on V <sub>IT</sub> Pin	V <sub>HYS</sub>			1.5	4	V <sub>IT</sub> %
$\overline{\text{MR}}$ Internal Pull-up Resistance	R <sub>MR</sub>		50	110		kΩ
Input Current at SENSE Pin	I <sub>SENSE</sub>	Fixed versions V <sub>SENSE</sub> = 6V		2.4		μA
$\overline{\text{RESET}}$ Leakage Current		V <sub>RESET</sub> = 5.5V, $\overline{\text{RESET}}$ not asserted			500	nA
$\overline{\text{MR}}$ Logic Low Input	V <sub>IL</sub>				0.25V <sub>CC</sub>	V
$\overline{\text{MR}}$ Logic High Input	V <sub>IH</sub>		0.7V <sub>CC</sub>			V
SENSE Maximum Transient Duration	t <sub>w</sub>	V <sub>IH</sub> = 1.05 V <sub>IT</sub> , V <sub>IL</sub> = 0.95 V <sub>IT</sub>		17.5		μs
$\overline{\text{RESET}}$ Delay Time	t <sub>d</sub>	C <sub>DELAY</sub> = Open	15	24	34	ms
		C <sub>DELAY</sub> = V <sub>CC</sub> <sup>(6)</sup>	230	380	530	ms
		C <sub>DELAY</sub> = 150pF	1.3	2.1	3	ms
		C <sub>DELAY</sub> = 10nF <sup>(6)</sup>	61	102	142	ms
$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ Propagation Delay	t <sub>pHL1</sub>	V <sub>IH</sub> = 0.7 V <sub>CC</sub> , V <sub>IL</sub> = 0.25 V <sub>CC</sub>		160		ns
High to Low Level $\overline{\text{RESET}}$ Delay, SENSE to $\overline{\text{RESET}}$	t <sub>pHL2</sub>	V <sub>IH</sub> = 1.05 V <sub>IT</sub> , V <sub>IL</sub> = 0.95 V <sub>IT</sub>		17.5		μs

**Note:**

- 5) The lowest supply voltage (V<sub>CC</sub>) at which  $\overline{\text{RESET}}$  becomes active.
- 6) Guaranteed by design.
- 7) V<sub>SENSE</sub> Falling Slowly

## ORDERING INFORMATION

Product	Package	Top Mark	Nominal Supply Voltage	Threshold Voltage (VIT)
MPQ6400DG-33	QFN		3.3V	3.07V

## PIN FUNCTIONS

QFN Pin #	Name	Description
1	V <sub>CC</sub>	Supply voltage. A 0.1uF decoupling ceramic capacitor should be put close to this pin.
2	SENSE	SENSE pin is connected to the monitored system voltage. When the monitored voltage is below desired threshold, $\overline{\text{RESET}}$ is asserted.
3	C <sub>DELAY</sub>	Programmable reset delay time pin. When C <sub>DELAY</sub> connected to V <sub>CC</sub> through a resistor between 50kΩ and 200kΩ, a 380ms delay time is selected. When C <sub>DELAY</sub> floated, the delay time is 24ms. A capacitor bigger than 150pF connected C <sub>DELAY</sub> to GND could be used to get the user's programmable time from 2.1ms to 10s.
4	$\overline{\text{MR}}$	The manual reset ( $\overline{\text{MR}}$ ) can introduce another logic signal to control the $\overline{\text{RESET}}$ . It is internally connected to V <sub>CC</sub> through a 90kΩ resistor.
5	GND	Ground.
6	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ is an open drain signal which will be asserted when the SENSE voltage drops below a preset threshold or when the manual reset ( $\overline{\text{MR}}$ ) pin drops to a logic low. The $\overline{\text{RESET}}$ delay time is programmable from 2.1ms to 10s by using external capacitors. A pull-up resistor bigger than 10k should be connected this pin to supply line, and the $\overline{\text{RESET}}$ outputting a higher voltage than V <sub>CC</sub> is allowable.

## DETAIL DESCRIPTION

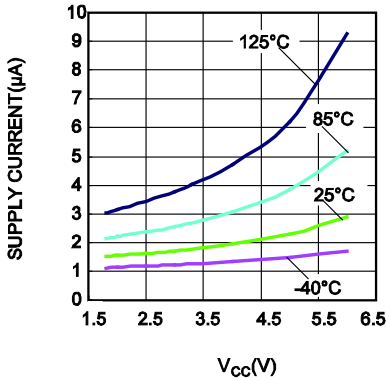
The MPQ6400 product family asserts a  $\overline{\text{RESET}}$  signal when either the SENSE pin voltage is lower than V<sub>IT</sub> or the manual reset ( $\overline{\text{MR}}$ ) is driven low. The MPQ6400-XX family, other than the MPQ6400DG-01, can monitor a fixed voltage from 0.9V to 5.0V. The MPQ6400DG-01 can monitor any voltage above 0.4V by adjusting the external resistor divider. After both the manual reset ( $\overline{\text{MR}}$ ) and SENSE voltages exceed their thresholds, the  $\overline{\text{RESET}}$

output remains asserted for a user's programmable delay time. Two fixed  $\overline{\text{RESET}}$  delay times are user-selectable: 380ms delay time by connecting the C<sub>DELAY</sub> pin to V<sub>CC</sub>, and 24ms delay time by leaving the C<sub>DELAY</sub> pin float. Any delay time from 2.1ms to 10s could be gotten by connecting a capacitor between C<sub>DELAY</sub> and GND. The wide monitor voltage and programmable reset delay time make MPQ6400 product family suitable for a broad array of applications.

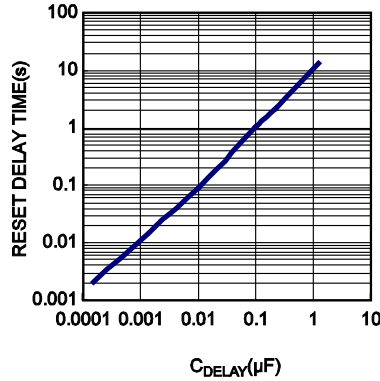
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC}=3.3V$ ,  $R_3 = 100k\Omega$ ,  $C_3 = 47pF$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ , Typical values are at  $T_A=+25^\circ C$ , unless otherwise noted.

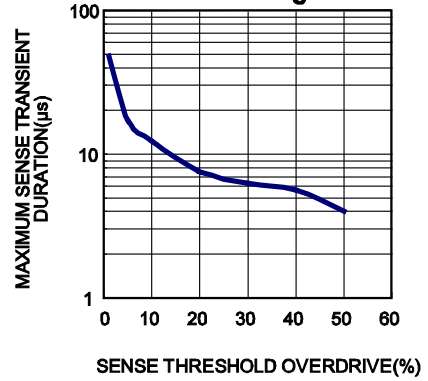
**Supply Current vs.  $V_{CC}$**



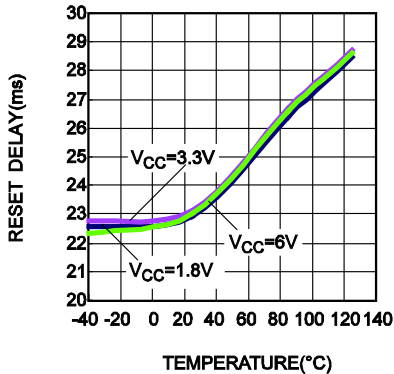
**Reset Delay Time vs.  $C_{DELAY}$**



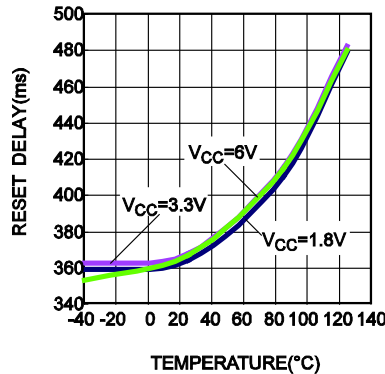
**Maximum SENSE Transient Duration vs. SENSE Threshold Overdrive Voltage**



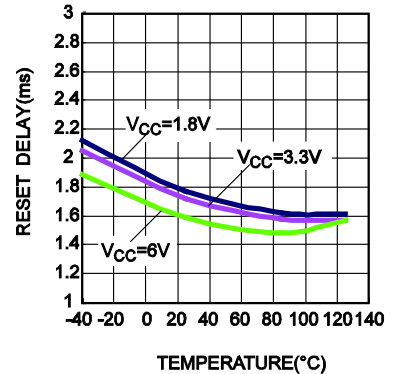
**Reset Delay vs. Temperature ( $C_{DELAY}=open$ )**



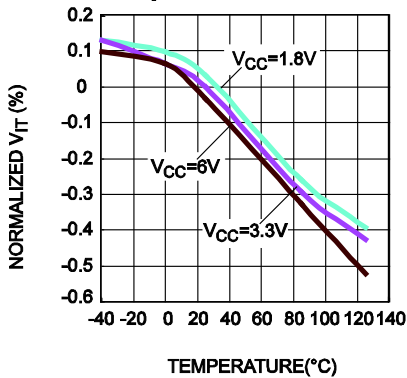
**Reset Delay vs. Temperature ( $C_{DELAY}=V_{CC}$ )**



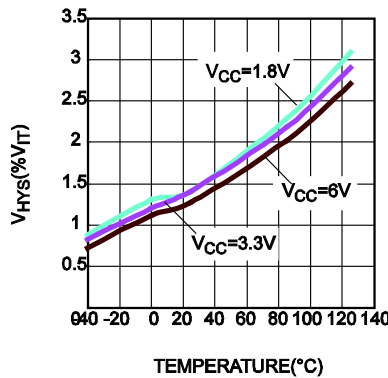
**Reset Delay vs. Temperature ( $C_{DELAY}=150pF$  Cap)**



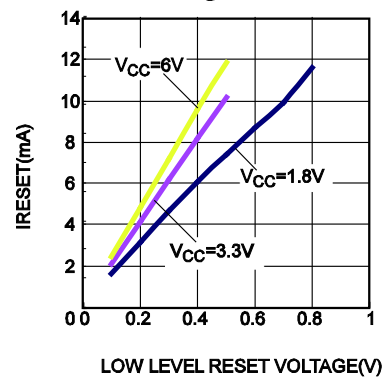
**Normalized  $V_{IT}$  vs. Temperature**



**$V_{HYS}$  vs. Temperature**



**$I_{RESET}$  vs. Low Level Reset Voltage**



## FUNCTIONAL BLOCK DIAGRAM

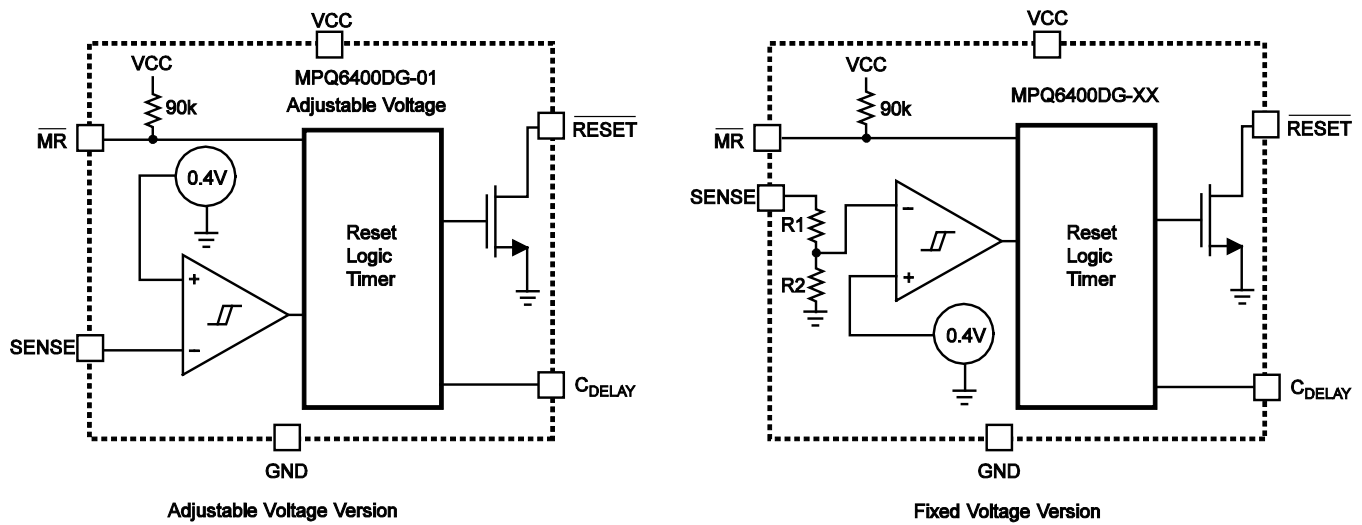


Figure 1—Functional Block Diagram

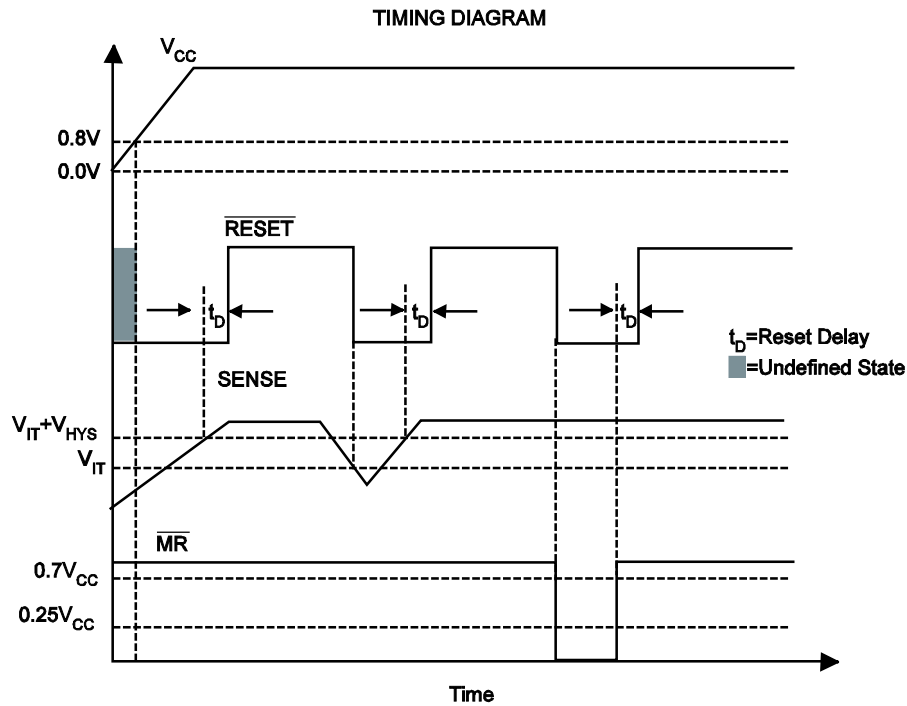


Figure 2—MPQ6400 Timing Diagram

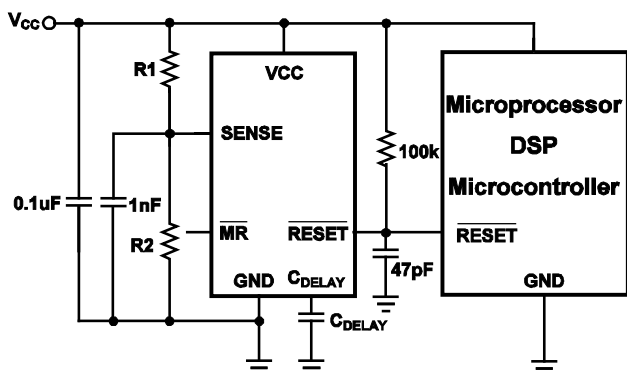
### TRUTH TABLE

$\overline{\text{MR}}$	$\text{SENSE} > V_{\text{IT}}$	$\overline{\text{RESET}}$
L	0	L
L	1	L
H	0	L
H	1	H

## APPLICATION INFORMATION

### Reset Output Function

The MPQ6400  $\overline{\text{RESET}}$  output is typically connected to the  $\overline{\text{RESET}}$  input of a microprocessor, as shown in Figure 3. When  $\overline{\text{RESET}}$  is not asserted, a pull up resistor must be connected to hold this signal high. The voltage of reset signal is allowed to be higher than  $V_{CC}$  (up to 6V) through a resistor pulling up from supply line. If the voltage is below 0.8V,  $\overline{\text{RESET}}$  output is undefined. This condition can be ignored generally because that most microprocessors do not function at this state. When both SENSE and  $\overline{\text{MR}}$  are higher than their threshold voltage,  $\overline{\text{RESET}}$  output holds logic high. Once either of the two drops below their threshold,  $\overline{\text{RESET}}$  will be asserted.



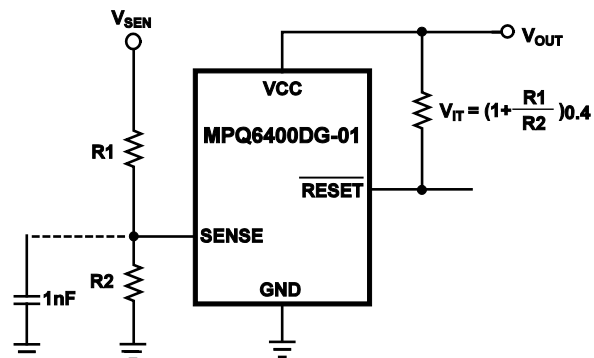
**Figure 3—Typical Application of MPQ6400 with Microprocessor**

From the point that  $\overline{\text{MR}}$  is again logic high and SENSE is above  $V_{IT} + V_{HYS}$  (the threshold hysteresis),  $\overline{\text{RESET}}$  will be driven to a logic high after a reset delay time. The reset delay time is programmable by  $C_{DELAY}$  pin. Due to the finite impedance of  $\overline{\text{RESET}}$  pin, the pull up resistor should be bigger than 10k $\Omega$ .

### Monitor a Voltage

The SENSE input pin is connected to the monitored system voltage directly or through a resistor network (on MPQ6400DG-01). When the voltage on the pin is below  $V_{IT}$ ,  $\overline{\text{RESET}}$  is asserted. A threshold hysteresis will prevent the chip from responding perturbation on SENSE pin. A 1nF to 10nF bypass capacitor should be put on this pin to increase its immunity to noise. A typical application of the MPQ6400DG-01 is shown in Figure 4. Two external resistors form a voltage

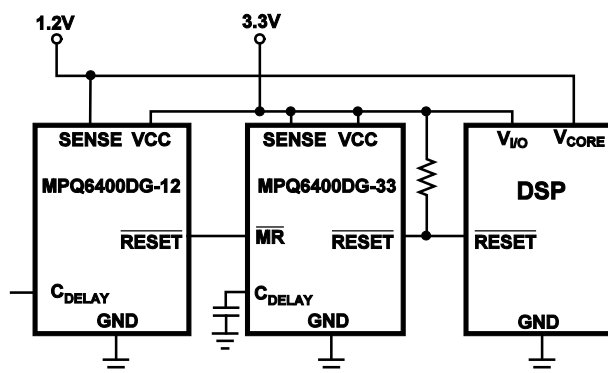
divider from monitored voltage to GND. Its tap connects to the SENSE pin. The circuit can be used to monitor any voltage higher than 0.4V.



**Figure 4—MPQ6400DG-01 Monitoring a User-Defined Voltage**

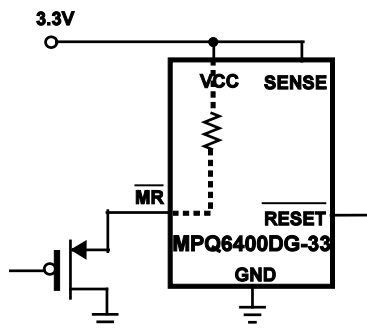
### Monitor Multiple System Voltages

The manual reset ( $\overline{\text{MR}}$ ) can introduce another logic signal to control the  $\overline{\text{RESET}}$ . When  $\overline{\text{MR}}$  is a logic low ( $0.25V_{CC}$ ),  $\overline{\text{RESET}}$  will be asserted. After both SENSE and  $\overline{\text{MR}}$  are above their thresholds,  $\overline{\text{RESET}}$  will be driven to a logic high after a reset delay time. The  $\overline{\text{MR}}$  is internally connected to  $V_{CC}$  through a 90k $\Omega$  resistor so this pin can float. See how multiple system voltages are monitored by  $\overline{\text{MR}}$  in Figure 5. If the signal on  $\overline{\text{MR}}$  isn't up to  $V_{CC}$ , there will be an additional current through internal 90k $\Omega$  pull up resistor. A logic-level FET can be used to minimize the leakage, as shown in Figure 6.



**Figure 5—MPQ6400 Family Monitoring Multiple System Voltages**

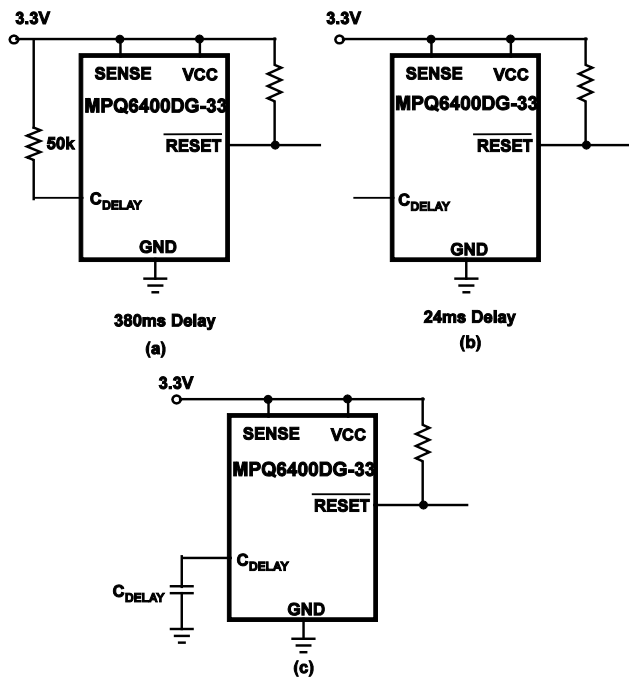




**Figure 6—Minimizing  $I_{CC}$  When  $\overline{MR}$  Signal isn't over  $V_{CC}$  by External MOSFET**

**Programmable Reset Delay Time**

The reset delay time can be programmed by  $C_{DELAY}$  configure. When  $C_{DELAY}$  is connected to  $V_{CC}$  through a resistor between 50kΩ and 200kΩ, the delay time is 380ms. When  $C_{DELAY}$  floated, the delay time is 24ms. In addition, a capacitor connected  $C_{DELAY}$  to GND could be used to get the user's programmable delay time from 2.1ms to 10s. The three configures can be found in Figure 7(a)(b)(c).



**Figure 7—Programmable Configurations to the Reset Delay Time**

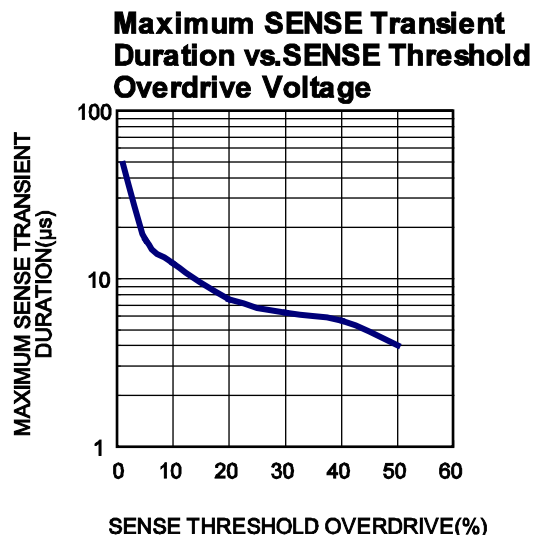
The external capacitor  $C_{DELAY}$  must be larger than 150pF. For a given delay time, the capacitor value can be calculated using the following equation:

$$C_{DELAY} \text{ (nF)} = [t_D \text{ (s)} - 4.99 \times 10^{-4} \text{ (s)}] \times 107$$

The reset delay time is determined by the charge time of external capacitor. While SENSE is above  $V_{IT}$  and  $\overline{MR}$  is a logic high, the internal 140nA current source is enabled and starts to charge the capacitor to set the delay time. When the capacitor voltage rises to 1.13V, the  $\overline{RESET}$  is de-asserted. The capacitor will be discharged when the  $\overline{RESET}$  is again asserted. Stray capacitance may cause errors of the delay time. A ceramic capacitor with low leakage is strongly recommended.

**SENSE Voltage Transients Immunity**

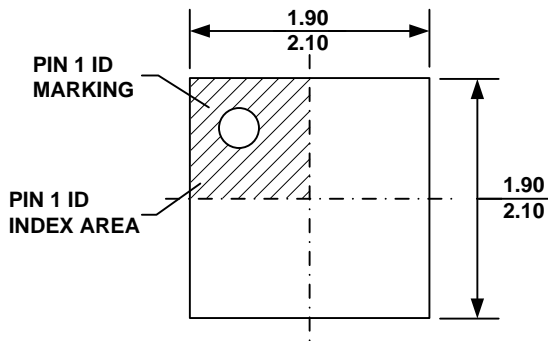
The MPQ6400 can be immune to SENSE pin short negative transient. The maximum immune duration is 17us while overdrive is 5%. A shorter negative transient can not assert the  $\overline{RESET}$  output. The effective duration is relative to the threshold overdrive, as shown in Figure 8.



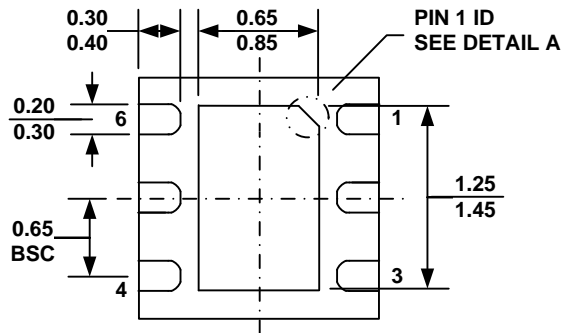
**Figure 8—Maximum Transient Duration vs. Sense Threshold Overdrive Voltage**

**PACKAGE INFORMATION**

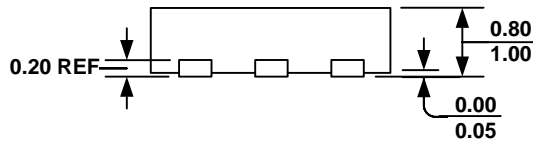
**QFN6 (2 x 2mm)**



**TOP VIEW**

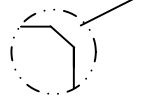


**BOTTOM VIEW**

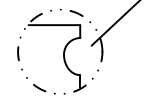


**SIDE VIEW**

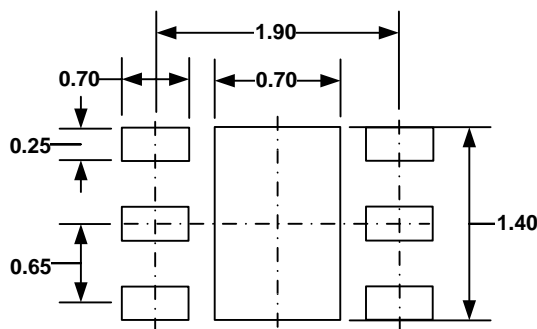
**PIN 1 ID OPTION A**  
0.30x45° TYP.



**PIN 1 ID OPTION B**  
R0.20 TYP.



**DETAIL A**



**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) JEDEC REFERENCE IS MO-229, VARIATION VCCC.
- 5) DRAWING IS NOT TO SCALE.

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