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Panasonic Global Part Number AN30888A-VF

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Product Standards

Part No.	AN30888A
Package Code No.	SSOP016-P-0225E

Contents

AN30888A

High Brightness LED Driver IC

■ Overview

AN30888A is a Boost/Buck-Boost/Buck DCDC controller that drives an external power NMOS switch.
It is suitable for driving high brightness LED for LED lighting applications.

■ Features

- Battery operation : 3 V to 20 V
- Output current range : 0 A to a few Amperes depending on rating of external NMOS and mode of operation
- Current mode control architecture
- LED dimming function available by using PWM signal
- 30 mV / 200 mV reference voltage
- Low standby current
- Configurable as either Boost/Buck-Boost/ Buck mode converter
- Built-in various protection circuit : Under voltage lock out
  Over voltage protection
  Soft start function

■ Applications

- LED lighting module
- LED lantern applications
- White LED backlighting for LCD panel
- White LED flash light driving applications
- General LED back lighting

■ Package

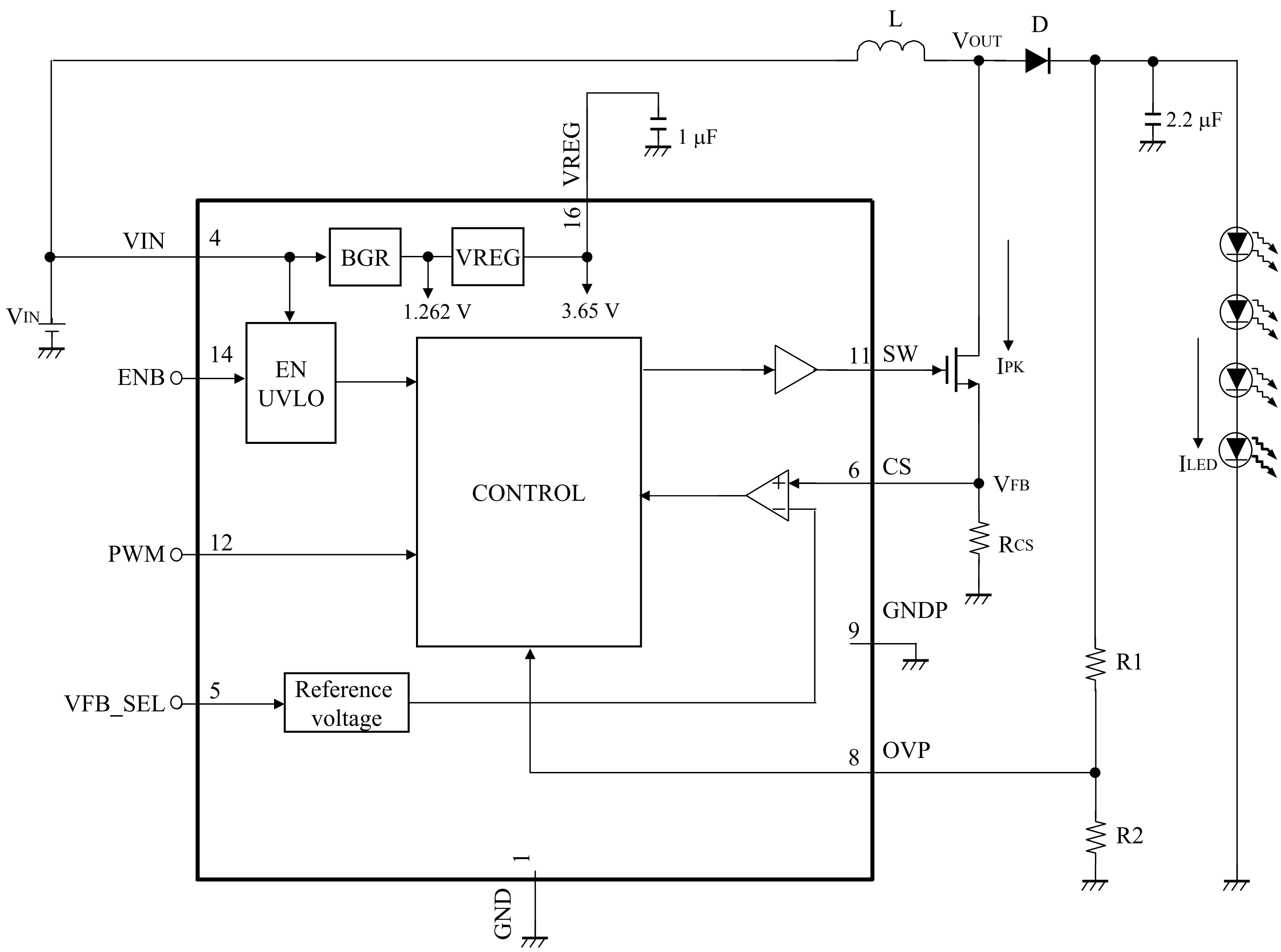
16 pin Plastic Shrink Small Outline Package (SSOP Type)

■ Type

- Bi–CMOS IC

■ Application Circuit Example (Block Diagram)

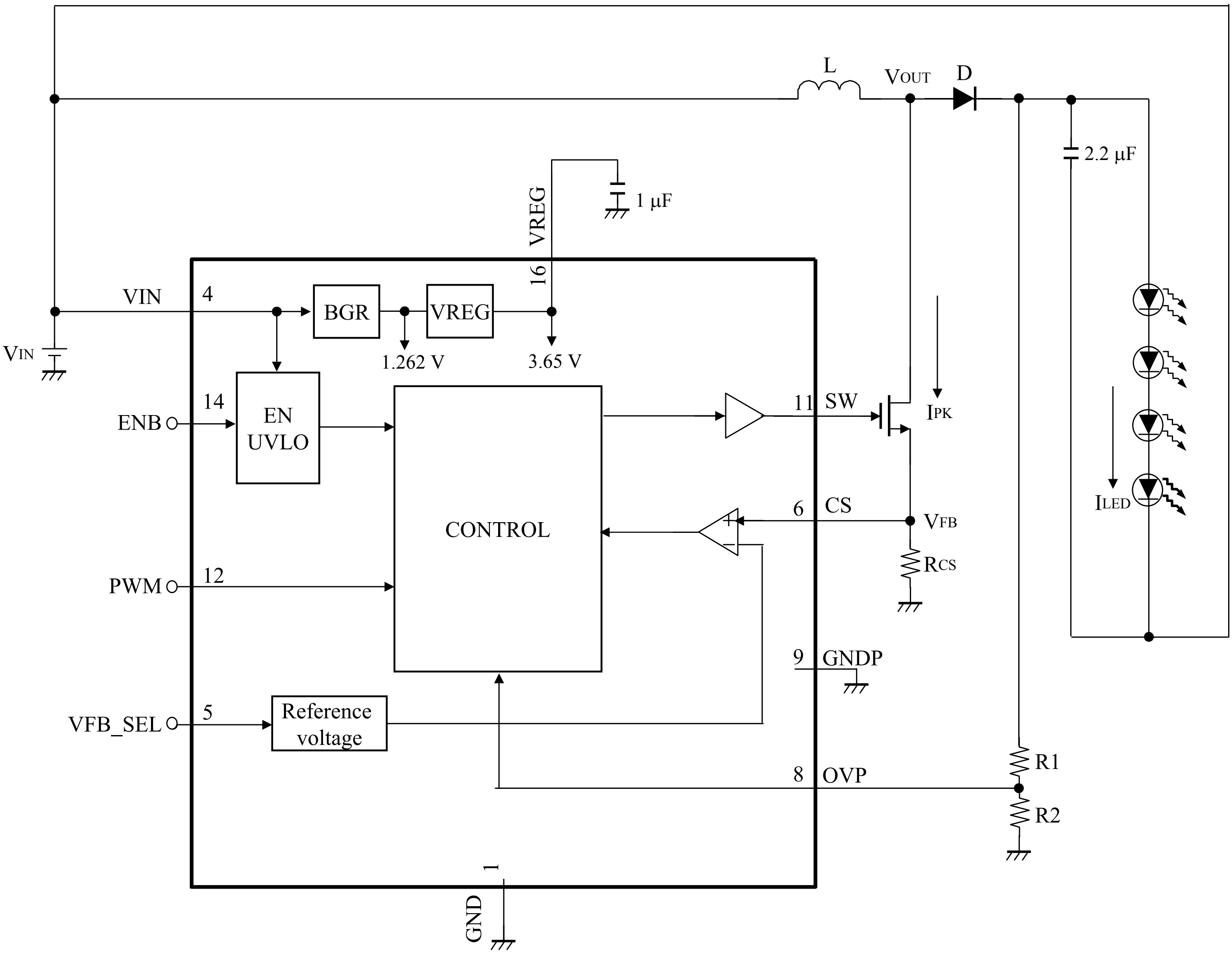
- Boost Mode



Notes)
- This application circuit is an example. The operation of mass production set is not guaranteed. You should perform enough evaluation and verification on the design of mass production set. You are fully responsible for the incorporation of the above application circuit and information in the design of your equipment.
- Use external resistor with ±1% accuracy at CS pin.
- Use ceramic type capacitor (Typ. 1 µF, Min. 0.5 µF) at VREG pin.
- Use schottky diode at VOUT.
- This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

■ Application Circuit Example (Block Diagram) (continued)

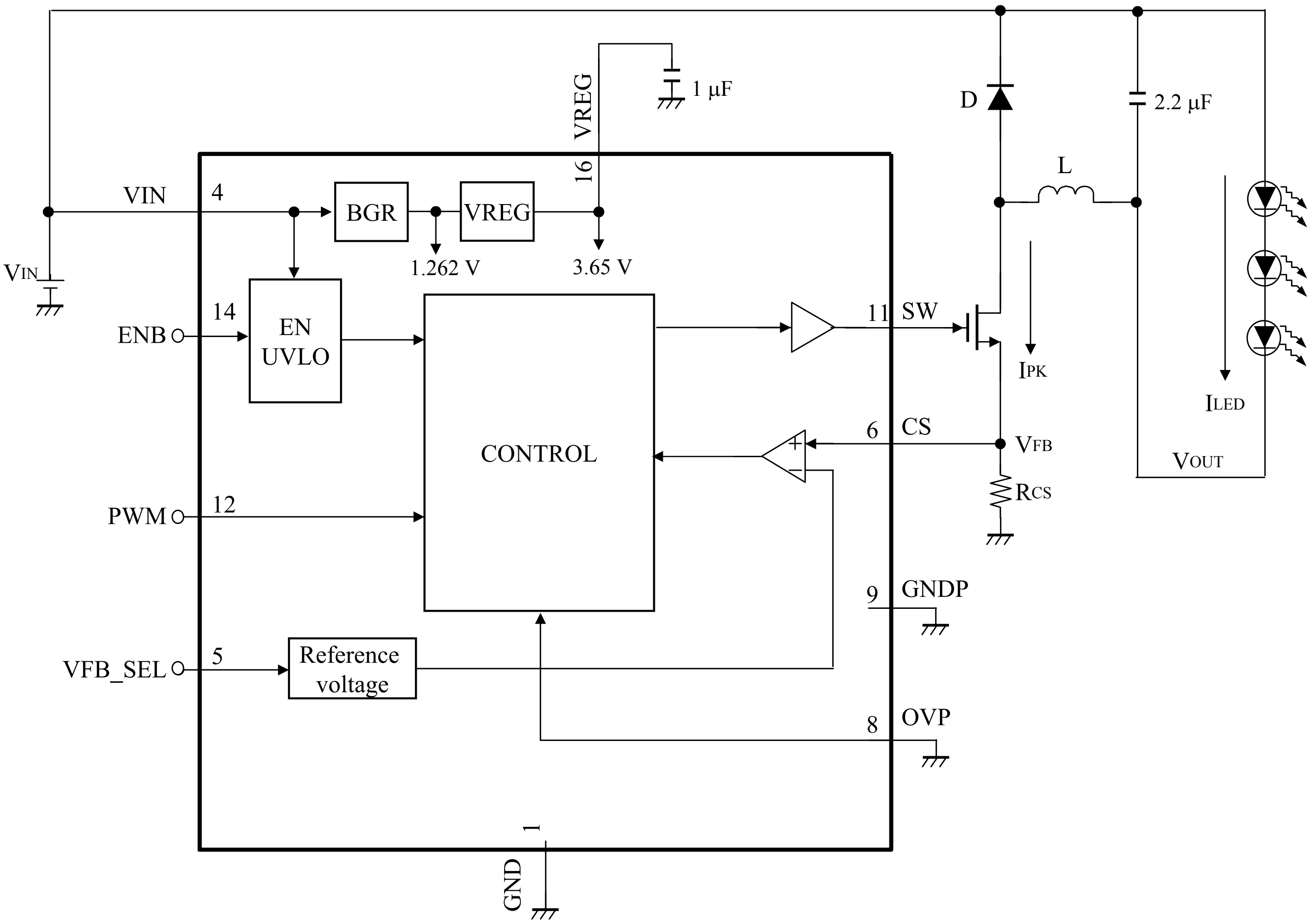
- Buck-Boost Mode



Notes)
- This application circuit is an example. The operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.
- Use external resistor with ±1% accuracy at CS pin.
- Use ceramic type capacitor (Typ. 1 µF, Min. 0.5 µF) at VREG pin.
- Use schottky diode at VOUT.
- This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

■ Application Circuit Example (Block Diagram) (continued)

- Buck Mode



Notes)
- This application circuit is an example. The operation of mass production set is not guaranteed. Perform enough evaluation and verification on the design of mass production set.
- Use external resistor with ±1% accuracy at CS pin.
- Use ceramic type capacitor (Typ. 1 µF, Min. 0.5 µF) at VREG pin.
- Use schottky diode at VOUT.
- This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	GND	Ground	Ground
2	N.C.	—	—
3	N.C.	—	—
4	VIN	Power Supply	Power Supply of IC
5	VFB_SEL	Input	Feedback voltage select
6	CS	Input	Current Sense
7	N.C.	—	—
8	OVP	Input	Over Voltage Protection input pin for Boost mode; Connect to GND for Buck mode
9	GNDP	Ground	Power Ground
10	N.C.	—	—
11	SW	Output	External NMOS Transistor Gate Drive
12	PWM	Input	PWM Dimming Control
13	N.C.	—	—
14	ENB	Input	Standby On/Off Control
15	N.C.	—	—
16	VREG	Output	Regulator Output

■ Absolute Maximum Ratings

Note) Absolute maximum ratings are limit values which do not result in damages to this IC, and IC operation is not guaranteed at these limit values.

A No.	Parameter	Symbol	Rating	Unit	Notes
1	Supply voltage	V_{DD}	21	V	*1
2	GND pin current	I_{GND}	—	A	—
3	Power dissipation	P_D	135	mW	*2
4	Operating ambient temperature	T_{opr}	–25 to +85	°C	*3
5	Storage temperature	T_{stg}	–55 to +125	°C	*3

Notes) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : The power dissipation shown is the value at T_a = 85°C for the independent (unmounted) IC package without a heat sink. When using this IC, refer to the P_D-T_a diagram of the package standard and design the heat radiation with sufficient margin so that the allowable value might not be exceeded based on the conditions of power supply voltage, load, and ambient temperature.

*3 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for T_a = 25°C.

■ Operating Supply Voltage Range

Parameter	Symbol	Range	Unit	Notes
Supply voltage range	V_{IN}	3.0 to 20	V	*1
Supply voltage range (Boost Mode/Buck-Boost Mode)	V_{IN1}	3.0 to 12	V	*1
Supply voltage range (Buck Mode)	V_{IN2}	3.0 to 20	V	*1

Note) *1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

■ Allowable Voltage Range

Notes)
- Allowable current and voltage ranges are limit ranges which do not result in damages to this IC, and IC operation is not guaranteed within these limit ranges.
- Voltage values, unless otherwise specified, are with respect to GND.
- V_{IN} is voltage for VIN pin.
- Do not apply external currents or voltages to any pin not specifically mentioned.

Pin No.	Pin name	Rating	Unit	Note
4	VIN	–0.3 to 20	V	*1
5	VFB_SEL	–0.3 to 5.5	V	—
6	CS	–0.3 to V_{REG}	V	*2
8	OVP	–0.3 to V_{REG}	V	*2
11	SW	–0.3 to V_{REG}	V	*2
12	PWM	–0.3 to 5.5	V	*2
14	ENB	–0.3 to V_{IN}	V	*1
16	VREG	–0.3 to 4.3	V	*2

Notes) *1 : V_{IN} must not exceed 20 V.
*2 : V_{REG} must not exceed 4.3 V.

■ Electrical Characteristics at V_{IN} = 6 V, ENB = 6 V, PWM = V_{REG}

Note) T_a = 25°C±2°C / T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Notes
					Min	Typ	Max		
Circuit Current Consumption									
1	Standby Current	I_{STB}	1	ENB = 0 V	—	—	10	µA	—
2	Operating Quiescent Current	I_{CC}	1	ENB = V_{IN} No load condition	—	—	1	mA	—
ENABLE (ENB), VFB_SEL and PWM Control Function									
3	ENB High Input Logic	V_{ENBH}	1	—	3	—	V_{IN}	V	—
4	ENB Low Input Logic	V_{ENBL}	1	—	0	—	0.3	V	—
5	VFB_SEL High Input Logic	$V_{VFBSELH}$	1	—	0.7 × V_{REG}	—	5	V	—
6	VFB_SEL Low Input Logic	$V_{VFBSELL}$	1	—	0	—	0.3 × V_{REG}	V	—
7	PWM High input Logic	V_{PWMH}	1	—	0.7 × V_{REG}	—	5	V	—
8	PWM Low input Logic	V_{PWML}	1	—	0	—	0.3 × V_{REG}	V	—
Input Pin Current Consumption									
9	Enable Pin Current	I_{ENB}	1	ENB = 6 V	—	—	25	µA	—
Output Driver									
10	SW High Output Logic	V_{SWH}	1	SW output High logic; MOSFET ON condition	0.7 × V_{REG}	—	V_{REG} +0.2	V	—
11	SW Low Output Logic	V_{SWL}	1	SW output Low logic; MOSFET OFF condition	–0.2	—	0.2	V	—
Under Voltage Lock Out (UVLO)									
12	Under Voltage protection on value	V_{UVLOON}	1	V_{IN} Falling SW OFF; V_{REG} = no load	1.9	2.1	2.3	V	—
13	Under voltage protection Hysteresis	$V_{UVLOHYS}$	1	V_{IN} Rising SW ON – V_{IN} Falling SW OFF; V_{REG} = no load	0.1	0.3	0.5	V	—

■ Electrical Characteristics (Reference values for design) at V_{IN} = 6 V

Note) T_a = 25°C±2°C /T_a = 25°C±2°C unless otherwise specified.
The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection.
If a problem does occur related to these characteristics, we will respond in good faith to user concerns.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Notes
					Min	Typ	Max		
Reference Voltage Control									
14	VFB Reference Voltage 1	V_{VFB1}	1	VFB_SEL = High OVP = 0 V (Buck mode)	196	202	208	mV	—
15	VFB Reference Voltage 2	V_{VFB2}	1	VFB_SEL = Low OVP = 0 V (Buck mode)	24	32	40	mV	—
Over Voltage Protection (Boost Mode Only)									
16	Over Voltage Protection Threshold	V_{OVP}	—	R1 = 470 kΩ, R2 = 30 kΩ	18	21	24	V	—
Output Driver									
17	Driver Off Time	T_{OFF}	1	Fix off time at SW pin	0.5	1	2	μs	—
18	Maximum Operating Frequency	F_{Max}	1	—	—	—	1.5	MHz	—
Regulator Voltage (VREG)									
19	VREG Output Voltage	V_{REG}	1	4 V ≤ V_{IN} ≤ 15 V No Load Condition, CVREG = 1 μF	3.45	3.65	3.85	V	—
Efficiency									
20	Efficiency	Eff	—	V_{IN} = 6 V 1 LED of V_F = 3.7 V I_{LED} = 400 mA VFB_SEL = High OVP = 0 V (Buck mode)	—	90	—	%	—

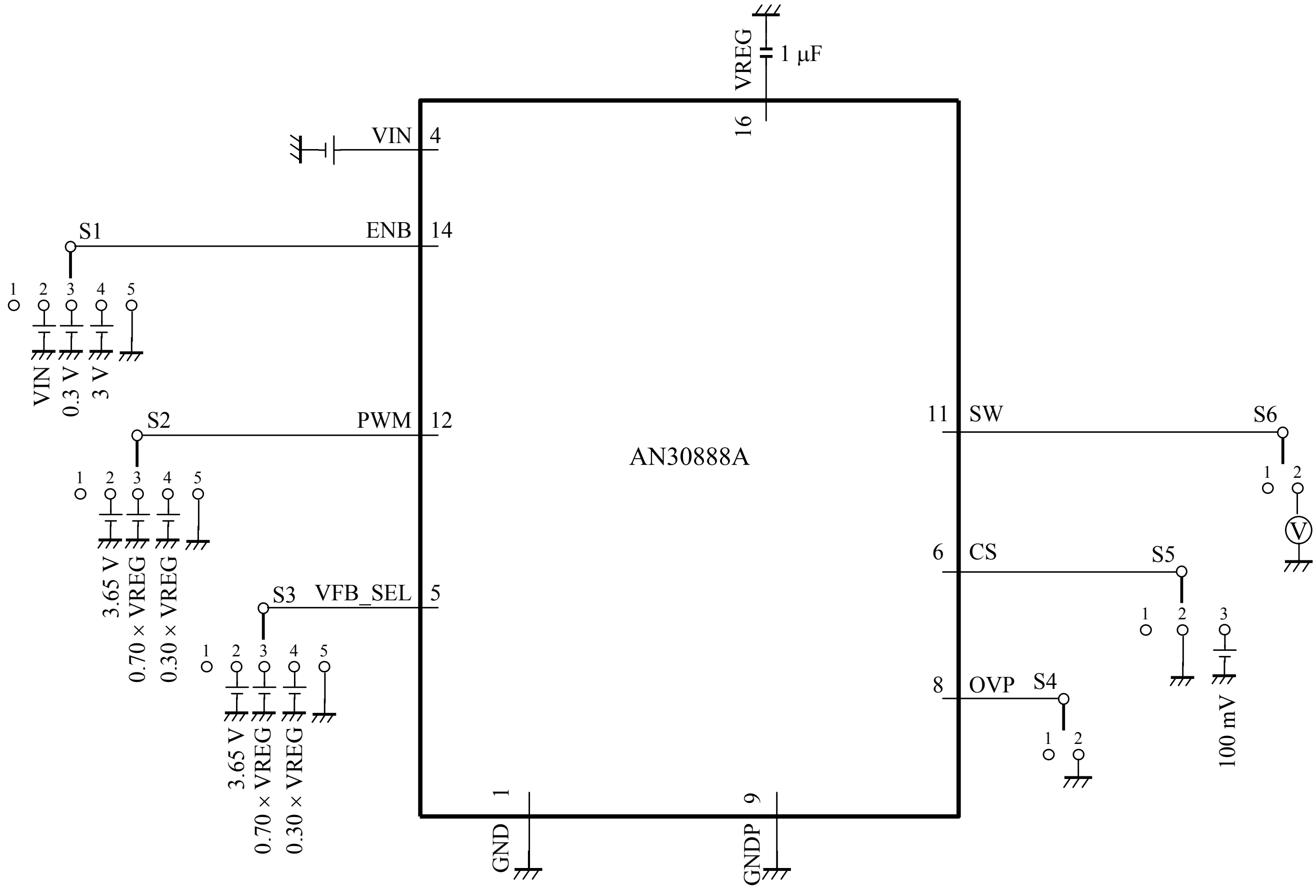
■ Control Pin Mode Table

Note) See parameters B No. 3, 4, 5, 6, 7 and 8 in the Electrical Characteristics for control voltage ranges.

Pin No.	Description		Pin voltage		Remarks
			Low	High	
5	VFB_SEL	ON/OFF	V_{FB} = 32 mV	V_{FB} = 202 mV	Feedback voltage selection
12	PWM	ON/OFF	PWM OFF	PWM ON	When PWM is not used, the pin is left floating
14	ENB	ON/OFF	STANDBY	OPERATING	Standby / Operating mode control

■ Test Circuit Diagram

1. Test Circuit 1



■ Electrical Characteristics Test Procedures

C No.	Parameter	Input		Output		Switch					
		Pin No.	Conditions	Pin No.	Conditions	S1	S2	S3	S4	S5	S6
Circuit Current Consumption											
1	Standby Current	14 12 5 8 6 11	ENB = 0 V PWM = 0 V VFB_SEL = 0 V OVP = 0 V CS = 0 V SW = Hi-Z	4	Standby current consumption	5	5	5	2	2	1
2	Operating Quiescent Current	14 12 5 8 6 11	ENB = V_{IN} PWM = 0 V VFB_SEL = 0 V OVP = 0 V CS = 0 V SW = Hi-Z	4	Current consumption	2	5	5	2	2	1
ENABLE (ENB), VFB_SEL and PWM Control Function											
3	ENB High Input Logic	14 12 5 8 6 11	ENB = 0.30 V PWM = Hi-Z VFB_SEL = 3.65 V OVP = 0 V CS = 0 V SW = Hi-Z	16	Output DC voltage	3	1	2	2	2	1
4	ENB Low Input Logic	14 12 5 8 6 11	ENB = 3.0 V PWM = Hi-Z VFB_SEL = 3.65 V OVP = 0 V CS = 0 V SW = Hi-Z	16	Output DC voltage	4	1	2	2	2	1
5	VFB_SEL High Input Logic	14 12 5 8 6 11	ENB = V_{IN} PWM = Hi-Z VFB_SEL = 0.70× V_{REG} OVP = 0 V CS = 100 mV SW = Hi-Z	11	Output DC voltage / 1 MHz	2	1	3	2	3	1
6	VFB_SEL Low Input Logic	14 12 5 8 6 11	ENB = V_{IN} PWM = Hi-Z VFB_SEL = 0.30 × V_{REG} OVP = 0 V CS = 100 mV SW = Hi-Z	11	Output DC voltage / 1 MHz	2	1	4	2	3	1
7	PWM High input Logic	14 12 5 8 6 11	ENB = V_{IN} PWM = 0.70 × V_{REG} VFB_SEL = 3.65 V OVP = 0 V CS = 0 V SW = Hi-Z	11	Output DC voltage / 1 MHz	2	3	2	2	2	1

■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Switch					
		Pin No.	Conditions	Pin No.	Conditions	S1	S2	S3	S4	S5	S6
8	PWM Low input Logic	14 12 5 8 6 11	ENB = V_{IN} PWM = 0.30 × V_{REG} VFB_SEL = 3.65 V OVP = 0 V CS = 0 V SW = Hi-Z	11	Output DC voltage / 1 MHz	2	4	2	2	2	1
Input Pin Current Consumption											
9	Enable Pin Current	14 12 5 8 6 11	ENB = V_{IN} PWM = Hi-Z VFB_SEL = 0 V OVP = 0 V CS = 0 V SW = Hi-Z	14	Current Consumption	2	1	5	2	2	1
Output Driver											
10	SW High Output Logic	14 12 5 8 6 11	ENB = V_{IN} PWM = 3.65 V VFB_SEL = 3.65 V OVP = 0 V CS = 0 V SW = 0 A	11	Output DC voltage / 1 MHz	2	2	2	2	2	2
11	SW Low Output Logic	14 12 5 8 6 11	ENB = V_{IN} PWM = 0 V VFB_SEL = 3.65 V OVP = 0 V CS = 0 V SW = 0 A	11	Output DC voltage / 1 MHz	2	5	2	2	2	2

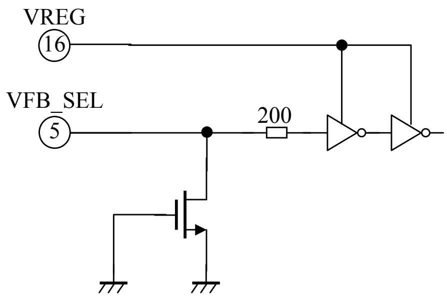
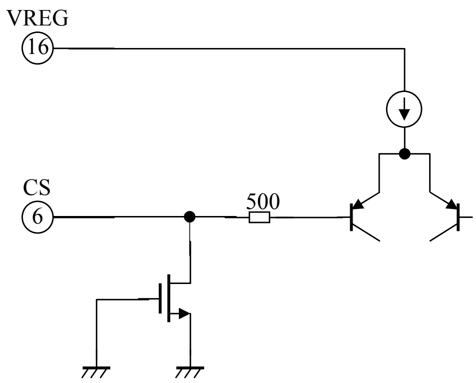
■ Electrical Characteristics Test Procedures (continued)

C No.	Parameter	Input		Output		Switch					
		Pin No.	Conditions	Pin No.	Conditions	S1	S2	S3	S4	S5	S6
Under voltage Lock Out (UVLO)											
12	Under voltage protection on value	14 12 5 8 6 11	ENB = V_{IN} PWM = Hi-Z VFB_SEL = 3.65 V OVP = 0 V CS = 0 V SW = Hi-Z	11	Output DC voltage / 1 MHz	2	1	2	2	2	1
13	Under voltage protection Hysteresis	14 12 5 8 6 11	ENB = V_{IN} PWM = Hi-Z VFB_SEL = 3.65 V OVP = 0 V CS = 0 V SW = Hi-Z	11	Output DC voltage / 1 MHz	2	1	2	2	2	1

■ Technical Data

• I/O block circuit diagrams and pin function descriptions

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
1	GND	—	—	Signal Ground
2	—	—	—	No connection
3	—	—	—	No connection
4	DC (3 V to 20 V)	—	Z : Low	VIN Power Supply of IC
5	DC (0 V to 5 V)		Z : Hi-Z	VFB_SEL Feedback voltage select pin
6	DC (0 V to 250 mV)		Z : Hi-Z	CS Current Sense Pin

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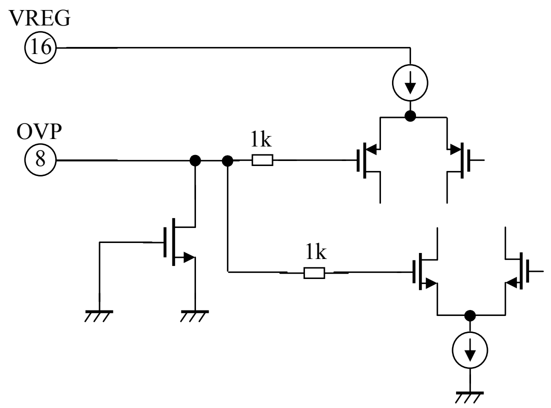
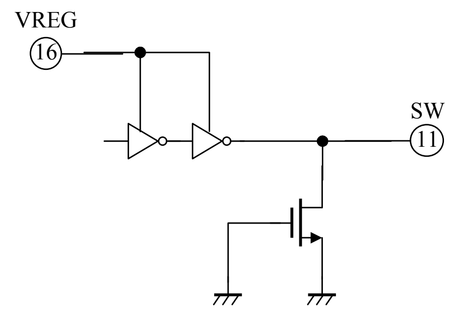
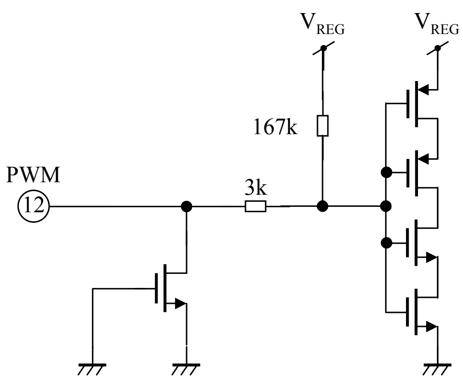
■ Technical Data (continued)

• I/O block circuit diagrams and pin function descriptions (continued)

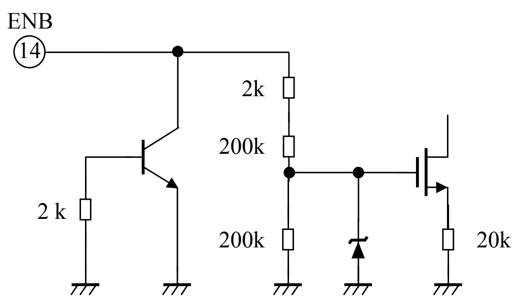
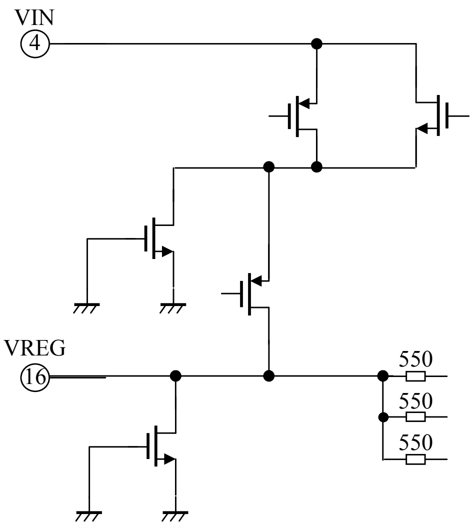
Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
7	—	—	—	No connection
8	DC (0 V to 1.26 V)		Z : Hi-Z	OVP Over Voltage Protection input pin for Boost and Buck-Boost mode Connect to GND for Buck mode
9	GNDP	—	—	Power Ground
10	—	—	—	No connection
11	Pulse (0 V to 3.65 V)		Z : Hi-Z	SW External NMOS Transistor Gate Driving Pulse
12	Pulse (0 V to 5 V)		Z : 170 kΩ	PWM PWM Dimming Control

■ Technical Data (continued)

• I/O block circuit diagrams and pin function descriptions (continued)

Note) The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

Pin No.	Waveform and voltage	Internal circuit	Impedance	Description
13	—	—	—	No connection
14	DC (3 V to 20 V)		Z : 402 kΩ	ENB Standby On/Off Control Pin
15	—	—	—	No connection
16	DC (Typ. 3.65 V)		Z : Hi-Z	VREG Regulator Output Pin

■ Technical Data (continued)

• Functions and properties descriptions

(1) Overview

AN30888A is a constant current LED driver. The IC works as a Boost /Buck-Boost/ Buck mode DCDC controller with external MOSFET.
Operating input voltages ranges from 3 V to 20 V. The mode of operation depends on the number of LEDs to be driven and the supply voltage level.

In general, please adhere to the following:
If total LED voltage drop is more than supply voltage, boost mode is adopted. If LED voltage drop is less than the supply voltage, buck mode is adopted . If supply voltage is close to the total LED voltage drop, the Buck-Boost mode can be used. Please note that the different mode of operation should be manually configured.

Output LED current can be designed ranges from 0 A and to a few amperes depending on the mode of operation, the external MOSFET characteristic and feasible R_{CS} value used. The control architecture uses current mode fix off time control. The V_{FB} reference voltage determines LED current by setting VFB_SEL pin with values of 32 mV or 202 mV under buck mode. By applying V_{FB} voltage of 32 mV, user can achieve higher efficiency with lower power dissipation in R_{CS} resistor. Applying 202 mV V_{FB} voltage achieves better LED current accuracy.

(2) Standby enable function

AN30888A enters standby mode when ENB pin is pulled low. During standby, the IC draws a small current of value less than 10 μA from the power supply. This helps to achieve longer battery usage time. During Boost mode operation, although external MOSFET cannot be turned on at standby condition, there is still a DC current path between the input and the LEDs through the inductor and schottky diode. Thus it is important to make sure that during boost mode, the minimum forward voltage of the LED array must exceed the maximum input voltage to ensure the LEDs remain off during standby mode.

■ Technical Data (continued)

• Functions and properties descriptions (continued)

(3) Internal regulator

An internal 3.65 V regulator is used as the power supply for internal core circuit of this IC.
This regulated voltage, V_{REG} will be provided when V_{IN} is approximately in the range of 4 V to 20V. For V_{IN} lower than 4 V, regulator will act as a V_{IN} voltage follower, with output voltage close to $V_{IN.}$ The amount of drop voltage from V_{IN} during V_{IN} follower mode depends on load current of the regulator and also tolerance of the IC. In general, the regulator output voltage will be approximately 0.3 V lower than V_{IN} during this mode of operation.
This regulator requires a capacitor of 1 µF to be connected to VREG pin. This capacitor helps to provide a stable regulated voltage to the IC. The regulator has a current ability of approximately 15 mA. However, it is not designed to provide as external power supply voltage. Hence an external load exceeding approximately 0.5 mA to the VREG pin is not allowed.

(4) Output setting consideration

The output voltage, V_{OUT} is set using the following equations for both boost and buck mode:

$$V_{OUT} = (V_F \times N_{LEDs} + V_D) \quad \text{Eq[1]} \quad \text{(Boost mode)}$$

$$V_{OUT} = (V_{IN} - V_F \times N_{LEDs}) \quad \text{Eq[2]} \quad \text{(Buck mode)}$$

$$V_{OUT} = (V_F \times N_{LEDs} + V_D + V_{IN}) \quad \text{Eq[3]} \quad \text{(Buck-Boost mode)}$$

V_{IN} : Battery or Input power supply voltage
V_F : LED forward drop voltage
N_{LEDs} : Number of LEDs stacked in series
V_D : Schottky diode forward drop voltage

For Boost mode or Buck-Boost mode operation, V_{OUT} setting should be lesser than Drain–Source breakdown voltage of external MOSFET as mention in (11). Also V_{OUT} should be lesser than OVP protection threshold as mentioned in (9).

For Buck mode operation, V_{OUT} setting should give sufficient voltage for external MOSFET to operate properly at the required output current setting.

■ Technical Data (continued)

• Functions and properties descriptions (continued)

(5) Feedback voltage V_{FB} at CS pin

The V_{FB} voltage is generated internally in the IC and output at CS pin. This voltage allows users to fix the input peak current, I_{PK} as well as the LED output current, I_{LED}. This voltage will change according to the setting at VFB_SEL pin.

For operation in boost mode/buck-boost mode, V_{FB} will be inversely proportionally to supply voltage, V_{IN}. When input supply voltage decreases, V_{FB} will increase. This ensure LED current remain accurate as supply voltage decreases.
When operating in buck mode, V_{FB} voltage will remain at 202 mV or 32 mV depending on whether VFB_SEL pin is high or low.

The following are some figures of V_{FB} voltage with respect to V_{IN}. For detail information, please refer to graph and data table information as the following.

For Boost mode and Buck-Boost mode :

V_{FB} = 116 mV (When VFB_SEL = High ; V_{IN} = 6 V)
V_{FB} = 50 mV (When VFB_SEL = Low ; V_{IN} = 6 V)
V_{FB} = 198.3 mV (When VFB_SEL = High ; V_{IN} = 3 V)
V_{FB} = 88 mV (When VFB_SEL = Low ; V_{IN} = 3 V)

For Buck mode :

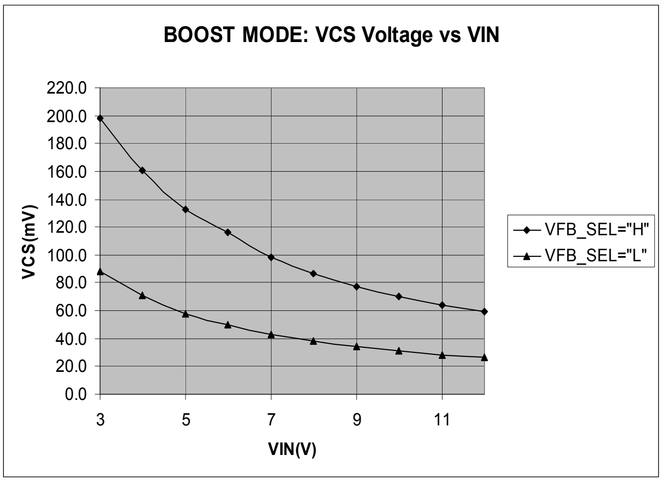
V_{FB} = 202 mV (When VFB_SEL = High, for all V_{IN} level)
V_{FB} = 32 mV (When VFB_SEL = Low, for all V_{IN} level)

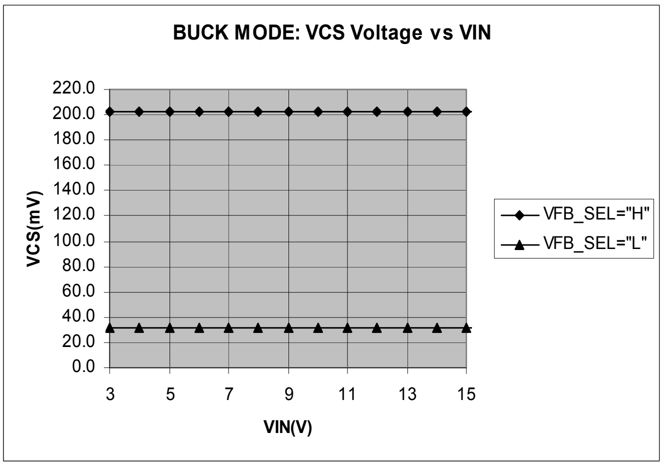
To improve overall efficiency V_{FB} voltage can be set lower by switching VFB_SEL = Low. On the other hand accuracy can be improved by using VFB_SEL = High mode.

■ Technical Data (continued)

• Functions and properties descriptions (continued)

(5) Feedback voltage V_{FB} at CS pin (continued)





V_{IN} (V)	Boost mode/ Buck-Boost mode		Buck mode	
	VFB_SEL = High	VFB_SEL = Low	VFB_SEL = High	VFB_SEL = Low
	V_{FB} (mV)	V_{FB} (mV)	V_{FB} (mV)	V_{FB} (mV)
3	198.3	88.0	202	32
4	161.0	71.0	202	32
5	132.3	57.7	202	32
6	116.0	50.0	202	32
7	98.3	43.0	202	32
8	86.3	38.0	202	32
9	77.3	34.0	202	32
10	70.0	31.0	202	32
11	64.0	28.3	202	32
12	59.0	26.3	202	32
13	N.A	N.A	202	32
14	N.A	N.A	202	32
15	N.A	N.A	202	32

■ Technical Data (continued)

• Functions and properties descriptions (continued)

(6) Inductor selection

Inductor value, L is set by the required inductor ripple current desired.
The general trend for lower inductor value is a smaller inductor physical size, but a larger input ripple current. Similarly, an increase in inductor value will decease input ripple current.
Users are advice to choose an inductor that can handle the peak current I_{PK}, flowing across it without saturating. In addition, inductor with lower series resistance are preferred to provide better operating efficiency.

The following equation gives a general guideline in selection inductor value based on 30% peak to peak ripple current across the inductor.

$$L = \frac{(V_{OUT} - V_{IN}) \times T_{OFF}}{0.3 \times I_{IN}} \quad \cdots\cdots\cdots \quad \text{Eq[4]} \qquad \text{(Boost mode, Buck-Boost mode)}$$

$$L = \frac{(V_{IN} - V_{OUT}) \times T_{OFF}}{0.3 \times I_{LED}} \quad \cdots\cdots\cdots \quad \text{Eq[5]} \qquad \text{(Buck mode)}$$

V_{OUT} / Output voltage
V_{IN} / Input supply voltage
T_{OFF} / Fixed off time design at 1 μs
I_{LED} / LED output current
I_{IN} / I_{IN} is input current from supply voltage

Please note that the 0.3 factor can be altered if 30% peak to peak current is changed.
i.e, if percentage of peak to peak current needed is 40%, this factor will be 0.4.

■ Technical Data (continued)

- Functions and properties descriptions (continued)

(7) Setting output LED current and choosing current sense resistor R_{CS}

The LED current in this IC can be set easily by selecting the appropriate R_{CS} resistor to be used at CS pin of this chip.

For Boost Mode and Buck-Boost mode :

R_{CS} resistor can be set in the following way :
First is to calculate input current I_{IN} at the required operating condition :

$$I_{IN} = (V_{OUT} + V_D) \times (I_{LED} / V_{IN}) \quad \text{Eq[6]} \quad \text{(Boost mode, Buck-Boost mode)}$$

V_{OUT} / Output voltage
V_D / Schottky diode forward drop voltage
I_{LED} / Required LED current
V_{IN} / Input supply voltage

After which the peak input current, I_{PK} can be determine by adding I_{IN} with half the peak to peak ripple current at the inductor.

$$I_{PK} = I_{IN} + \frac{(V_{OUT} - V_{IN}) \times T_{OFF}}{2L} \quad \text{Eq[7]} \quad \text{(Boost mode, Buck-Boost mode)}$$

T_{OFF} / T_{OFF} is fixed off time = 1 µs
L / Inductor value found in part (6) inductor selection
V_{OUT} / Output voltage
V_{IN} / Input supply voltage
I_{IN} / I_{IN} is input current found in Eq[6]

Lastly, R_{CS} resistor can be determine by using :

$$R_{CS} = \frac{V_{FB}}{I_{PK}} \quad \text{Eq[8]} \quad \text{(Boost mode, Buck-Boost mode)}$$

V_{FB} is voltage at CS pin. Refer to data graphs for the V_{FB} voltage at different input voltage condition.
I_{PK} is peak current found in Eq[7]

Using numeric example of operating condition :

V_{IN} = 6 V, V_{OUT} = 10 V, I_{LED} = 500 mA, T_{OFF} = 1 µs, L = 16 µH, V_D = 0.4 V, V_{FB} = 0.1 V@V_{IN} = 6 V

From Eq[6] : $I_{IN} = (10 + 0.4) \times (0.5 / 6) = 0.8667$ A

From Eq[7] : $I_{PK} = 0.8667 + \frac{(10 - 6) \times 1\mu}{2 \times 16\mu} = 0.9971$ A

From Eq[8] : $R_{CS} = \frac{0.1}{0.9917} = 100.8$ mΩ

■ Technical Data (continued)

• Functions and properties descriptions (continued)

(7) Setting output LED current and choosing current sense resistor R_{CS} (continued)

For Buck Mode :

R_{CS} resistor can be set in the following way :
First is to calculate the peak current I_{PK} using Eq[9]. During buck mode, peak current sense correspond to the average output LED current plus half of actual current ripple through the inductor.

$$I_{PK} = I_{LED} + \frac{(V_{IN} - V_{OUT}) \times T_{OFF}}{2L} \quad \text{.......................} \quad \text{Eq[9]} \qquad \text{(Buck mode)}$$

V_{OUT}	/ Output voltage
V_{IN}	/ Input supply voltage
T_{OFF}	/ T_{OFF} = Fixed off time design at 1 µs
I_{LED}	/ LED output current
L	/ L = Inductor value found in part (6) inductor selection

Lastly, R_{CS} resistor can be determine by using :

$$R_{CS} = \frac{V_{FB}}{I_{PK}} \quad \text{..} \quad \text{Eq[10]} \qquad \text{(Buck mode)}$$

V_{FB} is voltage at CS pin. Refer to data graphs for the V_{FB} voltage at different input voltage condition.
I_{PK} is peak current found in Eq[9] .

Using numeric example of operating condition :

V_{IN} = 12 V, V_{OUT} = 2 V, I_{LED} = 500 mA, T_{OFF} = 1 µs, L = 66 µH, V_{FB} = 0.2 V

From Eq[9] : $I_{PK} = 0.5 + \frac{(12 - 2) \times 1\mu}{2 \times 66\mu} = 0.575 \text{ A}$

From Eq[10] : $R_{CS} = \frac{0.2}{0.575} = 348 \text{ m}\Omega$

Please note that for component deviation such as inductor, diodes, etc, these deviation can cause the designed I_{PK} to be higher or lower than the calculated value.
Users may need to fine tune the value of R_{CS} from the calculated values in order to obtain accurate I_{LED} measurement.
Please take note of total impedance including parasitic impedance of PCB trace at CS pin to ground when designing the required R_{CS} value. This is especially important if the designed I_{LED} is high as R_{CS} value will be small and in turn making parasitic impedance significant to the total impedance seen at CS pin

■ Technical Data (continued)

• Functions and properties descriptions (continued)

(8) Soft start

Soft start circuit is incorporated into this IC to avoid high in-rush current during start-up.
After the device is enabled (ENB = High), the output inductor current and output voltage will rise slowly from initial condition. This slow start-up time ensure smooth start-up as well as minimize in-rush current.

(9) Over Voltage Protection (OVP)

When operating in Boost mode or Buck-Boost mode, over voltage protection is needed to prevent damages to IC or external component damages in cases of open LED condition.
OVP switches off external power MOSFET to prevent output from rising over a designed OVP voltage. Output voltage should be limited to the rating of external component used. (for example Drain Source voltage rating of the external MOSFET or the output capacitor)
OVP compares the internal reference voltage of 1.26 V with output voltage through resistor network.

OVP threshold is set using the following equation:

$$V_{OVP} = \frac{1.262\ \text{V} \times (R1 + R2)}{R2} \quad \text{........................} \quad \text{Eq[11]} \qquad \text{(Boost mode, Buck-Boost mode)}$$

If R1 = 470 kΩ, R2 = 30 kΩ, OVP threshold will be designed at around 21 V.
When OVP is triggered, output voltage will be clamped at this threshold voltage (with hysteresis of around 1 V to 2 V) until the fault (e.g open LED condition) has been removed.

When operating in buck mode, the OVP pin must be short to ground to disable this function as OVP function is not necessary in this mode.

■ Technical Data (continued)

- Functions and properties descriptions (continued)

(10) Under Voltage Lock Out (UVLO)

Under Voltage lock out prevents IC from operation at supply voltage lower than 2.1 V.
This function prevent IC from abnormal operation when supply voltage V_{IN} drops below our recommended input range. When input voltage is lower than this lock out value of 2.1 V, external MOSFET will be switched off. When input voltage rises to 2.4 V or more, device operation starts again. This means a hysteresis voltage of about 0.3 V.

(11) Power MOSFET consideration

When selecting the power MOSFET, it is important to consider parameters such as gate-source, drain-source breakdown voltage, total gate capacitance, ON resistance and the drain current rating.
When power is turned on for IC operating in boost mode, output voltage needed to drive LED will be reflected to Drain-Source voltage of the power MOSFET. Thus it is recommended to select a MOSFET that can handle this output voltage. Alternatively, output and Drain-Source voltage can be protected and clamped by OVP circuit as mentioned in point (9).
Gate capacitance of the MOSFET chosen should ideally to be smaller than 3 nF.

(12) PWM operation

PWM signal can be generated externally and input into PWM pin of this IC. This PWM signal will turn on and off the output driver, giving an average output LED current that is proportional to the duty cycle of the PWM signal.

$$I_{LED(avg.)} = I_{LED} \times Duty \quad \text{Eq[12]} \quad \text{(Boost / Buck-Boost / Buck mode)}$$

$I_{LED(avg.)}$ = The average output LED current after PWM is input
I_{LED} = The nominal LED current set in part (7)
Duty = The ratio of on pulse time compared to total period time of the PWM signal.

A PWM frequency of 1 kHz or lower is recommended to minimize error due to rise and fall time of the converter output.

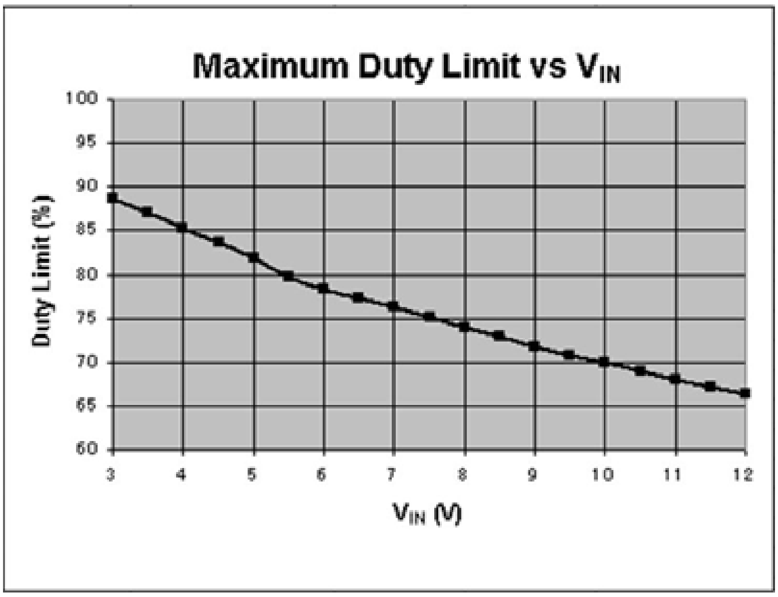
■ Technical Data (continued)

• Functions and properties descriptions (continued)

(13) Maximum duty operation

Maximum Duty limitation is needed when operating in Boost or Buck- Boost mode. This prevents the output voltage from having abnormal operation. For Buck mode, there is no need for maximum duty limit as SW pin is able to switch to 100% duty.
Please refer to the graph below for maximum duty vs V_{IN} data for Boost and Buck-Boost mode operation.

Boost/Buck-boost mode	
V_{IN} (V)	Duty Limit (%)
3.0	88.73
3.5	87.09
4.0	85.27
4.5	83.58
5.0	81.99
5.5	79.79
6.0	78.40
6.5	77.38
7.0	76.25
7.5	75.19
8.0	73.92
8.5	72.89
9.0	71.78
9.5	70.83
10.0	69.91
10.5	68.90
11.0	67.97
11.5	67.09
12.0	66.33



(14) Minimum duty operation

Parasitic circuit capacitance, inductance and external MOSFET gate drive current can create spike in the current sense, CS pin voltage at the point when external MOSFET is switched on. In order to prevent this spike to terminate the ON time prematurely, an internal filter of time constant, 100 ns is designed in chip. This time constant of 100 ns translates to a minimum duty of around 9% for all modes of operation. To further reduce the spike in the CS voltage especially when operating in low I_{LED} condition (example: R_{CS} is more than 0.8 Ω or more), external RC filter can be used in between V_{FB} node to CS pin which act as a low pass filter to filter spike noise from entering CS pin. This RC filter time constant should be long enough to reduce the parasitic spike without significantly affecting the shape of CS voltage.
The recommended RC value range from : R = 10 Ω to 1 kΩ and C = 100 pF to 500 pF depending on mode of operation and spike level.

■ Usage Notes

- Special attention and precaution in using

1. This IC is intended to be used for general electronic equipment [LED Lighting Devices].
   Consult our sales staff in advance for information on the following applications:
   - Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   - Any applications other than the standard applications intended.
     (1) Space appliance (such as artificial satellite, and rocket)
     (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
     (3) Medical equipment for life support
     (4) Submarine transponder
     (5) Control equipment for power plant
     (6) Disaster prevention and security device
     (7) Weapon
     (8) Others : Applications of which reliability equivalent to (1) to (7) is required

   It is to be understood that our company shall not be held responsible for any damage incurred as a result of or in connection with your using the IC described in this book for any special application, unless our company agrees to your using the IC in this book for any special application.

2. Pay attention to the direction of LSI. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might smoke or ignite.

3. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

4. Perform a visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as a solder-bridge between the pins of the semiconductor device. Also, perform a full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.

■ Usage Notes (continued)

• Special attention and precaution in using (continued)

5. Take notice in the use of this product that it might break or occasionally smoke when an abnormal state occurs such as output pin-V_{DD} short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short) .
   And, safety measures such as an installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

6. When designing your equipment, comply with the range of absolute maximum rating and the guaranteed operating conditions (operating power supply voltage and operating environment etc.). Especially, please be careful not to exceed the range of absolute maximum rating on the transient state, such as power-on, power-off and mode-switching. Otherwise, we will not be liable for any defect which may arise later in your equipment.
   Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

7. When using the LSI for new models, verify the safety including the long-term reliability for each product.

8. When the application system is designed by using this LSI, be sure to confirm notes in this book.
   Be sure to read the notes to descriptions and the usage notes in the book.

PACKAGE STANDARDS

Package Code	SSOP016-P-0225E

Semiconductor Company
Panasonic Corporation

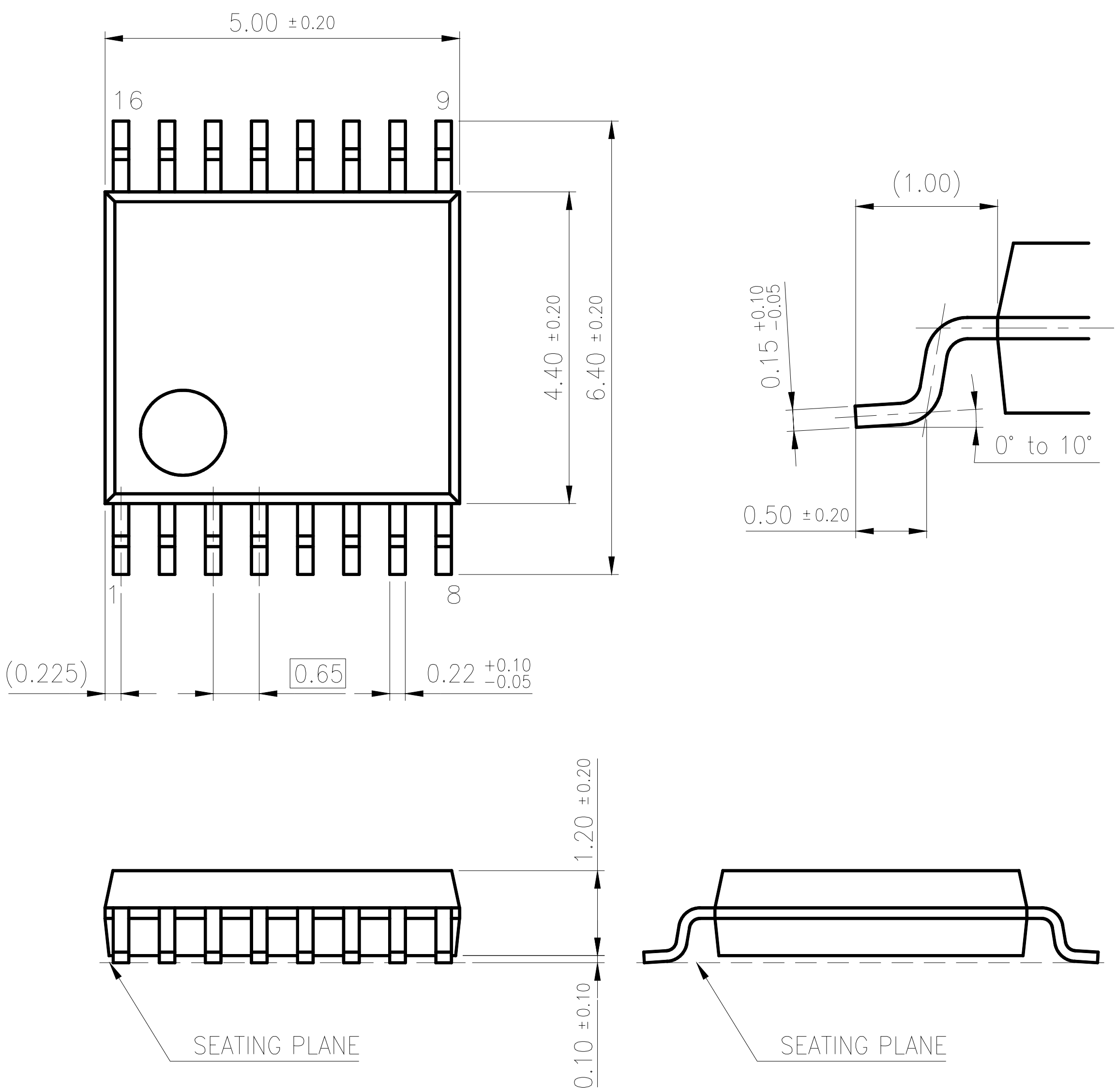
Established by	Applied by	Checked by	Prepared by
H.Shidooka	H.Yoshida	M.Okajima	M.Itoh

Established: 2004-01-19
Revised : 2009-01-26

	PACKAGE STANDARDS SSOP016-P-0225E	Total Pages	Page
		6	2

1. Outline Drawing

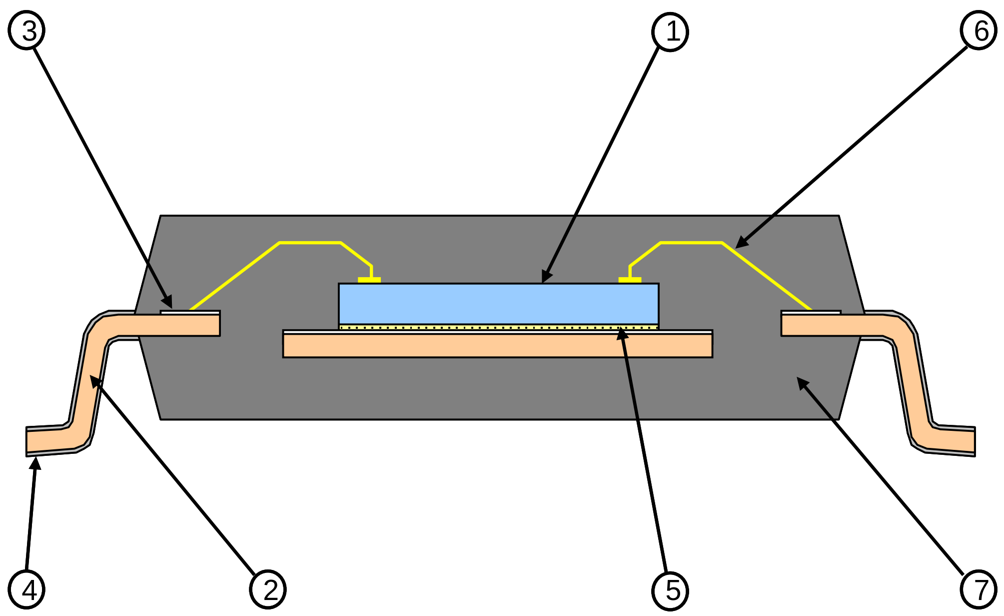
Unit:mm



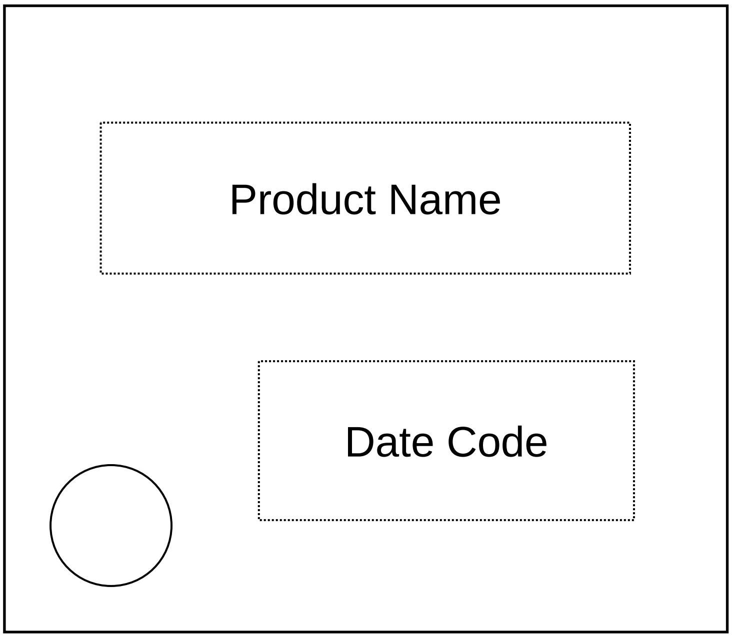
Body Material : Epoxy Resin	
Lead Material : Cu Alloy	
Lead Finish Method : SnBi Plating	

2. Package Structure (Technical Report : Reference Value)

Chip Material		Si	①
Leadframe material		Cu alloy	②
Inner lead surface		Ag plating	③
Outer lead surface		SnBi plating	④
Chip mount	Method	Resin adhesive method	⑤
	Material	Adhesive material	
Wirebond	Method	Thermo-compression bonding	⑥
	Material	Au	
Molding	Method	Transfer molding	⑦
	Material	Epoxy resin	
Mass		72 mg	

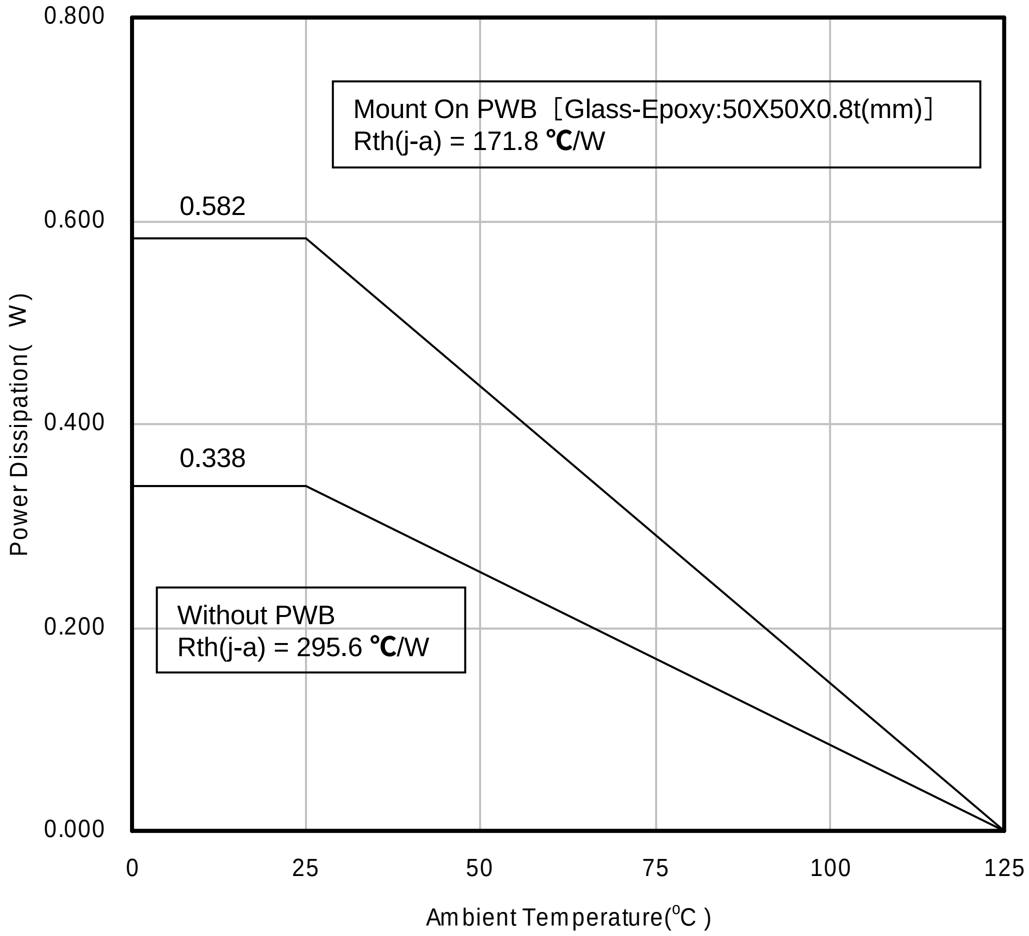


3. Mark Drawing



Established: 2004-01-19
Revised : 2009-01-26

4. Power Dissipation (Technical Report)



Established: 2004-01-19
Revised : 2009-01-26

5. Power Dissipation（Supplementary Explanation）

[Experiment environment]

Power Dissipation（Technical Report）is a result in the experiment environment of SEMI standard conformity. （Ambient air temperature (Ta) is 25 degrees C）

[Supplementary information of PWB to be used for measurement]

The supplement of PWB information for Power Dissipation data (Technical Report）are shown below.

Indication	Total Layer	Resin Material
Glass-Epoxy	1-layer	FR-4
4-layer	4-layer	FR-4

[Notes about Power Dissipation（Thermal Resistance）]

Power Dissipation values（Thermal Resistance）depend on the conditions of the surroundings, such as specification of PWB and a mounting condition , and a ambient temperature. (Power Dissipation (Thermal Resistance) is not a fixed value.)

The Power Dissipation value（Technical Report）is the experiment result in specific conditions (evaluation environment of SEMI standard conformity) ,and keep in mind that Power Dissipation values (Thermal resistance) depend on circumference conditions and also change.

[Definition of each temperature and thermal resistance]

Ta ：Ambient air temperature
※The temperature of the air is defined at the position where the convection, radiation, etc. don't affect the temperature value, and it's separated from the heating elements.

Tc ：It's the temperature near the center of a package surface. The package surface is defined at the opposite side if the PWB.

Tj ：Semiconductor element surface temperature (Junction temperature.)

Rth(j-c)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the package surface

Rth(c-a)：The thermal resistance (difference of temperature of per 1 Watts) between the package surface and the ambient air

Rth(j-a)：The thermal resistance (difference of temperature of per 1 Watts) between a semiconductor element junction part and the ambient air

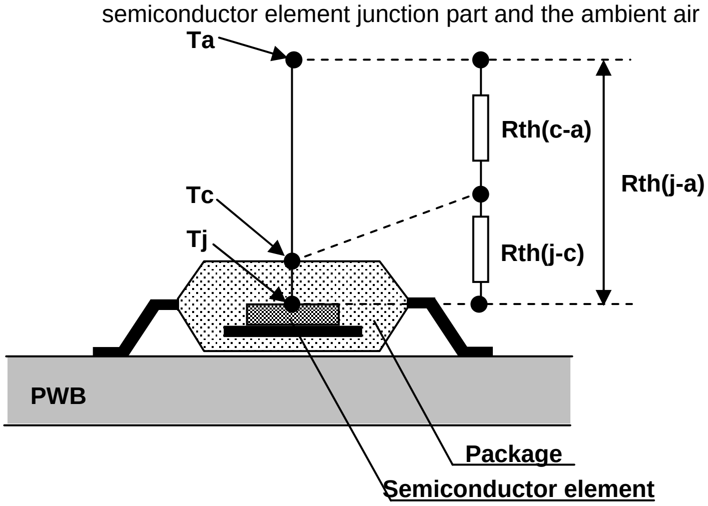


Fig1. Definition image

[Definition formula]

$$Tj=\{Rth(j\text{-}c)+Rth(c\text{-}a)\}\times P+Ta$$
$$=Rth(j\text{-}a)\times P+Ta$$

$$Rth(j\text{-}c)=\frac{Tj-Tc}{P}\quad (℃/W)$$

$$Rth(c\text{-}a)=\frac{Tc-Ta}{P}\quad (℃/W)$$

$$Rth(j\text{-}a)=\frac{Tj-Ta}{P}\quad (℃/W)$$

$$=Rth(j\text{-}c)+Rth(c\text{-}a)$$

P:power(W)

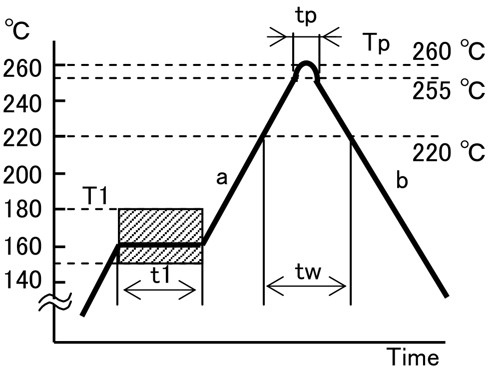
Product name : AN30888A-VF
Package : SSOP016-P-0225E

1. Recommended Soldering Conditions

In case that the semiconductor packages are mounted on the PCB, the soldering should be performed under the following conditions.

① Reflow soldering

Reflow peak temp. :	max. 260 ℃



No.	mark	contents	value
1	T1	Pre-heating temp.	150 ℃～180 ℃
2	t1	Pre-heating temp. hold time	60 s～120 s
3	a	Rising rate	2 ℃/s～5 ℃/s
4	Tp	Peak temp.	255 ℃+5 ℃､-0 ℃
5	tp	Peak temp. hold time	10 s±3 s
6	tw	High temp. region hold time	within 60 s (≧220 ℃)
7	b	Down rate	2 ℃/s～5 ℃/s
8	-	Number of reflow	within 2 times

＊Peak temperature : less than 260 ℃
＊Temperature is measured at package surface point

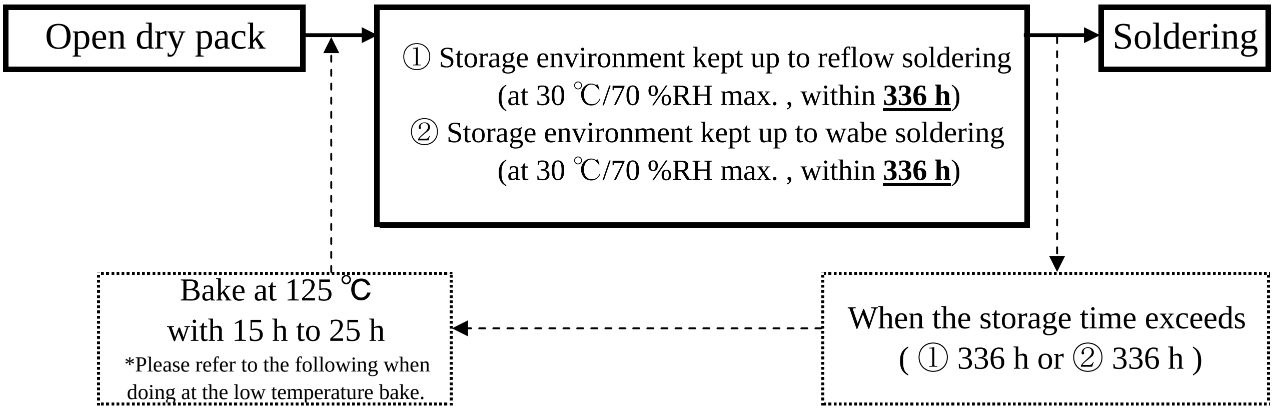
② Wave soldering (Flow soldering)

＊Temp. of solder : 260 ℃ or less
＊Soak time : within 5 s
＊Number of flow : only 1 time

③ Manual soldering

＊Iron Temperature : 350 ℃ or less (Device lead temperature : 270 ℃､10 s max.)
＊Soldering time : within 3 s
＊Number of manual soldering : only 1 time

2. Storage environment after dry pack opening



※ Because the taping and the magazine materials are not the heat-resistant materials, the bake at 125℃ cannot be done.
Therefore, please solder everything or control everything in the rule time.
Please keep them in an equal environment with the moisture-proof packaging or dry box.
(Temperature: room temperature, relative humidity: 30% or less.)
To control storage time, when bake in the taping and the magazine is necessary, it is necessary for each type to set a bake condition. Please inquire of our company.

☆ **AN30888A-VF limitation, low temperature bake condition** : **40 ℃ / 25 %RH or less / 192 h**

3. Note

① Storage environment conditions: keep the following conditions Ta=5 ℃～30 ℃、RH=30 %～70 %.

② Storage period before opening dry pack shall be 1year from a shipping day under Ta=5 ℃～30 ℃、RH=30 %～70 %. When the storage exceeds, Bake at 125 ℃ with 15 h to 25 h.

③ Baking cycle should be only one time.
Please be cautious of solderability at baking.

④ In case that use reflow two times, 2nd reflow must be finished within **336 hours**.

⑤ Remove flux sufficiently from product in the washing process.
(Flux : Chlorineless rosin flux is recommended.)

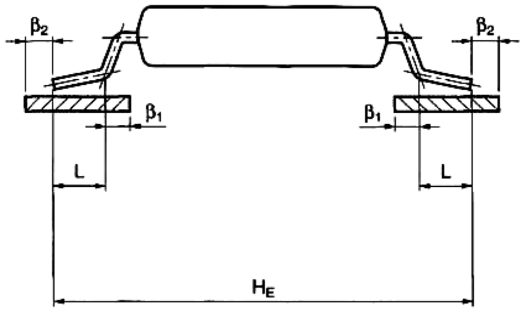
⑥ In case that use ultrasonic for product washing,
There is the possibility that the resonance may occur due to the frequency and shape of PCB.
It may be affected to the strength of lead. Please be cautious of this matter.

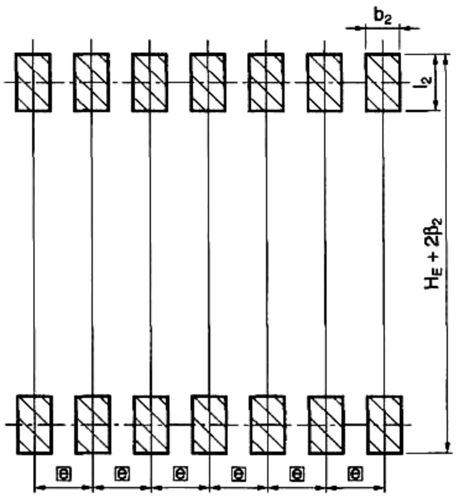
	Recommended Land Pattern	
		Total pages: 1 / page: 1

Integrated circuits

The land width for surface-mount semiconductor devices is related to on the amount of solder applied. It is necessary to optimize the land dimensions together with the method of solder application. Previously, EIAJ defined recommended land dimensions by package type, but because of the above reasons, currently only the positions where the terminals should be (the terminal land area) are standardized. For reference, the land design guidelines previously defined by EIAJ are shown below. During the actual design of the printed circuit board, the solder application method, etc. should be thoroughly considered before deciding.

SO type





$l_2 \geq L + \beta_1 + \beta_2$

$b \leq b_2 \leq e - \gamma$

γ : Solder resistance bridge (γ = 0.3 mm)

b : Terminal width

β_1 : Soldering strength (β_1 = 0.3 mm)

β_2 : Solder mask pattern accuracy or soldering guideline (β_2 = 0.2 mm)

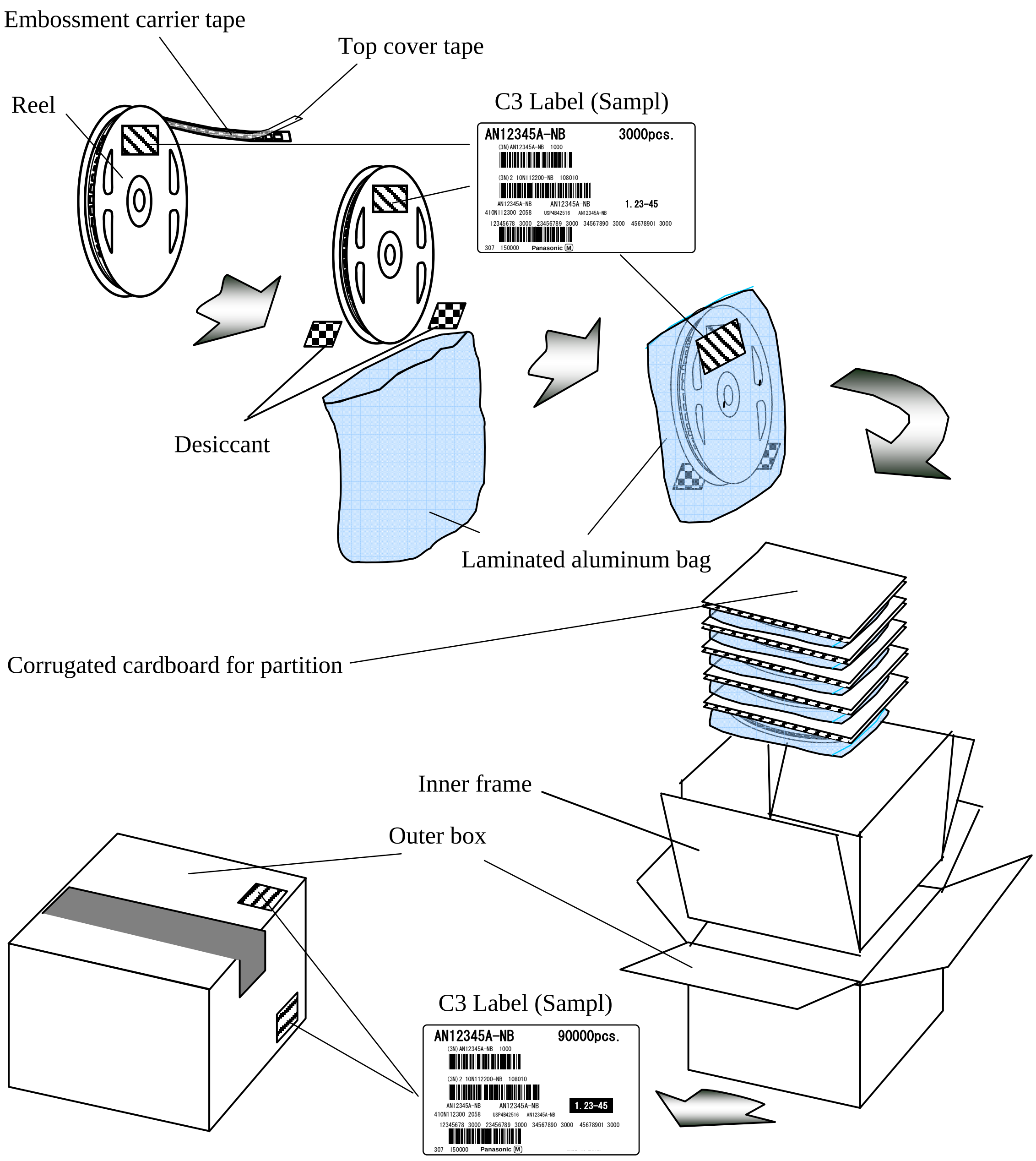
Note: Values within parentheses ( ) are recommended values.

※The above size is calculated based on the experiment results by Matsushita Electric Industrial Co., Ltd., and is not intended as a guarantee of mounting reliability. Mounting reliability can vary depending on factors such as the equipment specifications and conditions material specifications and properties , and environmental conditions. To ensure satisfactory results, your company should evaluate and confirm actual mounting performance.

2009.03.09		
Prepared	Revised	

Specifications of packing by the embossment tape

(Specifications for dampproof packing of the reel without the inner carton)



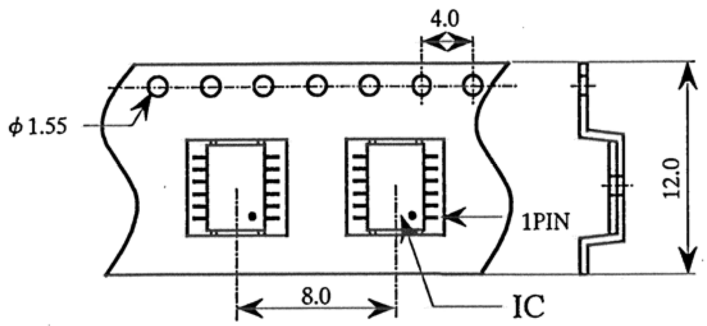
Package : SSOP016-P-0225E

Unit : mm

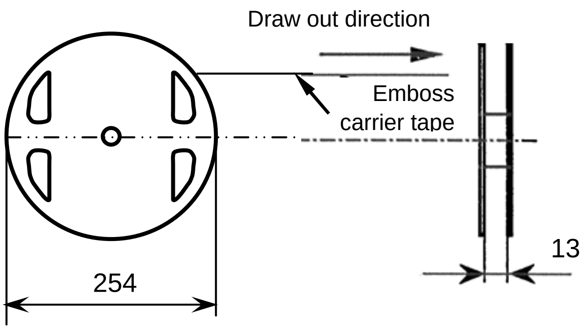
1 Packing

1) Tape

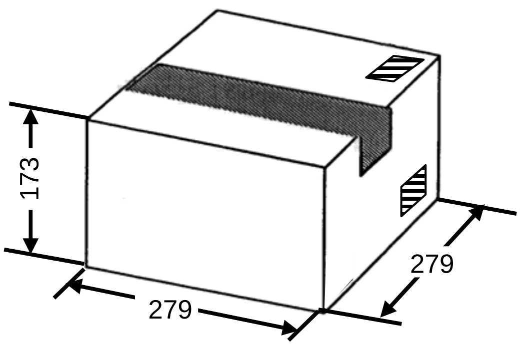
VF



2) Reel



3) Packing case



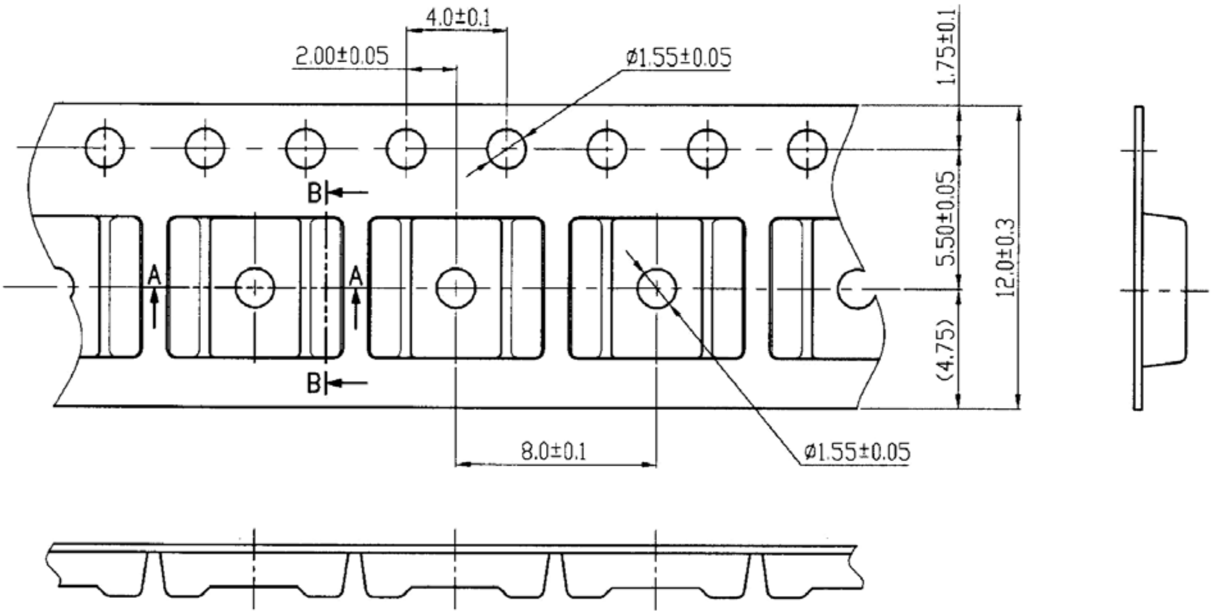
2 Packing quantity

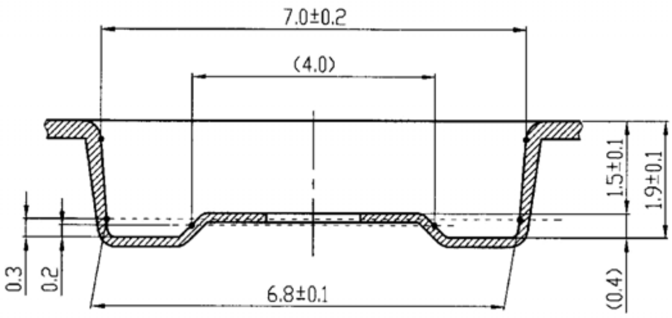
Form	IC quantity	Contents
Reel	2000 Pcs	Reel × 1Pcs
Packing case	10000 Pcs	Reel × 5Pcs

	Packing Specification	Total pages	page
			3

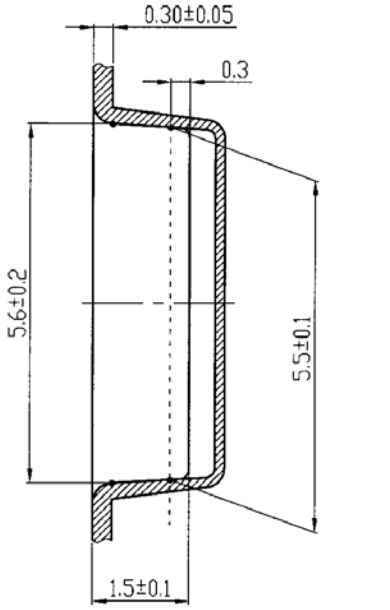
Package : SSOP016-P-0225E

Unit : mm





(A–A)



(B–B)

Prepared	Revised	

Panasonic

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