PIC16C432

PIC16C432 Data Sheet Errata

The PIC16C432 parts you have received conform functionally to the Device Data Sheet (DS41140**A**), except for the anomalies described below.

None.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41140**A**), the following clarifications and corrections should be noted.

The positions of LINTX and LINVDD are shown in Register 1.

REGISTER 1: LININTF REGISTER (ADDRESS 90h)

U-0	U-0	U-0	U-0	U-0	R/W-1	U-0	R/W-1
—	—	—	—	—	LINTX	—	LINVDD
bit 7							bit 0

bit 7-3 **Unimplemented:** Read as '0'

bit 2 **LINTX**: LIN Bus Transmit bit

1 = LIN Bus line is high
0 = LIN Bus line is low

bit 1 **Unimplemented**: Read as ’0’

bit 0 **LINVDD:** LIN Bus Transceiver V_{DD} Supply bit

1 = V_{DD} is supplied to the LIN Bus transceiver via microcontroller
0 = V_{DD} is not supplied to the LIN Bus transceiver

Note: Transceiver V_{DD} is same as microcontroller V_{DD}.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

The description of the BACT (Bus activity output) function in Table 3-1 has changed. Refer to updated Table 3-1:

TABLE 3-1: PIC16C432 PINOUT DESCRIPTION

Name	DIP/ SSOP Pin #	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	17	I	ST/CMOS	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	16	O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	5	I/P	ST	Master Clear (Reset) input/programming voltage input. This pin is an active low RESET to the device.
				PORTA is a bi-directional I/O port.
RA0/AN0	18	I/O	ST	Analog comparator input.
BACT	19	O	—	Bus activity output. No connection if not used. It is a CMOS-levels representation of the LIN pin
RA2/AN2/VREF	2	I/O	ST	Analog comparator input or VREF output.
RA3/AN3	3	I/O	ST	Analog comparator input/output.
RA4/T0CKI	4	I/O	ST	Can be selected to be the clock input to the Timer0 timer/ counter or a comparator output. Output is open drain type.
				PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	7	I/O	TTL/ST(1)	RB0/INT can also be selected as an external interrupt pin.
RB1	8	I/O	TTL	
RB2	9	I/O	TTL	
RB3	10	I/O	TTL	
RB4	11	I/O	TTL	Interrupt-on-change pin.
RB5	12	I/O	TTL	Interrupt-on-change pin.
RB6	13	I/O	TTL/ST(2)	Interrupt-on-change pin. Serial programming clock.
RB7	14	I/O	TTL/ST(2)	Interrupt-on-change pin. Serial programming data.
LIN	1	I/O	HV/OD	High Voltage Bi-directional Bus Interface.
VBAT	20	P	—	Battery Input Voltage.
VSS	6, 19	P	—	Ground reference for logic and I/O pins.
VDD	15	P	—	Positive supply for logic and I/O pins.

Legend: O = Output, I/O = Input/Output, P = Power
— = Not used, I = Input, ST = Schmitt Trigger input
TTL = TTL input, OD = Open Drain, HV = High Voltage

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

Page 27 of the Data Sheet, Section 6.2 LIN Bus Interfacing, Section 6.3 LIN Bus Hardware Interface and Section 6.5 Wake-up from SLEEP upon Bus Activity, have been changed to the following:

6.2 LIN Bus Interfacing

The LIN protocol is implemented and programmed by the user, using the LINTX and LINRX bits, which are used to interface to the transceiver. The LIN Bus firmware transmits by toggling the LINTX bit in the LININTF register and is read by reading the LINRX bit in the PORTA register. All aspects of the protocol are handled by software (i.e. bit-banged), where the transceiver is used as the physical interface to the LIN Bus network.

For an interrupt based LIN Bus slave implementation, please refer to AN729, available on Microchip's website (www.microchip.com). This application note is based on PIC16C622, but can be converted for either PIC16C432 or PIC16C433.

For the PIC16C432, the changes required include but are not limited to:

1. Change the include file to "`p16C432.inc`".
2. Use LINTX bit in LININTF register instead of TXLINEPIN in PORTB to transmit. Note LININTF is in bank 1.
3. Use LINRX bit in PORTA register instead of TXLINEPIN in PORTB to receive.
4. Connect the bus to LIN pin to receive and transmit instead of PORTB<0> and PORTB<4>.
5. Ensure that LINRX and LINVDD remain set.

Note:	The LINTX is bit 2 of the LININTF register and not bit 1 as documented in the PIC16C432 data sheet.

If the LINTX bit is left cleared, no other nodes on the network will be able to communicate on the LIN Bus for this is the dominate state for the protocol. The transceiver can be powered down by clearing the LINVDD bit in the LININTF register. This can be useful to reduce current consumption but does not allow the microcontroller to wake-up on LIN Bus activity because the transceiver will be disabled. It is recommended that the firmware verify each bit transmitted, by comparing the LINTX and LINRX bits, to ensure no bus contention or hardware failure has occurred. The LINTX bit has no associated TRIS bit and is always an output. The LINRX bit has an associated TRIS bit, TLINRX, in the TRISA register.

Note:	TLINRX, bit 1 of TRISA register, must be set to '1' at all times.

6.3 LIN Bus Hardware Interface

Figure 6-1 shows how to implement a hardware LIN Bus interface in a master configuration and Figure 6-2 in a slave configuration using the PIC16C432. Figure 6-3 shows how to implement the hardware for a master configuration using BACT pin to generate a wake-up interrupt using RB0. The transceiver has an internal series resistor and diode, as defined in the LIN 1.2 specification, connecting V_{BAT} and LIN.

Note:	No resistor is required between V_{BAT} pin and 12V supply and for slave configuration, no resistor is required between V_{BAT} and LIN.

6.5 Wake-up from SLEEP upon Bus Activity

The PIC16C432 can wake-up from SLEEP upon bus activity in two ways:

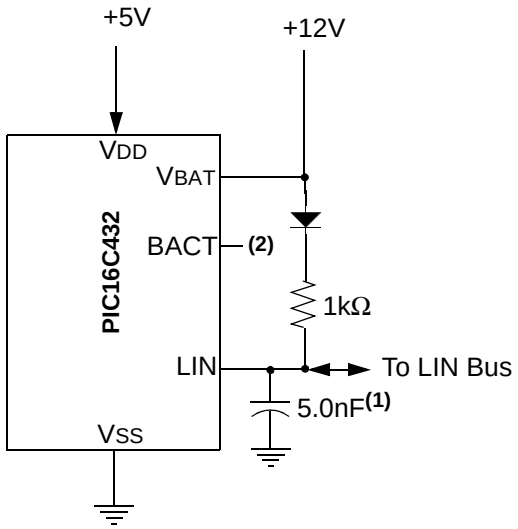
1. With the use of the comparators.
2. Connecting BACT to one of PORTB<0,4:7> pins.

In case the comparators are used to wake-up the device upon bus activity, a reference to the LIN Bus signal has to be supplied. This is usually $V_{DD}/2$. The reference can either be an external reference or the internal voltage reference. Once the device is in SLEEP mode, the comparator interrupt will wake-up the device. On RESET, LINRX is configured as an analog comparator input (Section 8.1 of Data Sheet) which can be used to generate an interrupt to wake-up the device from SLEEP on bus activity. The LINRX bit will not receive data from the bus configured as an analog input, therefore, after wake-up from comparator interrupt or RESET, LINRX must be configured as a digital input to read the bus.

The BACT output is a CMOS-levels representation of the LIN pin. This signal can be routed to one of the PORTB<0,4:7> pins. The RB0/INT external interrupt or PORTB<4:7> interrupt-on-change wakes up the device from SLEEP. Any one of the five PORTB pins can be used for wake-up where PORTB<0> offers multiple configuration options (Section 10.5.1 of Data Sheet) and PORTB<4:7> are interrupt-on-change (Section 10.5.3 of Data Sheet).

Note:	BACT pin is an output and must be left open if unused.

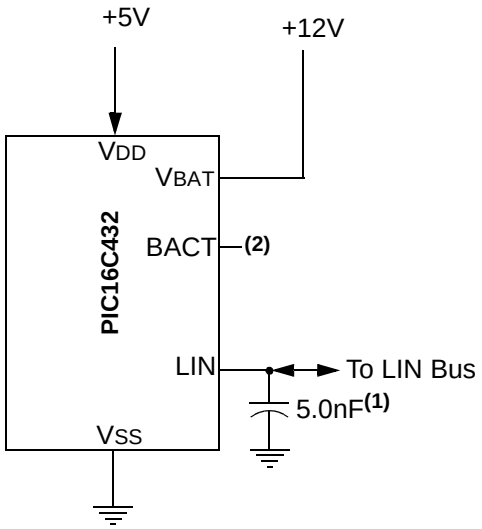
FIGURE 6-1: TYPICAL LIN BUS MASTER APPLICATION



Note 1: May not be required.
2: BACT pin should be left open if not used.

A new figure has been added to show LIN Bus slave configuration, Figure 6-2:

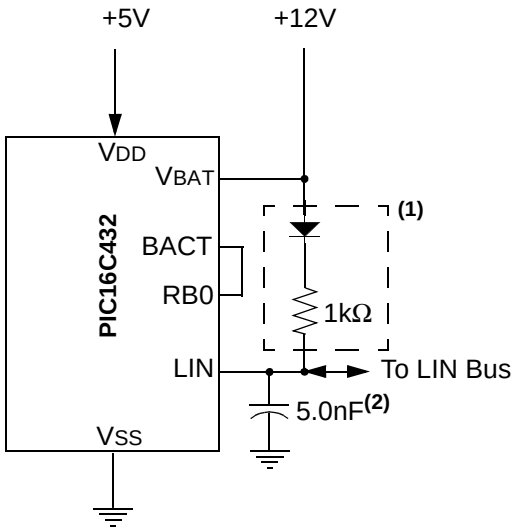
FIGURE 6-2: TYPICAL LIN BUS SLAVE APPLICATION



Note 1: May not be required.
2: BACT pin should be left open if not used.

A new figure has been added to show LIN Bus configuration using Wake-up interrupt, Figure 6-3:

FIGURE 6-3: LIN BUS APPLICATION USING WAKE-UP INTERRUPT



Note 1: For master configuration only.
2: May not be required.

TABLE 6-1: SUMMARY OF REGISTERS ASSOCIATED WITH LIN TRANSCEIVER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR	Value on All Other RESETS
05h	PORTA	—	—	—	RA4	RA3	RA2	LINRX	RA0	---x 0000	---u 0000
85h	TRISA	—	—	—	TRISA4	TRISA3	TRISA2	TLINRX(2)	TRISA0	---1 1111	---1 1111
90h	LININTF	—	—	—	—	—	LINTX	—	LINVDD	---- -1-1	---- -1-1

Legend: x = unknown, u = unchanged, — = Unimplemented locations read as '0'.

Note 1: Shaded bits are not used by LIN transceiver

2: TLINRX must be set to '1' at all times.

The Electrical Specifications have been changed to include the maximum current sunk by LIN and BACT pins, as shown in the following table in Section 13.0 of the PIC16C432 Data Sheet.

13.0 Electrical Specifications for PIC16C432

Absolute Maximum Ratings (†)

Ambient Temperature under bias ..... -40° to +125°C

Storage Temperature ..... -65° to +150°C

Voltage on any pin with respect to V_{SS} (except V_{DD} and $\overline{MCLR}$) .....-0.6V to V_{DD} +0.6V

Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.0V

Voltage on RA4 with respect to V_{SS}.....8.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} **(Note 2)** .....0 to +14V

Voltage on RA4 with respect to V_{SS}.....8.5V

Total power Dissipation **(Note 1)**.....1.0W

Maximum Current out of V_{SS} pin .....300 mA

Maximum Current into V_{DD} pin .....250 mA

Input Clamp Current, I_{IK} (V_I <0 or V_I> V_{DD}) .....±20 mA

Output Clamp Current, I_{OK} (V_O <0 or V_O>V_{DD}).....±20 mA

Maximum Output Current sunk by any I/O pin.....25 mA

Maximum Output Current sourced by any I/O pin.....25 mA

Maximum Current sunk by PORTA and PORTB.....200 mA

Maximum Current sourced by PORTA and PORTB.....200 mA

Maximum Current sunk by LIN.....200 mA

Maximum Current sunk by BACT.....1.8 mA

Note 1: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin, rather than pulling this pin directly to V_{SS}.

† **NOTICE**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

APPENDIX A: REVISION HISTORY

Rev. A Document (4/2001)

First revision of this document.

Rev. B Document (9/2001)

Under Clarifications/Corrections to the Data Sheet, corrections have been made to the following:

TABLE 3-1 - description of the BACT function.

Page 27:

Section 6.2 - LIN Bus Interfacing.

FIGURE 6-2 - added to show connections using Wake-up interrup.

Section 6.3 - LIN Bus Hardware Interface.

Section 6.5 - Wake-up from SLEEP upon Bus Activity.

13.0 Electrical Specifications for PIC16C432 - changed to include the maximum current sunk by LIN and BACT pins.

Rev. C Document (10/2001)

Change title of document from Rev. B Silicon Errata to Data Sheet Errata. Deleted ‘Rev. C’ from first paragraph, page 1.

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable".
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