

KA3882E/KA3883E

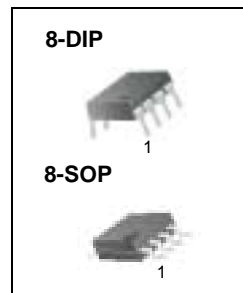
SMPS Controller

Features

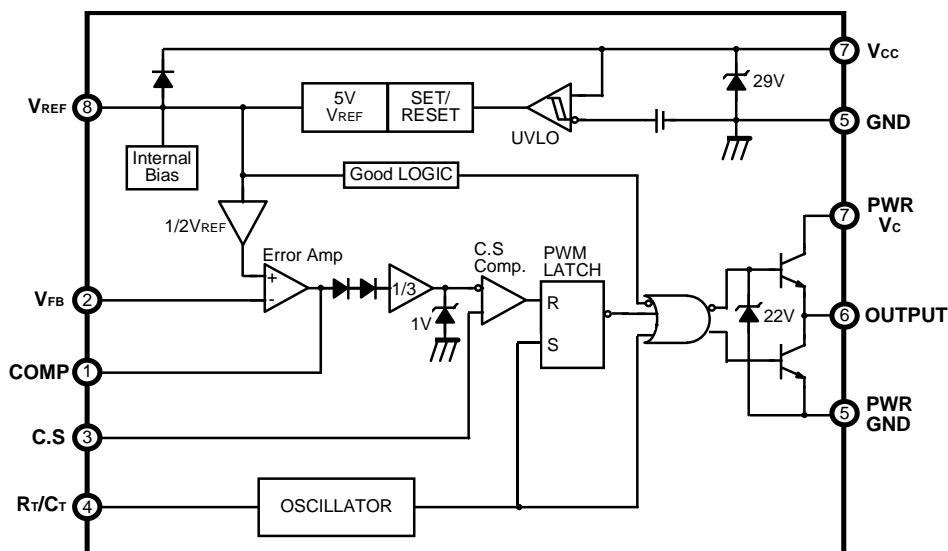
- Low start current 0.2mA (typ)
- Operating range up to 500kHz
- Cycle by cycle current limiting
- Under voltage lock out with hysteresis
- Short shutdown delay time: typ.100ns
- High current totem-pole output
- Output swing limiting: 22V

Description

The KA3882E/KA3883E is a fixed PWM controller for Off-Line and DC to DC converter applications. The internal circuits include a UVLO, a low start-up current circuit, a temperature compensated reference, a high gain error amplifier, a current sensing comparator, and the high current totem-pole output for driving a POWER MOSFET. Also the KA3882E/KA3883E provides low start-up current below 0.3mA and short shutdown delay time typ. 100ns. The KA3882E has UVLO threshold of 16V(on) and 10V(off). The KA3883E is 8.4V(on) and 7.6V(off). The KA3882E and KA3883E can operate within 100% duty cycle.



Internal Block Diagram



Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--|-----------------------|-------------|------|
| Supply voltage | V _{CC} | 30 | V |
| Output current | I _O | +1 | A |
| Analog inputs (pin2, 3) | V _{I(ANA)} | -0.3 to 6.3 | V |
| Error amp. output sink current | I _{SINK(EA)} | 10 | mA |
| Power dissipation | P _D | 1 | W |
| Thermal resistance, junction-to-air (Note4) 8-SOP 8-DIP | R _{θja} | 280 95 | °C/W |
| Storage temperature | T _{stg} | -65 ~ 150 | °C |

Electrical Characteristics

(V_{CC} = 15V, R_T = 10kΩ, C_T = 3.3nF, T_A = 0°C to +70°C, Unless otherwise specified)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|------------------------------|---------------------|---|------|------|------|------|
| REFERENCE SECTION | | | | | | |
| Output voltage | V _{REF} | T _J = 25°C, I _O = 1mA | 4.9 | 5.0 | 5.1 | V |
| Line regulation | R _{Line} | V _{CC} = 12V to 25V | - | 6 | 20 | mV |
| Load regulation | R _{LOAD} | I _O = 1mA to 20mA | - | 6 | 25 | mV |
| Output short circuit | I _{SC} | T _a = 25°C | - | -100 | -180 | mA |
| OSILLATOR SECTION | | | | | | |
| Initial accuracy | F _{OSC} | T _J = 25°C | 47 | 52 | 57 | kHz |
| Voltage stability | ST _V | V _{CC} = 12V to 25V | - | 0.2 | 1 | % |
| Amplitude | V _{OSC} | V _{PIN4} , peak to peak | - | 1.7 | - | V |
| Discharge current | I _{DISCHG} | T _J = 25°C | 7.8 | 8.3 | 8.8 | mA |
| CURRENT SENSE SECTION | | | | | | |
| Gain | G _V | (Note2, 3) | 2.85 | 3 | 3.15 | V/V |
| Maximum input signal | V _{I(MAX)} | V _{PIN1} = 5V(Note2) | 0.9 | 1.0 | 1.1 | V |
| PSRR | PSRR | V _{CC} = 12V to 25V (Note1, 2) | - | 70 | - | dB |
| Input bias current | I _{BIAS} | V _{SENSE} = 0V | - | -2 | -10 | uA |
| Delay to output | T _D | V _{PIN3} = 0 V to 2V (Note1) | - | 100 | 200 | ns |

Electrical Characteristics (Continued)(V_{CC} = 15V, R_T = 10kΩ, C_T = 3.3nF, T_A = 0°C to +70°C, Unless otherwise specified)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---------------------|---|------|------|------|------|
| ERROR AMPLIFIER SECTION | | | | | | |
| Input voltage | V _I | V _{PIN1} = 2.5V | 2.42 | 2.50 | 2.58 | V |
| Input bias current | I _{BIAS} | V _{FB} =0V | - | -0.3 | - 2 | μA |
| Open loop gain | G _{VO} | V _O = 2V to 4V (Note1) | 65 | 90 | - | dB |
| Unity gain bandwidth | GBW | T _J = 25°C (Note1) | 0.7 | 1 | - | MHz |
| PSRR | PSRR | V _{CC} = 12V to 25V (Note1) | 60 | 70 | - | dB |
| Output sink current | I _{SINK} | V _{PIN2} = 2.7V, V _{PIN1} = 1.1V | 2 | 6 | - | mA |
| Output source current | I _{SOURCE} | V _{PIN2} = 2.3V, V _{PIN1} = 5.0V | -0.5 | -0.8 | - | mA |
| Output high voltage | V _{OH} | V _{PIN2} = 2.3V, R ₁ = 15kΩ to GND | 5 | 6 | - | V |
| Output low voltage | V _{OL} | V _{PIN2} = 2.7V, R ₁ = 15kΩ to V _{ref} | - | 0.8 | 1.1 | V |
| OUTPUT SECTION | | | | | | |
| Output low level | V _{OL} | I _{SINK} = 20mA | - | 0.1 | 0.4 | V |
| | | I _{SINK} = 200mA | - | 1.5 | 2.2 | V |
| Output high level | V _{OH} | I _{SOURCE} = 20mA | 13 | 13.5 | - | V |
| | | I _{SOURCE} = 200mA | 12 | 13.5 | - | V |
| Rise time | t _R | T _J = 25°C, C ₁ = 1nF (Note1) | - | 40 | 100 | ns |
| Fall time | t _F | T _J = 25°C, C ₁ = 1nF (Note1) | - | 40 | 100 | ns |
| Output voltage swing limit | V _{OLIM} | V _{CC} = 27V, C ₁ = 1nF | - | 22 | - | V |
| UNDER VOLTAGE LOCKOUT SECTION | | | | | | |
| Start threshold | V _{TH} | KA3882E | 15 | 16 | 17 | V |
| | | KA3883E | 7.8 | 8.4 | 9.0 | V |
| Min. operating voltage (after turn on) | V _{TL} | KA3882E | 9 | 10 | 11 | V |
| | | KA3883E | 7.0 | 7.6 | 8.2 | V |
| PWM SECTION | | | | | | |
| Maximum duty cycle | D _{MAX} | KA3882E/KA3883E | 94 | 96 | 100 | % |
| Minimum duty cycle | D _{MIN} | - | - | - | 0 | % |
| TOTAL STANDBY CURRENT | | | | | | |
| Start-up current | I _{ST} | - | - | 0.2 | 0.4 | mA |
| Operating supply current | I _{CC} | V _{PIN2} = V _{PIN3} = 0V | - | 11 | 17 | mA |
| V _{CC} zener voltage | V _Z | I _{CC} = 25mA | - | 29 | - | V |

* Adjust V_{CC} above the start threshold before setting at 15V**Notes :**

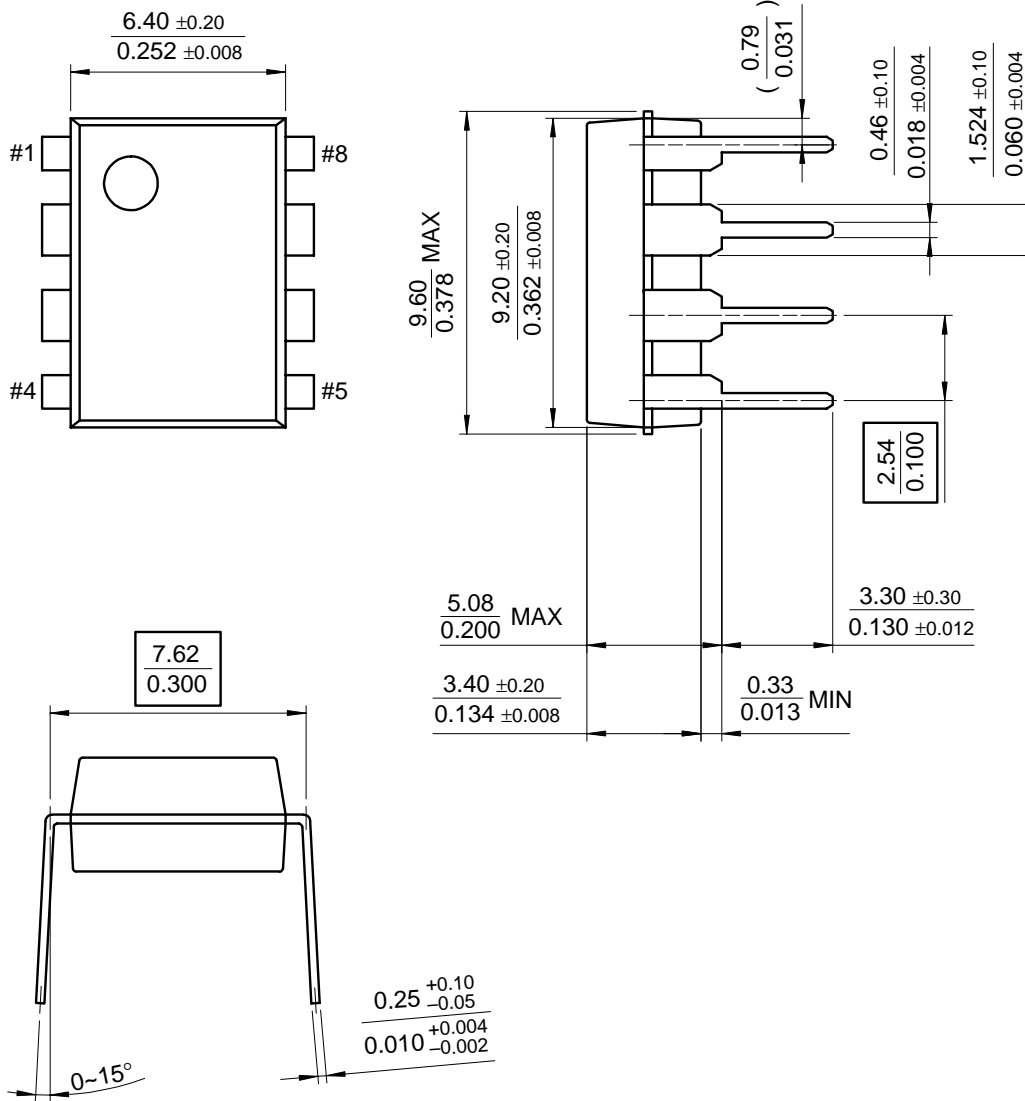
- These parameters, although guaranteed, are not 100% tested in production.
- Parameter measured at trip point of latch with V_{FB} = 0V.
- Gain defined as: $G_V = \frac{\Delta V_{COMP}}{\Delta V_{SENSE}}$; $0 \leq V_{SENSE} \leq 0.8V$
- Junction-to-air thermal resistance test environments.
 - PCB information ;
Board thickness : 1.6mm , Board dimension : 76.2 X 114.3mm² , Ref. : EIA / JSED51-3 and EIA / JSED51-7
 - Board structure; Using the single layer PCB.

Mechanical Dimensions

Package

Dimensions in millimeters

8-DIP

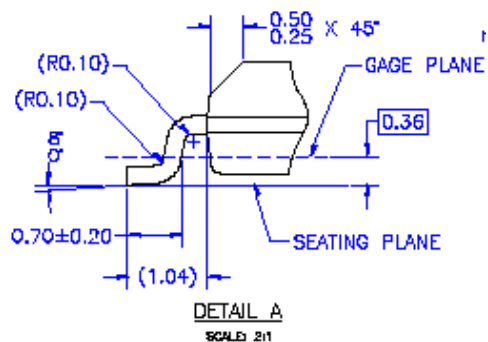
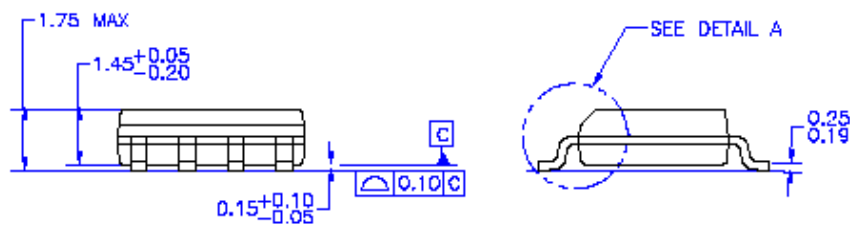
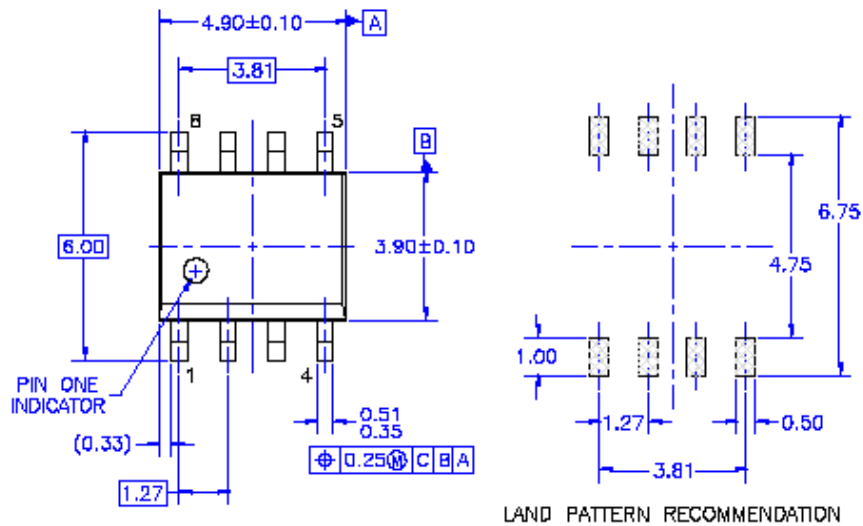


Mechanical Dimensions (Continued)

Package

Dimensions in millimeters

8-SOP



Ordering Information

| Product Number | Package | Operating Temperature |
|----------------|---------|-----------------------|
| KA3882E | 8-DIP | 0 ~ +70°C |
| KA3882ED | 8-SOP | |
| KA3883E | 8-DIP | |
| KA3883ED | 8-SOP | |

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