User's Manual

16

R8C/3MQ Group

User's Manual: Hardware

RENESAS MCU
R8C Family / R8C/3x Series

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.
The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the R8C/3MQ Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Datasheet	Hardware overview and electrical characteristics	R8C/3MQ Group Datasheet	R01DS0044EJ0100
User's manual: Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation description Note: Refer to the application notes for details on using peripheral functions.	R8C/3MQ Group User's Manual: Hardware	This User's manual
User's manual: Software	Description of CPU instruction set	R8C/Tiny Series Software Manual	REJ09B0001
Application note	Information on using peripheral functions and application examples Sample programs Information on writing programs in assembly language and C	Available from Renesas Electronics Web site.	
Renesas technical update	Product specifications, updates on documents, etc.		

2. Notation of Numbers and Symbols

The notation conventions for register names, bit names, numbers, and symbols used in this manual are described below.

(1) Register Names, Bit Names, and Pin Names
Registers, bits, and pins are referred to in the text by symbols. The symbol is accompanied by the word “register,” “bit,” or “pin” to distinguish the three categories.
Examples the PM03 bit in the PM0 register
P3_5 pin, VCC pin

(2) Notation of Numbers
The indication “b” is appended to numeric values given in binary format. However, nothing is appended to the values of single bits. The indication “h” is appended to numeric values given in hexadecimal format. Nothing is appended to numeric values given in decimal format.
Examples Binary: 11b
Hexadecimal: EFA0h
Decimal: 1234

3. Register Notation

The symbols and terms used in register diagrams are described below.

x.x.x XXX Register (Symbol)

Address XXXXh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	XXX7	XXX6	XXX5	XXX4	—	—	XXX1	XXX0
After Reset	0	0	0	0	0	0	0	0

*1

Bit	Symbol	Bit Name	Function	R/W
b0	XXX0	XXX bit	b1 b0 0 0: XXX 0 1: XXX 1 0: Do not set. 1 1: XXX	R/W
b1	XXX1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	—	Reserved bit	Set to 0.	R/W
b4	XXX4	XXX bit	Function varies according to the operating mode.	R/W
b5	XXX5			W
b6	XXX6			R/W
b7	XXX7	XXX bit	0: XXX 1: XXX	R

*2 *3

*1

R/W: Read and write.
R: Read only.
W: Write only.
—: Nothing is assigned.

*2

- Reserved bit

  Reserved bit. Set to specified value.

*3

- Nothing is assigned.

  Nothing is assigned to the bit. As the bit may be used for future functions, if necessary, set to 0.
- Do not set to a value.

  Operation is not guaranteed when a value is set.
- Function varies according to the operating mode.

  The function of the bit varies with the peripheral function mode. Refer to the register diagram for information on the individual modes.

4. List of Abbreviations and Acronyms

Abbreviation	Full Form
ACIA	Asynchronous Communication Interface Adapter
bps	bits per second
CRC	Cyclic Redundancy Check
DMA	Direct Memory Access
DMAC	Direct Memory Access Controller
GSM	Global System for Mobile Communications
Hi-Z	High Impedance
IEBus	Inter Equipment Bus
I/O	Input/Output
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NC	Non-Connection
PLL	Phase Locked Loop
PWM	Pulse Width Modulation
SIM	Subscriber Identity Module
UART	Universal Asynchronous Receiver/Transmitter
VCO	Voltage Controlled Oscillator

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Table of Contents

SFR Page Reference

Address	Register	Symbol	Page
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	29
0005h	Processor Mode Register 1	PM1	160
0006h	System Clock Control Register 0	CM0	92
0007h	System Clock Control Register 1	CM1	93
0008h	Module Standby Control Register	MSTCR	229, 317, 348
0009h	System Clock Control Register 3	CM3	94
000Ah	Protect Register	PRCR	117
000Bh	Reset Source Determination Register	RSTFR	29
000Ch	Oscillation Stop Detection Register	OCD	95
000Dh	Watchdog Timer Reset Register	WDTR	160
000Eh	Watchdog Timer Start Register	WDTS	160
000Fh	Watchdog Timer Control Register	WDTC	161
0010h			
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	161
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	96
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h	Voltage Monitor Circuit Control Register	CMPA	41
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	42
0032h			
0033h			
0034h	Voltage Detect Register 2	VCA2	43, 96
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	44
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	45
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	46
003Ah	WDT Detection Flag	VW2C	47
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	125
0042h	BB Timer Compare 2 Interrupt Control Register	BBTIM2IC	124
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	125
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	124
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	124
004Eh			
004Fh	SSU Interrupt Control Register/IIC bus Interrupt Control Register	SSUIC/IICIC	125
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	124
0052h	UART0 Receive Interrupt Control Register	S0RIC	124
0053h			
0054h	Bank 0 Receive Complete/IDLE Interrupt Control Register	BBRX0IC/BBIDLEIC	124
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	124
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	124
0059h	INT1 Interrupt Control Register	INT1IC	126
005Ah	INT3 Interrupt Control Register	INT3IC	126
005Bh			
005Ch	BB Timer Compare 1 Interrupt Control Register	BBTIM1IC	124
005Dh	INT0 Interrupt Control Register	INT0IC	126
005Eh	CCA Complete Interrupt Control Register	BBCCAIC	124
005Fh	BB Timer Compare 0 Interrupt Control Register	BBTIM0IC	124
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch	Address Filter Interrupt Control Register	BBADFIC	124
006Dh	Transmit Overrun Interrupt Control Register	BBTXORIC	124
006Eh	Transmission Complete Interrupt Control Register	BBTXIC	124
006Fh	Receive Overrun 1 Interrupt Control Register	BBRXOR1IC	124
0070h	PLL Lock Detection Interrupt Control Register	BBPLLIC	124
0071h	Receive Overrun 0/Calibration Complete Interrupt Control Register	BBRXOR0IC/ BBCALIC	124
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	124
0073h	Bank 1 Reception Complete/Clock Regulator Interrupt Control Register	BBRX1IC/BBCREGIC	124
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

Address	Register	Symbol	Page
0080h	DTC Activation Control Register	DTCTL	172
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	171
0089h	DTC Activation Enable Register 1	DTCEN1	171
008Ah	DTC Activation Enable Register 2	DTCEN2	171
008Bh	DTC Activation Enable Register 3	DTCEN3	171
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	171
008Eh	DTC Activation Enable Register 6	DTCEN6	171
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	294
00A1h	UART0 Bit Rate Register	U0BRG	294
00A2h	UART0 Transmit Buffer Register	U0TB	295
00A3h			
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	296
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	296
00A6h	UART0 Receive Buffer Register	U0RB	297
00A7h			
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			
:			
00E0h	Port P0 Register	P0	66
00E1h	Port P1 Register	P1	66
00E2h	Port P0 Direction Register	PD0	65
00E3h	Port P1 Direction Register	PD1	65
00E4h			
00E5h	Port P3 Register	P3	66
00E6h			
00E7h	Port P3 Direction Register	PD3	65
00E8h	Port P4 Register	P4	66
00E9h			
00EAh	Port P4 Direction Register	PD4	65
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			

Note:
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Address	Register	Symbol	Page
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			
0100h	Timer RA Control Register	TRACR	190
0101h	Timer RA I/O Control Register	TRAIOC	190, 193, 196, 198, 200, 203
0102h	Timer RA Mode Register	TRAMR	191
0103h	Timer RA Prescaler Register	TRAPRE	191
0104h	Timer RA Register	TRA	192
0105h			
0106h			
0107h			
0108h	Timer RB Control Register	TRBCR	207
0109h	Timer RB One-Shot Control Register	TRBOCR	207
010Ah	Timer RB I/O Control Register	TRBIOC	208, 211, 215, 218, 222
010Bh	Timer RB Mode Register	TRBMR	208
010Ch	Timer RB Prescaler Register	TRBPRE	209
010Dh	Timer RB Secondary Register	TRBSC	209
010Eh	Timer RB Primary Register	TRBPR	210
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	277, 285
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	277, 285
011Ah	Timer RE Hour Data Register	TREHR	278
011Bh	Timer RE Day of Week Data Register	TREWK	278
011Ch	Timer RE Control Register 1	TRECR1	279, 286
011Dh	Timer RE Control Register 2	TRECR2	280, 286
011Eh	Timer RE Count Source Select Register	TRECSR	281, 287
011Fh			
0120h	Timer RC Mode Register	TRCMR	230
0121h	Timer RC Control Register 1	TRCCR1	231, 251, 260, 266
0122h	Timer RC Interrupt Enable Register	TRCIER	231
0123h	Timer RC Status Register	TRCSR	232
0124h	Timer RC I/O Control Register 0	TRCIOR0	233, 246, 252
0125h	Timer RC I/O Control Register 1	TRCIOR1	233, 247, 253
0126h	Timer RC Counter	TRC	234
0127h			
0128h	Timer RC General Register A	TRCGRA	234
0129h			
012Ah	Timer RC General Register B	TRCGRB	234
012Bh			
012Ch	Timer RC General Register C	TRCGRC	234
012Dh			
012Eh	Timer RC General Register D	TRCGRD	234
012Fh			

Address	Register	Symbol	Page
0130h	Timer RC Control Register 2	TRCCR2	235, 254, 261, 267
0131h	Timer RC Digital Filter Function Select Register	TRCDF	235, 268
0132h	Timer RC Output Master Enable Register	TRCOER	236
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			
:			
0180h	Timer RA Pin Select Register	TRASR	67, 192
0181h	Timer RB/RC Pin Select Register	TRBRCSR	67, 210, 236
0182h	Timer RC Pin Select Register 0	TRCPSR0	68, 237
0183h	Timer RC Pin Select Register 1	TRCPSR1	68, 237
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	69, 298
0189h			
018Ah			
018Bh			
018Ch	SSU/IIC Pin Select Register	SSUIICSR	69, 317, 348
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	70, 135
018Fh	I/O Function Pin Select Register	PINSR	71, 97, 349
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	318
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register	SSTDR / ICDRT	318, 350
0195h	SS Transmit Data Register H	SSTDRH	
0196h	SS Receive Data Register L / IIC bus Receive Data Register	SSRDR / ICDRR	319, 350
0197h	SS Receive Data Register H	SSRDRH	
0198h	SS Control Register H / IIC bus Control Register 1	SSCRH / ICCR1	319, 351
0199h	SS Control Register L / IIC bus Control Register 2	SSCRL / ICCR2	320, 352
019Ah	SS Mode Register / IIC bus Mode Register	SSMR / ICMR	321, 353
019Bh	SS Enable Register / IIC bus Interrupt Enable Register	SSER / ICIER	322, 354
019Ch	SS Status Register / IIC bus Status Register	SSSR / ICSR	323, 355
019Dh	SS Mode Register 2 / Slave Address Register	SSMR2 / SAR	324, 356
019Eh			
019Fh			
:			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	444
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	446
01B5h	Flash Memory Control Register 1	FMR1	449
01B6h	Flash Memory Control Register 2	FMR2	451
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

Address	Register	Symbol	Page
01C0h	Address Match Interrupt Register 0	RMAD0	144
01C1h			
01C2h			
01C3h	Address Match Interrupt Enable Register 0	AIER0	144
01C4h	Address Match Interrupt Register 1	RMAD1	144
01C5h			
01C6h			
01C7h	Address Match Interrupt Enable Register 1	AIER1	144
01C8h			
:			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	72
01E1h	Pull-Up Control Register 1	PUR1	72
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	73
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	74
01F3h	Drive Capacity Control Register 1	DRR1	75
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	76
01F6h	Input Threshold Control Register 1	VLT1	77
01F7h			
01F8h			
01F9h			
01FAh	External Input Enable Register 0	INTEN	136
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	137
01FDh			
01FEh	Key Input Enable Register 0	KIEN	141
01FFh	Key Input Enable Register 1	KIEN1	142
0200h			
:			
D2FFh			
2C00h	DTC Transfer Vector Area		
2C01h	DTC Transfer Vector Area		
2C02h	DTC Transfer Vector Area		
2C03h	DTC Transfer Vector Area		
2C04h	DTC Transfer Vector Area		
2C05h	DTC Transfer Vector Area		
2C06h	DTC Transfer Vector Area		
2C07h	DTC Transfer Vector Area		
2C08h	DTC Transfer Vector Area		
2C09h	DTC Transfer Vector Area		
2C0Ah	DTC Transfer Vector Area		
:	DTC Transfer Vector Area		
:	DTC Transfer Vector Area		
2C3Ah	DTC Transfer Vector Area		
2C3Bh	DTC Transfer Vector Area		
2C3Ch	DTC Transfer Vector Area		
2C3Dh	DTC Transfer Vector Area		
2C3Eh	DTC Transfer Vector Area		
2C3Fh	DTC Transfer Vector Area		

Note:
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Address	Register	Symbol	Page
2C40h	DTC Control Data 0	DTCD0	
2C41h			
2C42h			
2C43h			
2C44h			
2C45h			
2C46h			
2C47h			
2C48h	DTC Control Data 1	DTCD1	
2C49h			
2C4Ah			
2C4Bh			
2C4Ch			
2C4Dh			
2C4Eh			
2C4Fh			
2C50h	DTC Control Data 2	DTCD2	
2C51h			
2C52h			
2C53h			
2C54h			
2C55h			
2C56h			
2C57h			
2C58h	DTC Control Data 3	DTCD3	
2C59h			
2C5Ah			
2C5Bh			
2C5Ch			
2C5Dh			
2C5Eh			
2C5Fh			
2C90h	DTC Control Data 10	DTCD10	
2C91h			
2C92h			
2C93h			
2C94h			
2C95h			
2C96h			
2C97h			
2C98h	DTC Control Data 11	DTCD11	
2C99h			
2C9Ah			
2C9Bh			
2C9Ch			
2C9Dh			
2C9Eh			
2C9Fh			
2C60h	DTC Control Data 4	DTCD4	
2C61h			
2C62h			
2C63h			
2C64h			
2C65h			
2C66h			
2C67h			
2C68h	DTC Control Data 5	DTCD5	
2C69h			
2C6Ah			
2C6Bh			
2C6Ch			
2C6Dh			
2C6Eh			
2C6Fh			

Address	Register	Symbol	Page
2C70h	DTC Control Data 6	DTCD6	
2C71h			
2C72h			
2C73h			
2C74h			
2C75h			
2C76h			
2C77h			
2C78h	DTC Control Data 7	DTCD7	
2C79h			
2C7Ah			
2C7Bh			
2C7Ch			
2C7Dh			
2C7Eh			
2C7Fh			
2C80h	DTC Control Data 8	DTCD8	
2C81h			
2C82h			
2C83h			
2C84h			
2C85h			
2C86h			
2C87h			
2C88h	DTC Control Data 9	DTCD9	
2C89h			
2C8Ah			
2C8Bh			
2C8Ch			
2C8Dh			
2C8Eh			
2C8Fh			
2CA0h	DTC Control Data 12	DTCD12	
2CA1h			
2CA2h			
2CA3h			
2CA4h			
2CA5h			
2CA6h			
2CA7h			
2CA8h	DTC Control Data 13	DTCD13	
2CA9h			
2CAAh			
2CABh			
2CACh			
2CADh			
2CAEh			
2CAFh			
2CB0h	DTC Control Data 14	DTCD14	
2CB1h			
2CB2h			
2CB3h			
2CB4h			
2CB5h			
2CB6h			
2CB7h			
2CB8h	DTC Control Data 15	DTCD15	
2CB9h			
2CBAh			
2CBBh			
2CBCh			
2CBDh			
2CBEh			
2CBFh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
2CC0h	DTC Control Data 16	DTCD16	
2CC1h			
2CC2h			
2CC3h			
2CC4h			
2CC5h			
2CC6h			
2CC7h			
2CC8h	DTC Control Data 17	DTCD17	
2CC9h			
2CCAh			
2CCBh			
2CCCh			
2CCDh			
2CCEh			
2CCFh			
2CD0h	DTC Control Data 18	DTCD18	
2CD1h			
2CD2h			
2CD3h			
2CD4h			
2CD5h			
2CD6h			
2CD7h			
2CD8h	DTC Control Data 19	DTCD19	
2CD9h			
2CDAh			
2CDBh			
2CDCh			
2CDDh			
2CDEh			
2CDFh			
2CE0h	DTC Control Data 20	DTCD20	
2CE1h			
2CE2h			
2CE3h			
2CE4h			
2CE5h			
2CE6h			
2CE7h			
2CE8h	DTC Control Data 21	DTCD21	
2CE9h			
2CEAh			
2CEBh			
2CECh			
2CEDh			
2CEEh			
2CEFh			
2CF0h	DTC Control Data 22	DTCD22	
2CF1h			
2CF2h			
2CF3h			
2CF4h			
2CF5h			
2CF6h			
2CF7h			
2CF8h	DTC Control Data 23	DTCD23	
2CF9h			
2CFAh			
2CFBh			
2CFCh			
2CFDh			
2CFEh			
2CFFh			

Address	Register	Symbol	Page
2D00h	Baseband Control Register	BBCON	397
2D01h	Transmit/Receive Reset Register	BBTXRXRST	398
2D02h	Transmit/Receive Mode Register 0	BBTXRXMODE0	399
2D03h	Transmit/Receive Mode Register 1	BBTXRXMODE1	400
2D04h	Receive Frame Length Register	BBRXFLEN	401
2D05h	Receive Data Counter Register	BBRXCOUNT	402
2D06h	RSSI/CCA Result Register	BBRSSICCARSLT	403
2D07h	Transmit/Receive Status Register 0	BBTXRXST0	404
2D08h	Transmit Frame Length Register	BBTXFLEN	406
2D09h	Transmit/Receive Mode Register 2	BBTXRXMODE2	407
2D0Ah	Transmit/Receive Mode Register 3	BBTXRXMODE3	408
2D0Bh	Receive Level Threshold Set Register	BBLVLVTH	409
2D0Ch	Transmit/Receive Control Register	BBTXRXCON	410
2D0Dh	CSMA Control Register 0	BBCSMACON0	411
2D0Eh	CCA Level Threshold Set Register	BBCCAVTH	412
2D0Fh	Transmit/Receive Status Register 1	BBTXRXST1	413
2D10h	RF Control Register	BBRFCON	414
2D11h	Transmit/Receive Mode Register 4	BBTXRXMODE4	415
2D12h	CSMA Control Register 1	BBCSMACON1	417
2D13h	CSMA Control Register 2	BBCSMACON2	417
2D14h	PAN Identifier Register	BBPANID	418
2D15h			
2D16h	Short Address Register	BBSHORTAD	418
2D17h			
2D18h	Extended Address Register	BBEXTENDAD0	419
2D19h			
2D1Ah		BBEXTENDAD1	419
2D1Bh			
2D1Ch		BBEXTENDAD2	419
2D1Dh			
2D1Eh		BBEXTENDAD3	419
2D1Fh			
2D20h	Timer Read-Out Register 0	BBTIMEREAD0	420
2D21h			
2D22h	Timer Read-Out Register 1	BBTIMEREAD1	420
2D23h			
2D24h	Timer Compare 0 Register 0	BBCOMP0REG0	421
2D25h			
2D26h	Timer Compare 0 Register 1	BBCOMP0REG1	421
2D27h			
2D28h	Timer Compare 1 Register 0	BBCOMP1REG0	421
2D29h			
2D2Ah	Timer Compare 1 Register 1	BBCOMP1REG1	421
2D2Bh			
2D2Ch	Timer Compare 2 Register 0	BBCOMP2REG0	421
2D2Dh			
2D2Eh	Timer Compare 2 Register 1	BBCOMP2REG1	421
2D2Fh			
2D30h	Time Stamp Register 0	BBTSTAMP0	422
2D31h			
2D32h	Time Stamp Register 1	BBTSTAMP1	422
2D33h			
2D34h	Timer Control Register	BBTIMECON	423
2D35h	Backoff Period Register	BBBOFFPROD	424
2D36h			
2D37h			
2D38h			
2D39h			
2D3Ah	PLL Division Register 0	BBPLLDIVL	425
2D3Bh	PLL Division Register 1	BBPLLDIVH	425
2D3Ch	Transmit Output Power Register	BBTXOUTPWR	426
2D3Dh	RSSI Offset Register	BBRSSIOFS	427
2D3Eh			
2D3Fh			

Note:
1. The blank regions are reserved. Do not access locations in these regions.

Address	Register	Symbol	Page
2D40h			
:			
2D45h			
2D46h	Automatic ACK Response Timing Adjustment Register	BBACKRTNTIMG	431
2D47h			
:			
2D63h			
2D64h			
2D65h			
2D66h			
2D67h			
2D68h	Verification Mode Set Register	BBEVAREG	428
2D69h			
2D6Ah			
2D6Bh			
2D6Ch			
2D6Dh			
2D6Eh			
2D6Fh			
2D70h			
2D71h			
2D72h			
2D73h			
2D74h			
2D75h			
2D76h	IDLE Wait Set Register	BBIDELWAIT	429
2D77h			
2D78h			
2D79h			
2D7Ah	ANTSW Output Timing Set Register	BBANTSWTIMG	429
2D7Bh			
2D7Ch	RF Initial Set Register	BBRFINI	430
2D7Dh			
2D7Eh			
2D7Fh			
2D80h			
2D81h			
2D82h	ANTSW Control Register	BBANTSWCON	431
2D83h			
:			
2DFFh			
2E00h	Transmit RAM	TRANSMIT_RAM_START	
:	Transmit RAM		
2E7Eh	Transmit RAM	TRANSMIT_RAM_END	
2E7Fh			
2D80h	Receive RAM	RECIEVE_RAM_START	
:	Receive RAM		
2EFEh	Receive RAM	RECIEVE_RAM_END	
2EFFh			
2F00h			
:			
2FFFh			
:			
FFDBh	Option Function Select Register 2	OFS2	31, 156, 163
:			
FFFFh	Option Function Select Register	OFS	30, 48, 155, 162, 442

1. Overview

1.1 Features

The R8C/3MQ Group single-chip MCU functions as a low-power-consumption transceiver which supports 2.4 GHz compliant to IEEE802.15.4 standard and incorporates the R8C CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.
Power consumption is low, and the supported operating modes allow additional power control.
Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.
The R8C/3MQ Group has data flash (1 KB × 4 blocks) with the background operation (BGO) function.

1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/3MQ Group.

Table 1.1 Specifications for R8C/3MQ Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 62.5 ns (f(BCLK) = 16 MHz, VCC = 2.7 to 3.6 V) 125 ns (f(BCLK) = 8 MHz, VCC = 2.15 to 3.6 V) 250 ns (f(BCLK) = 4 MHz, VCC = 1.8 to 3.6 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.4 Product List for R8C/3MQ Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 2 (detection level selectable)
I/O Ports	Programmable I/O ports	CMOS I/O ports: 18 (including XCIN and XCOUT), selectable pull-up resistor (for some ports)
Clock	Clock generation circuits	• 3 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, low-speed clock, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		• Interrupt Vectors: 69 • External: 11 sources ($\overline{\text{INT}}$ × 3, key input × 8) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 17 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode

Table 1.2 Specifications for R8C/3MQ Group (2)

Item	Function	Specification
Serial Interface (UART0)		Shared with clock synchronous serial I/O mode and clock asynchronous serial I/O
Synchronous Serial Communication Unit (SSU)		1 (shared with I²C bus)
I²C bus		1 (shared with SSU)
RF	RF frequency	2405 MHz to 2480 MHz
	Reception sensitivity	-95 dBm
	Transmission output level	0 dBm
Baseband		• 127-byte transmit RAM, 127-byte receive RAM × 2 • Automatic ACK response function • 26-bit timer: Compare function in 3 channels
Encryption	AES	AES Encryption/Decryption (Key length 128bits)
Flash Memory		• Programming and erasure voltage: VCC = 1.8 to 3.6 V (in CPU rewrite mode) • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function
Operating Frequency/ Supply Voltage (in single mode)		f(BCLK) = 16 MHz, VCC = 2.7 to 3.6 V) f(BCLK) = 8 MHz (VCC = 2.15 to 3.6V) f(BCLK) = 4 MHz, VCC = 1.8 to 3.6 V) Note: f(XIN) = fixed at 16 MHz

Table 1.3 Specifications for R8C/3MQ Group (3)

Item	Function	Specification
Current Consumption (1)		RF = Tx: 18 mA RF = Rx (reception in progress): 25 mA RF = Rx (reception standby): 24 mA RF = Rx (reception standby)/wait mode: 23 mA RF = idle: 4 mA RF = off: 2.5 mA *The above applies when: f(XIN) = 16 MHz, f(BCLK)= 4 MHz, and VCC = VCCRF = 1.8 to 3.6 V
		RF = Tx: 19 mA RF = Rx (reception in progress): 26 mA RF = Rx (reception standby): 25 mA RF = Rx (reception standby)/wait mode: 23 mA RF = idle: 5 mA RF = off: 3.5 mA *The above applies when: f(XIN) = 16 MHz, f(BLCK) = 8 MHz, and VCC = VCCRF = 2.15 to 3.6 V
		RF = Tx: 21.5 mA RF = Rx (reception in progress): 28.5 mA RF = Rx (reception standby): 27.5 mA RF = Rx (reception standby)/wait mode: 23 mA RF = idle: 7.5 mA RF = off: 6 mA *The above applies when: f(XIN) = 16 MHz, f(BLCK) = 16 MHz, and VCC = VCCRF = 2.7 to 3.6 V
		Low-speed on-chip oscillator mode (f(BCLK) = 15.6 kHz): 80 μA Low-speed clock mode (f(BCLK) = 32 kHz, flash memory low-power-consumption mode): 95 μA Low-speed clock mode (f(BCLK) = 32 kHz, flash memory off/program operation on RAM: 45 μA Wait mode (system clock = XCIN (32 kHz)), peripheral function clock on: 6 μA Wait mode (system clock = XCIN (32 kHz)), peripheral function clock off: 4.5 μA Wait mode (system clock = fOCO-S (125 kHz)), peripheral function clock on: 13 μA Wait mode (system clock = fOCO-S (125 kHz)), peripheral function clock off: 7.5 μA Stop mode (all clocks off): 2 μA *When VCC = VCCRF = 1.8 to 3.6 V and RF = off
Operating Ambient Temperature		−20°C to 85°C (N version)
Package		40-pin HWQFN Package code: PWQN0040KB-A (previous code: 40PJS-A)

Note:
1. Refer to **28. Electrical Characteristics** for details on the measurement conditions.

1.2 Product List

Table 1.4 lists Product List for R8C/3MQ Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/3MQ Group.

Table 1.4 Product List for R8C/3MQ Group **Current of Jun 2012**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F213M6QNNP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PWQN0040KB-A	N version
R5F213M7QNNP	48 Kbytes	1 Kbyte × 4	4 Kbytes		
R5F213M8QNNP	64 Kbytes	1 Kbyte × 4	6 Kbytes		
R5F213MAQNNP	96 Kbytes	1 Kbyte × 4	7 Kbytes		
R5F213MCQNNP	112 Kbytes	1 Kbyte × 4	7.5 Kbytes		

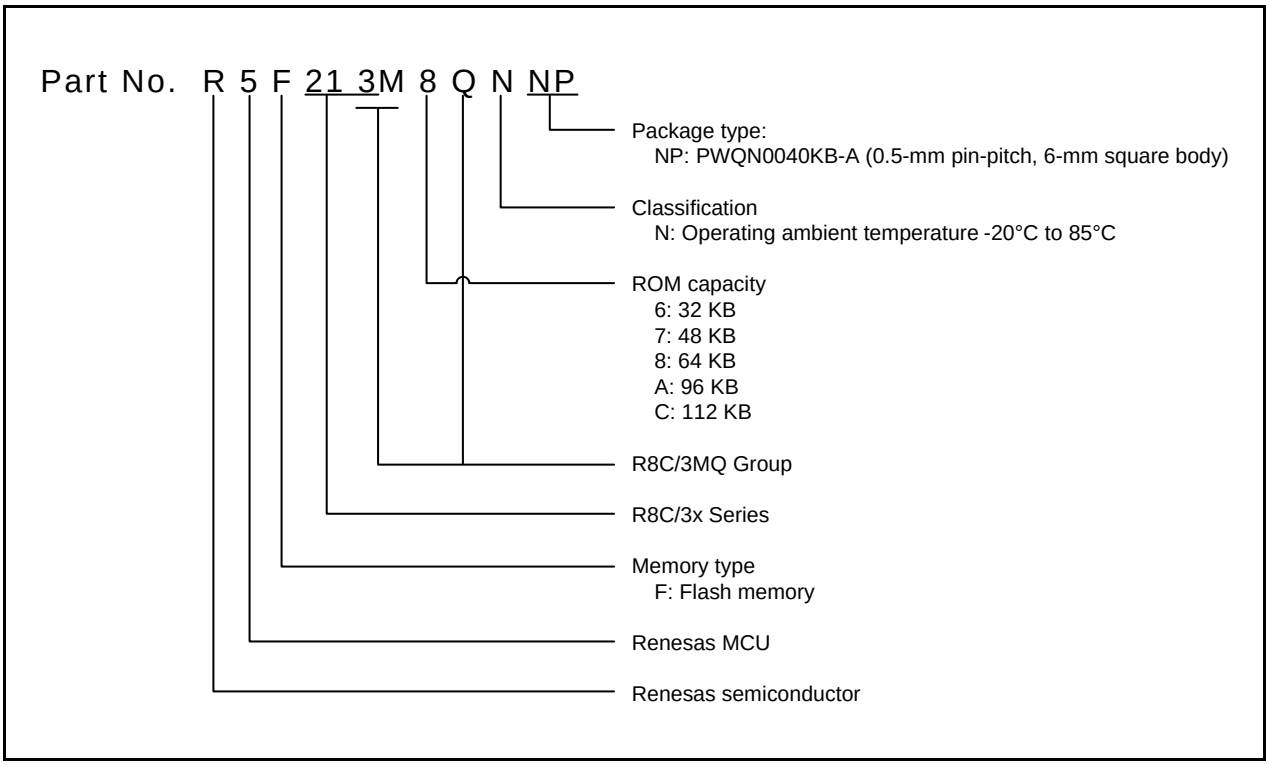


Figure 1.1 Part Number, Memory Size, and Package of R8C/3MQ Group

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

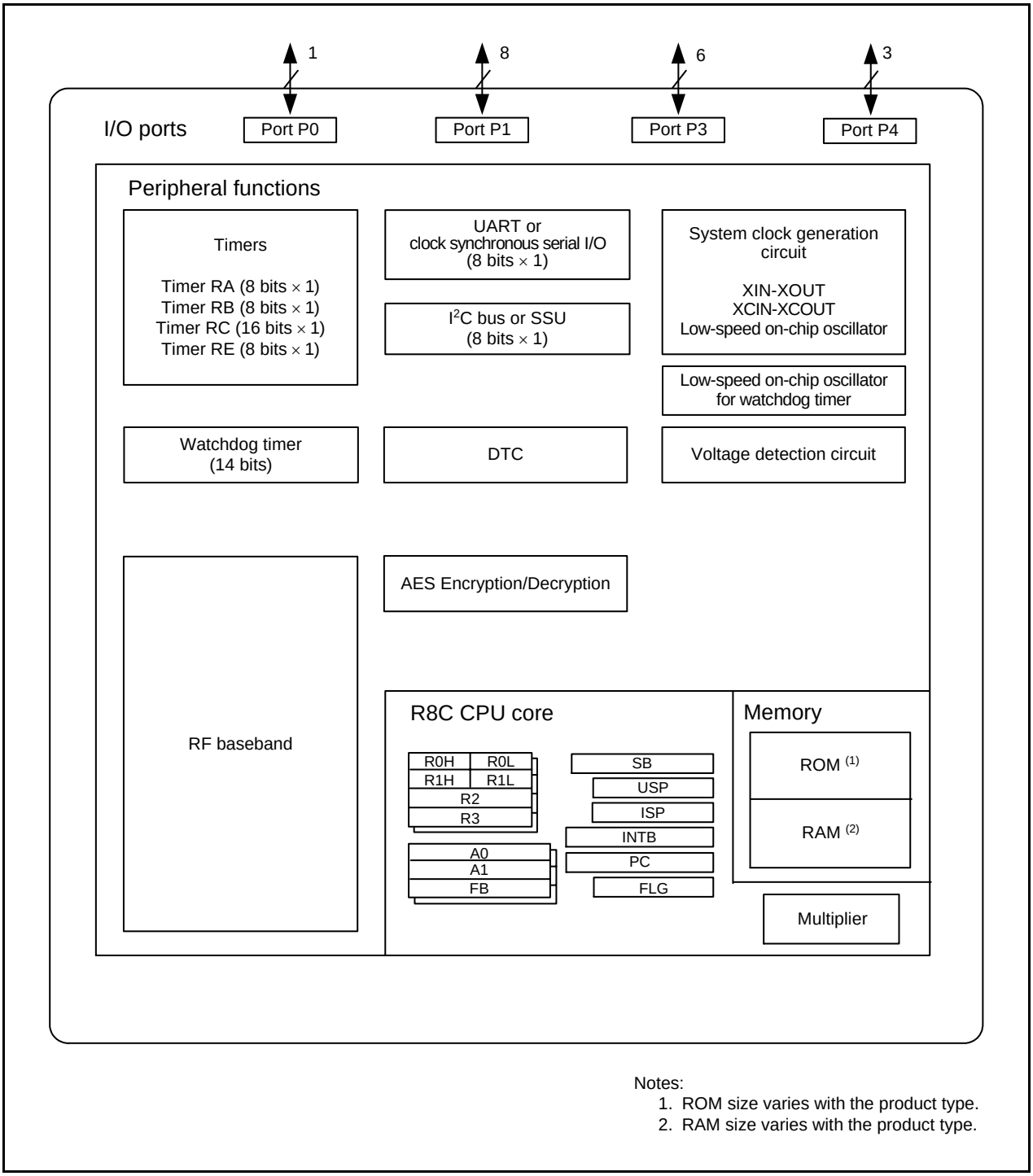
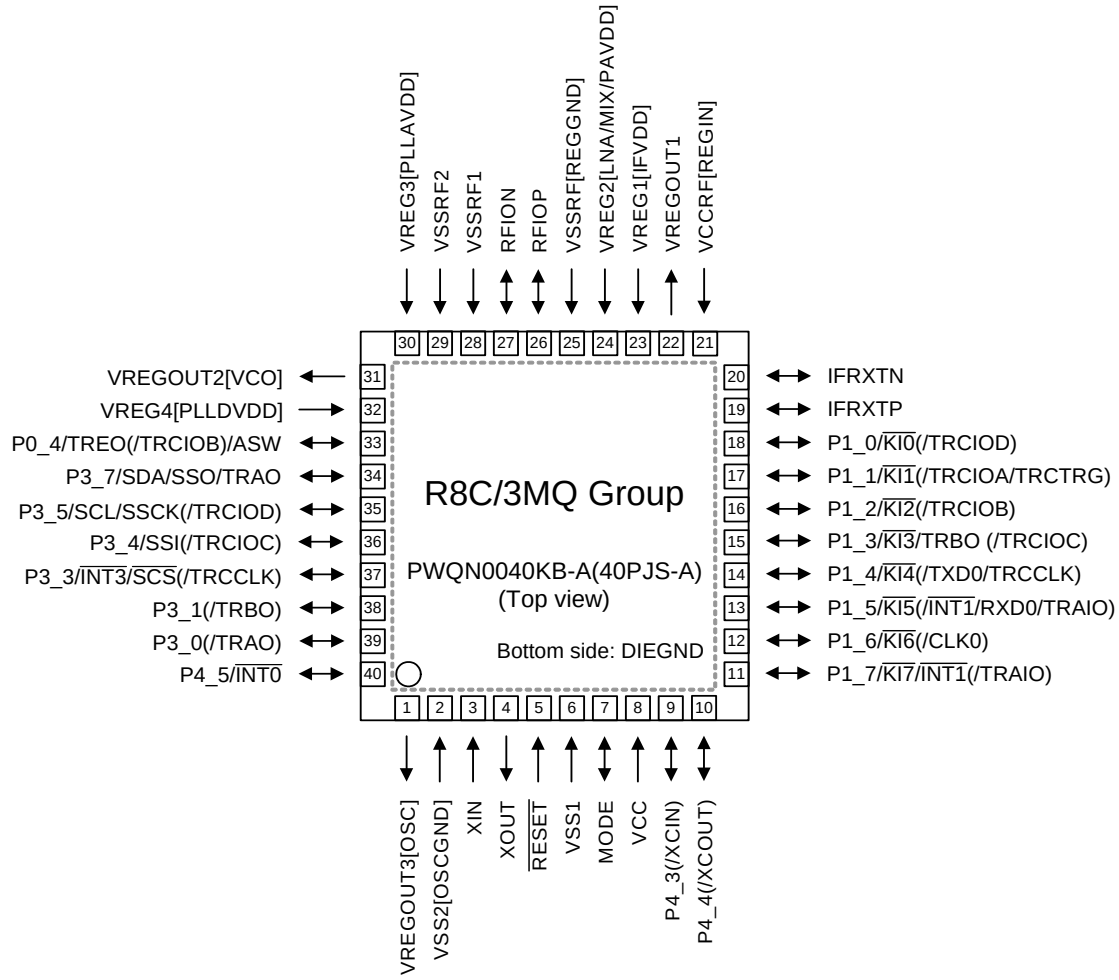


Figure 1.2 Block Diagram

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.5 outlines Pin Name Information by Pin Number.



Notes:
1. The function in parentheses can be assigned to the pin by a program.
2. [ ] indicates the internal function name related to the pin.
3. Confirm the pin 1 position on the package by referring to the package dimensions.
4. Connect the metal pad (DIEGND) of the package's bottom side to the board's GND side.

Figure 1.3 Pin Assignment (Top View)

Table 1.5 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I^2C bus	RF Pin Other
1	VREGOUT3							
2	VSS2							
3	XIN							
4	XOUT							
5	$\overline{\text{RESET}}$							
6	VSS1							
7	MODE							
8	VCC							
9	(XCIN)	P4_3						
10	(XCOUT)	P4_4						
11		P1_7	$\overline{\text{KI7}}$/$\overline{\text{INT1}}$	(TRAIO)				
12		P1_6	$\overline{\text{KI6}}$		(CLK0)			
13		P1_5	$\overline{\text{KI5}}$(/$\overline{\text{INT1}}$)	(TRAIO)	(RXD0)			
14		P1_4	$\overline{\text{KI4}}$	(TRCCLK)	(TXD0)			
15		P1_3	$\overline{\text{KI3}}$	TRBO(/TRCIOC)				
16		P1_2	$\overline{\text{KI2}}$	(TRCIOB)				
17		P1_1	$\overline{\text{KI1}}$	(TRCIOA/TRCTRG)				
18		P1_0	$\overline{\text{KI0}}$	(TRCIOD)				
19								IFRXTP
20								IFRXTN
21	VCCRF							
22	VREGOUT1							
23	VREG1							
24	VREG2							
25	VSSRF							
26								RFIOP
27								RFION
28	VSSRF1							
29	VSSRF2							
30	VREG3							
31	VREGOUT2							
32	VREG4							
33		P0_4		TREO(/TRCIOB)				ASW
34		P3_7		TRAO		SSO	SDA	
35		P3_5		(TRCIOD)		SSCK	SCL	
36		P3_4		(TRCIOC)		SSI		
37		P3_3	$\overline{\text{INT3}}$	(TRCCLK)		$\overline{\text{SCS}}$		
38		P3_1		(TRBO)				
39		P3_0		(TRAO)				
40		P4_5	$\overline{\text{INT0}}$					
Bottom side	DIEGND							

Note:
1. The function in parentheses can be assigned to the pin by a program.

1.5 Pin Functions

Tables 1.6 and 1.7 list Pin Functions.

Table 1.6 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS1	—	Apply 1.8 to 3.6 V to the VCC pin. Apply 0 V to the VSS1 pin.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock oscillation circuit I/O. Connect a crystal oscillator between the XIN and XOUT pins.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock oscillation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is used as an input pin for timer RB and timer RC.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Timer RE	TREO	O	Divided clock output pin.
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0	I	Serial data input pin.
	TXD0	O	Serial data output pin.
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I^2C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
I/O ports	P0_4, P1_0 to P1_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.

I: Input O: Output I/O: Input and output

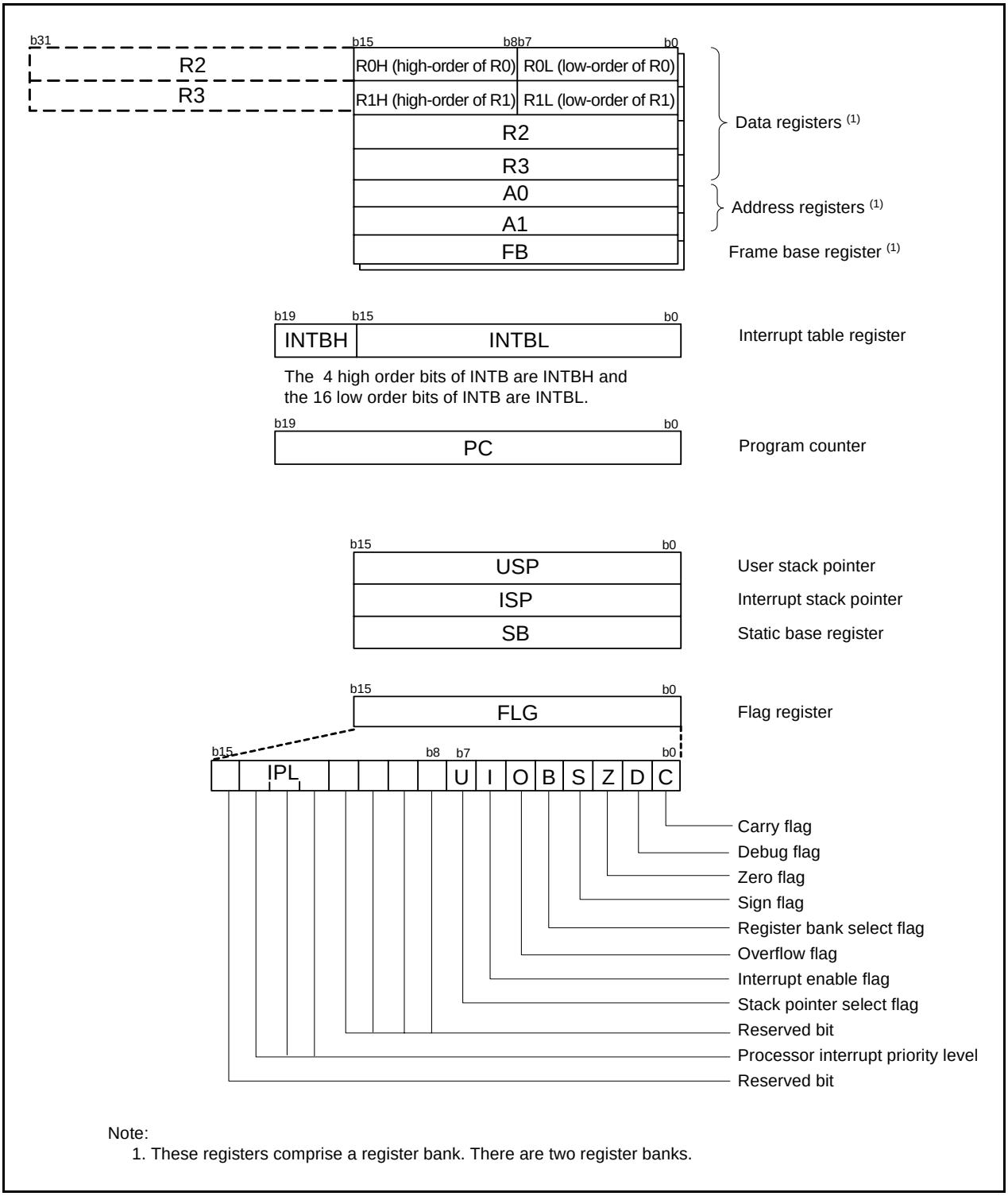
Table 1.7 Pin Functions (2)

Item	Pin Name	I/O Type	Description
Analog power supply input	VCCRF, VSSRF, VSSRF1, VSSRF2, VSS2, DIEGND	—	Apply the same voltage as the VCC of 1.8 V to 3.6 V to VCCRF. Apply 0 V to VSSRF, VSSRF1, VSSRF2, VSS2, and DIEGND.
	VREG1	—	1.5 V IF VDD pin. Connect to the VREGOUT1 pin.
	VREG2	—	1.5 V LNA/MIX/PA VDD pin. Connect to the VREGOUT1 pin.
	VREG3	—	1.5 V PLL ANALOG VDD pin. Connect to the VREGOUT1 pin.
	VREG4	—	1.5 V PLL DIGITAL VDD pin. Connect to the VREGOUT1 pin.
Regulator output	VREGOUT1	—	On-chip regulator output (1.5 V) pin for the analog circuit. Connect only a bypass capacitor between pins VREGOUT1 and VSS. Use only as the power supply for pins VREG1, VREG2, VREG3, and VREGF4.
	VREGOUT2	—	Regulator output (1.5 V) pin for the VCO circuit. Connect only a bypass capacitor between pins VREGOUT2 and VSS. Do not use as the power supply for other circuits.
	VREGOUT3	—	Regulator output (1.5 V) pin for the XIN oscillation circuit. Connect only a bypass capacitor between pins VREGOUT3 and VSS. Do not use as the power supply for other circuits.
RF I/O	RFIOP, RFION	I/O	RF I/O pins
Test pins	IFRXTN, IFRXTP	I/O	Ports for testing. Leave open or apply 0 V.
External antenna switch control output	ASW	O	Signal output pin to control the external antenna switch. If antenna switch control is not required, leave open.

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



Note:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

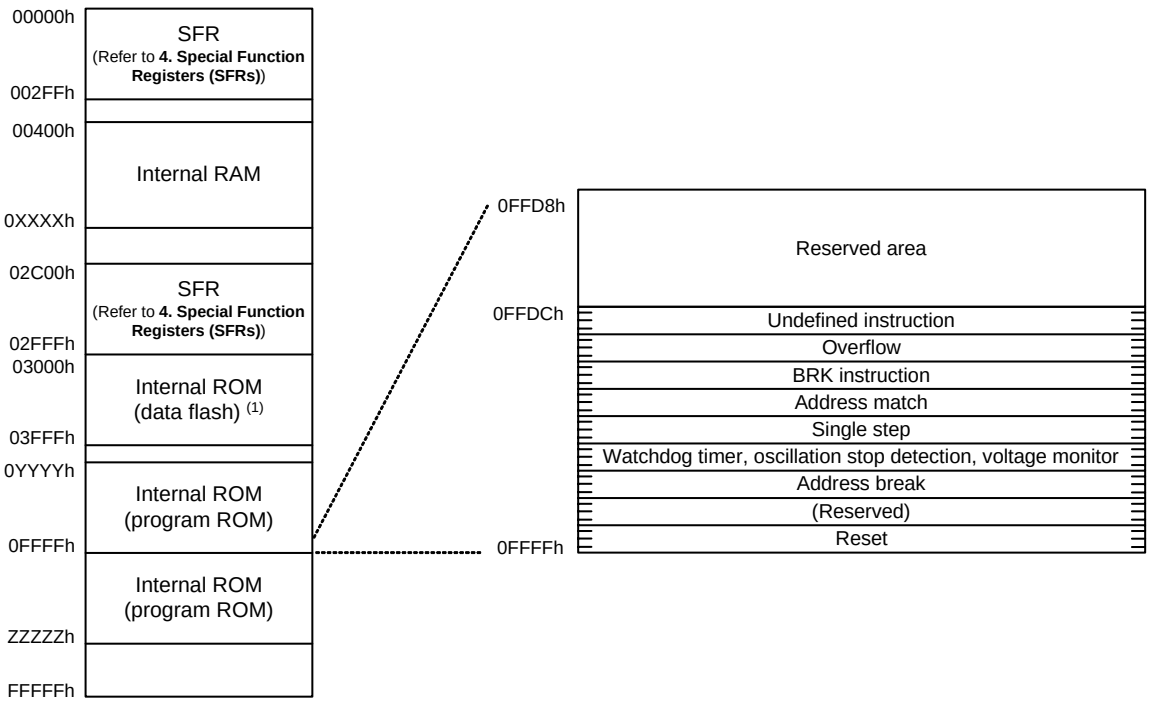
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/3MQ Group

Figure 3.1 is a Memory Map of R8C/3MQ Group. The R8C/3MQ Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. However, for products with internal ROM (program ROM) capacity of 64 Kbytes or more, the internal ROM is also allocated higher addresses, beginning with address 0FFFFh.
For example, a 32-Kbyte internal ROM area is allocated addresses 08000h to 0FFFFh, and a 96-Kbyte internal ROM is allocated addresses 04000h to 1BFFFh.
The fixed interrupt vector table is allocated addresses 08000h to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. The data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. The blank areas are reserved and cannot be accessed by users. Do not use the data flash as a program area.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F213M6QNNP	32 Kbytes	08000h	–	2.5 Kbytes	00DFFh
R5F213M7QNNP	48 Kbytes	04000h	–	4 Kbytes	013FFh
R5F213M8QNNP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F213MAQNNP	96 Kbytes	04000h	1BFFFh	7 Kbytes	01FFFh
R5F213MCQNNP	112 Kbytes	04000h	1FFFFh	7.5 Kbytes	021FFh

Figure 3.1 Memory Map of R8C/3MQ Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.11 list the special function registers. Table 4.12 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (0000h to 002Fh) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00101000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) (0030h to 006Fh) (1)

Address	Register	Symbol	After Reset
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h			
0034h	Voltage detection Register 2	VCA2	00h (3) 00100000b (4)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (3) 1100X011b (4)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b
003Ah	WDT Detection Flag	VW2C	10000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h	BB Timer Compare 2 Interrupt Control Register	BBTIM2IC	XXXXX000b
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh			
004Fh	SSU Interrupt Control Register/IIC bus Interrupt Control Register (2)	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h	Bank 0 Reception Complete/IDLE Interrupt Control Register (5)	BBRX0IC/BBIDELIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch	BB Timer Compare 1 Interrupt Control Register	BBTIM1IC	XX00X000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	CCA Complete Interrupt Control Register	BBCCAIC	XXXXX000b
005Fh	BB Timer Compare 0 Interrupt Control Register	BBTIM0IC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch	Address Filter Interrupt Control Register	BBADFIC	XXXXX000b
006Dh	Transmit Overrun Interrupt Control Register	BBTXORIC	XXXXX000b
006Eh	Transmission Complete Interrupt Control Register	BBTXIC	XX00XX00b
006Fh	Receive Overrun 1 Interrupt Control Register	BBRXOR1IC	XXXXX000b

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.
3. The LVDAS bit in the OFS register is set to 1.
4. The LVDAS bit in the OFS register is set to 0.
5. Can be selected by the BANK0INTSEL bit in the BBTXRXMODE4 register.

Table 4.3 SFR Information (3) (0070h to 00AFh) (1)

Address	Register	Symbol	After Reset
0070h	PLL Lock Detection Interrupt Control Register	BBPLLIC	XXXXX000b
0071h	Receive Overrun 0/Calibration Complete Interrupt Control Register (3)	BBRXOR0IC/BBCALIC	XXXXX000b
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Bank 1 Reception Complete/Clock Regulator Interrupt Control Register (2)	BBRX1IC/BBCREGIC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Can be selected by the BANK1INTSEL bit in the BBTXRXMODE4 register.
3. Can be selected by the ROR0INTSEL bit in the BBTXRXMODE4 register.

Table 4.4 SFR Information (4) (00B0h to 011Fh) (1)

Address	Register	Symbol	After Reset
00B0h			
:			
00DFh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	XXh
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h			
0107h			
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (0120h to 019Fh) (1)

Address	Register	Symbol	After Reset
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			
:			
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah			
018Bh			
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR / ICMR	00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2 / SAR	00h
019Eh			
019Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.6 SFR Information (6) (01A0h to 02FFh) (1)

Address	Register	Symbol	After Reset
01A0h			
:			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
:			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h			
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KI1EN	00h
0200h			
:			
02FFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (2C00h to 2C6Fh) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) (2C70h to 2CAFh) (1)

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (2CB0h to 2CEFh) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (2CF0h to 2D2Fh) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h	Baseband Control Register	BBCON	00h
2D01h	Transmit/Receive Reset Register	BBTXRXRST	00h
2D02h	Transmit/Receive Mode Register 0	BBTXRXMODE0	00h
2D03h	Transmit/Receive Mode Register 1	BBTXRXMODE1	00h
2D04h	Receive Frame Length Register	BBRXFLEN	00h
2D05h	Receive Data Counter Register	BBRXCOUNT	00h
2D06h	RSSI/CCA Result Register	BBRSSICCARSLT	00h
2D07h	Transmit/Receive Status Register 0	BBTXRXST0	80h
2D08h	Transmit Frame Length Register	BBTXFLEN	00h
2D09h	Transmit/Receive Mode Register 2	BBTXRXMODE2	30h
2D0Ah	Transmit/Receive Mode Register 3	BBTXRXMODE3	00h
2D0Bh	Receive Level Threshold Set Register	BBLVLVTH	80h
2D0Ch	Transmit/Receive Control Register	BBTXRXCON	00h
2D0Dh	CSMA Control Register 0	BBCSMACON0	00h
2D0Eh	CCA Level Threshold Set Register	BBCCAVTH	80h
2D0Fh	Transmit/Receive Status Register 1	BBTXRXST1	00h
2D10h	RF Control Register	BBRFCON	00h
2D11h	Transmit/Receive Mode Register 4	BBTXRXMODE4	00h
2D12h	CSMA Control Register 1	BBCSMACON1	9Ch
2D13h	CSMA Control Register 2	BBCSMACON2	05h
2D14h	PAN Identifier Register	BBPANID	00h
2D15h			00h
2D16h	Short Address Register	BBSHORTAD	00h
2D17h			00h
2D18h	Extended Address Register	BBEXTENDAD0	00h
2D19h			00h
2D1Ah		BBEXTENDAD1	00h
2D1Bh			00h
2D1Ch		BBEXTENDAD2	00h
2D1Dh			00h
2D1Eh		BBEXTENDAD3	00h
2D1Fh			00h
2D20h	Timer Read-Out Register 0	BBTIMEREAD0	00h
2D21h			00h
2D22h	Timer Read-Out Register 1	BBTIMEREAD1	00h
2D23h			00h
2D24h	Timer Compare 0 Register 0	BBCOMP0REG0	00h
2D25h			00h
2D26h	Timer Compare 0 Register 1	BBCOMP0REG1	00h
2D27h			00h
2D28h	Timer Compare 1 Register 0	BBCOMP1REG0	00h
2D29h			00h
2D2Ah	Timer Compare 1 Register 1	BBCOMP1REG1	00h
2D2Bh			00h
2D2Ch	Timer Compare 2 Register 0	BBCOMP2REG0	00h
2D2Dh			00h
2D2Eh	Timer Compare 2 Register 1	BBCOMP2REG1	00h
2D2Fh			00h

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (2D30h to 2FFFh) (1)

Address	Register	Symbol	After Reset
2D30h	Time Stamp Register 0	BBTSTAMP0	00h
2D31h			00h
2D32h	Time Stamp Register 1	BBTSTAMP1	00h
2D33h			00h
2D34h	Timer Control Register	BBTIMECON	00h
2D35h	Backoff Period Register	BBBOFFPROD	00h
2D36h			
2D37h			
2D38h			
2D39h			
2D3Ah	PLL Division Register 0	BBPLLDIVL	65h
2D3Bh	PLL Division Register 1	BBPLLDIVH	09h
2D3Ch	Transmit Output Power Register	BBTXOUTPWR	00h
2D3Dh	RSSI Offset Register	BBRSSIOFS	F6h
2D3Eh			
2D3Fh			
2D40h			
:			
2D45h			
2D46h	Automatic ACK Response Timing Adjustment Register	BBACKRTNTIMG	22h
2D47h			
:			
2D63h			
2D64h			
2D65h			
2D66h			
2D67h			
2D68h	Verification Mode Set Register	BBEVAREG	00h
2D69h			
2D6Ah			
2D6Bh			
2D6Ch			
2D6Dh			
2D6Eh			
2D6Fh			
2D70h			
2D71h			
2D72h			
2D73h			
2D74h			
2D75h			
2D76h	IDLE Wait Set Register	BBIDELWAIT	01h
2D77h			
2D78h			
2D79h			
2D7Ah	ANTSW Output Timing Set Register	BBANTSWTIMG	72h
2D7Bh			
2D7Ch	RF Initial Set Register	BBRFINI	XXh
2D7Dh			XXh
2D7Eh			
2D7Fh			
2D80h			
2D81h			
2D82h	ANTSW Control Register	BBANTSWCON	00h
2D83h			
:			
2DFFh			
2E00h	Transmit RAM	TRANSMIT_RAM_START	
:	Transmit RAM		
2E7Eh	Transmit RAM	TRANSMIT_RAM_END	
2E7Fh			
2D80h	Receive RAM	RECIEVE_RAM_START	
:	Receive RAM		
2EFEh	Receive RAM	RECIEVE_RAM_END	
2EFFh			
2F00h			
:			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
   At shipment, the option function select area is set to FFh. It is set to the written value after written by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
   At shipment, the ID code areas are set to FFh. They are set to the written value after written by the user.

5. Resets

The following resets are implemented: hardware reset, power-on reset, voltage monitor 0 reset, watchdog timer reset, and software reset.
Table 5.1 lists the Reset Names and Sources, Figure 5.1 shows a Block Diagram of Reset Circuit.

Table 5.1 Reset Names and Sources

Reset Name	Source
Hardware reset	Input voltage of $\overline{\text{RESET}}$ pin is held “L”
Power-on reset	VCC rises
Voltage monitor 0 reset	VCC falls (monitor voltage: Vdet0)
Watchdog timer reset	Underflow of watchdog timer
Software reset	Write 1 to PM03 bit in PM0 register

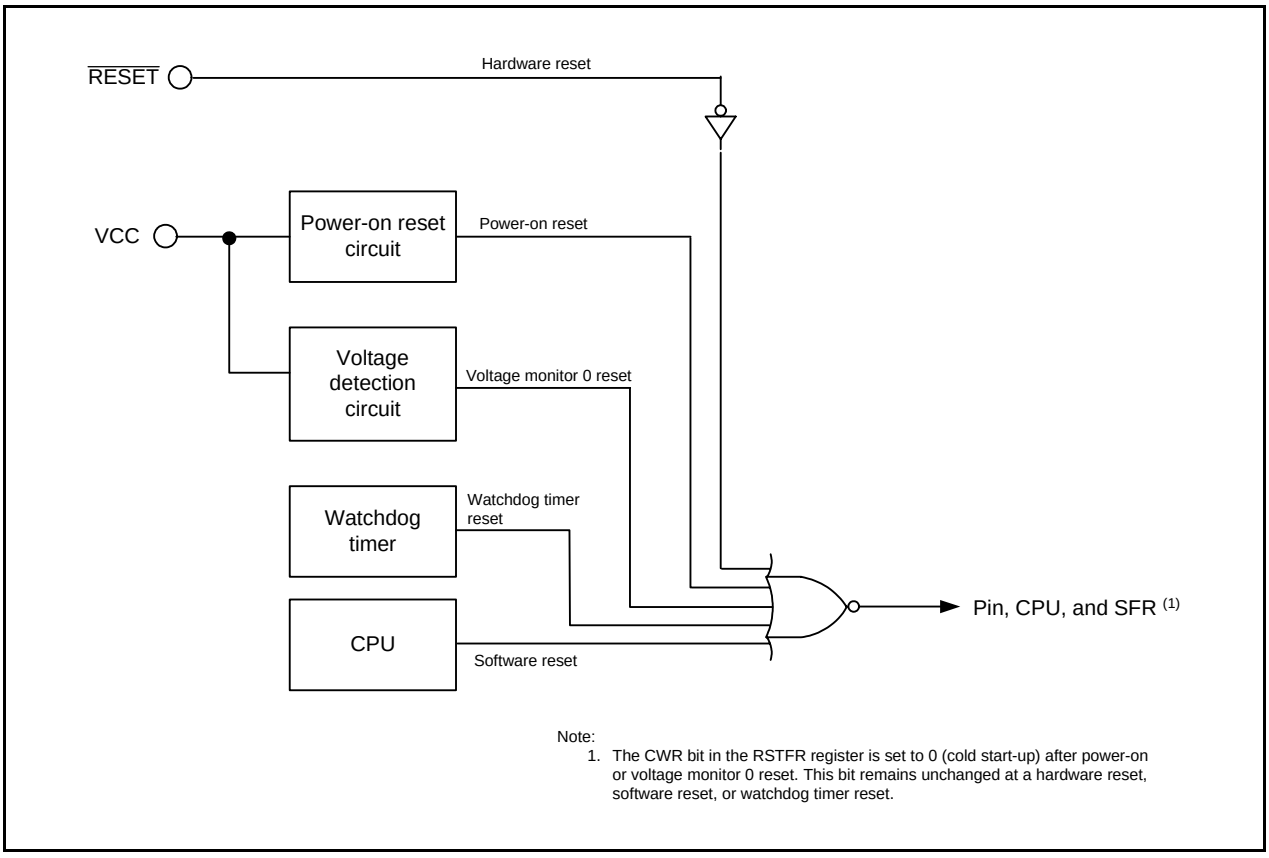


Figure 5.1 Block Diagram of Reset Circuit

Table 5.2 lists the Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”, Figure 5.2 shows the CPU Register Status after Reset, Figure 5.3 shows the Reset Sequence.

Table 5.2 Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”

Pin Name	Pin Function
P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Input port

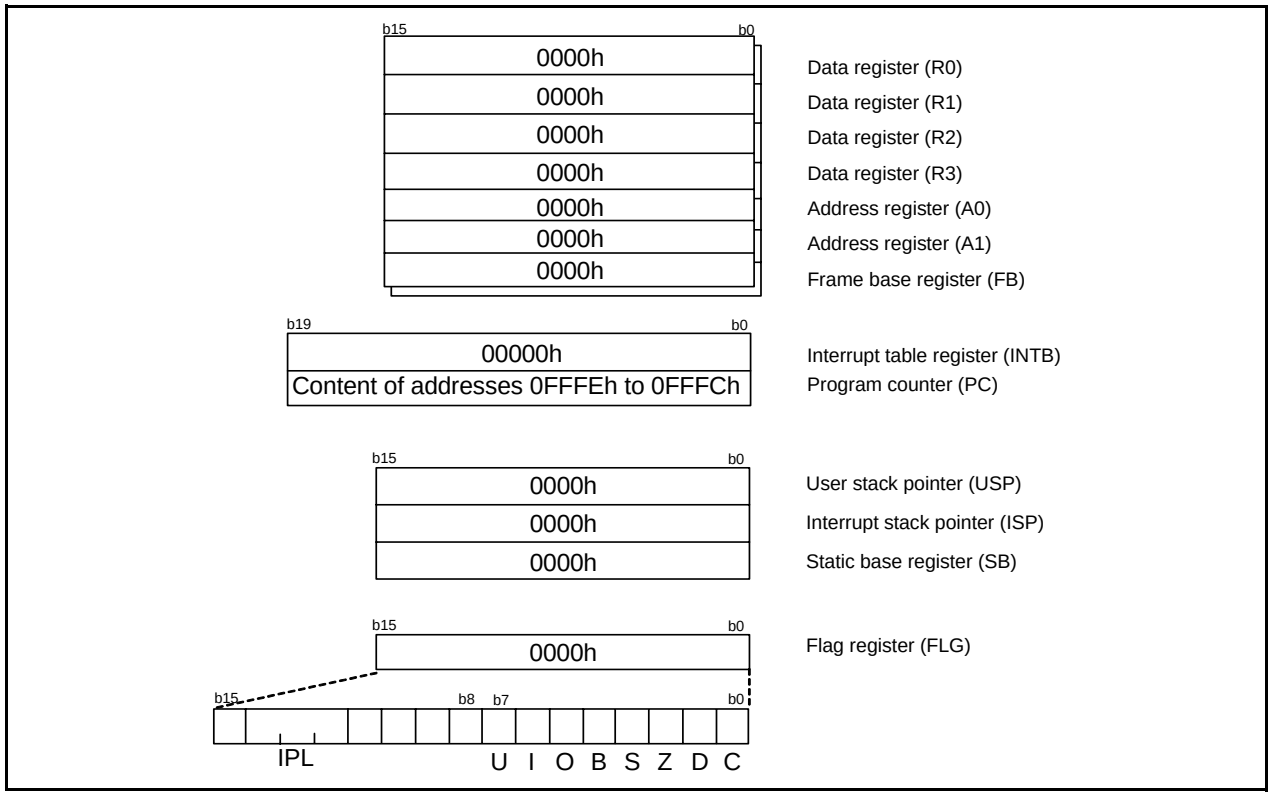


Figure 5.2 CPU Register Status after Reset

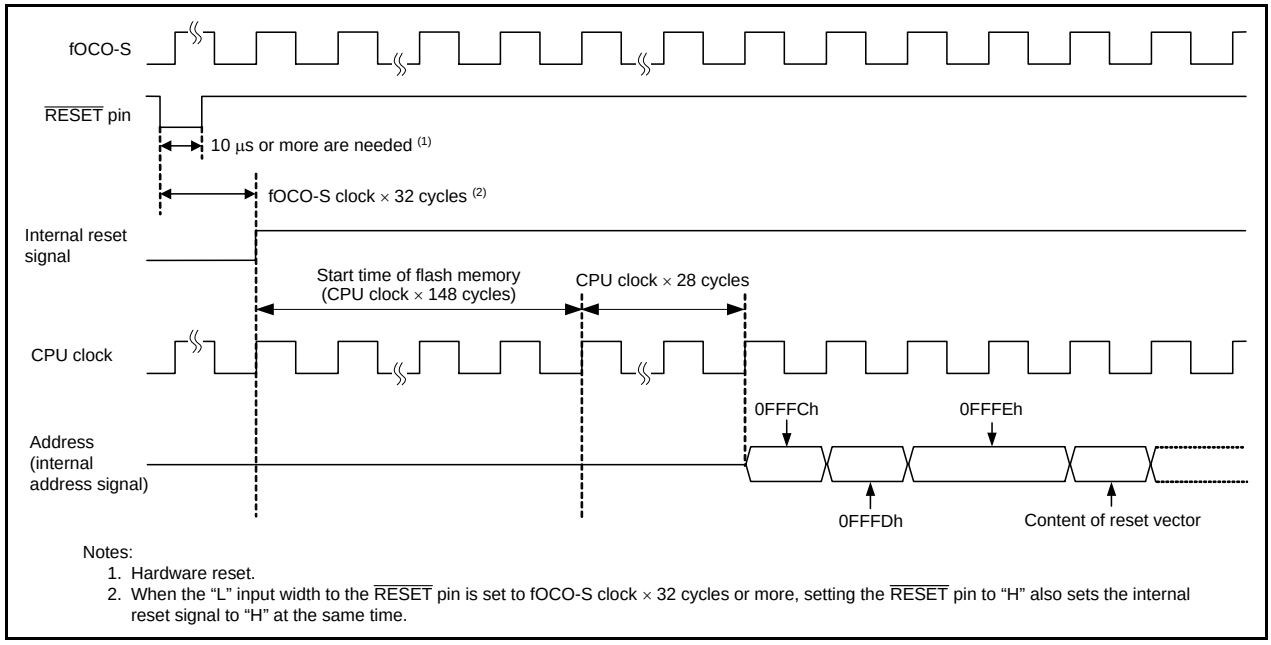


Figure 5.3 Reset Sequence

5.1 Registers

5.1.1 Processor Mode Register 0 (PM0)

Address 0004h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PM03	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	PM03	Software reset bit	The MCU is reset when this bit is set to 1. When read, the content is 0.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM0 register.

5.1.2 Reset Source Determination Register (RSTFR)

Address 000Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	WDR	SWR	HWR	CWR	
After Reset	0	X	X	X	X	X	X	X	(Note 1)

Bit	Symbol	Bit Name	Function	R/W
b0	CWR	Cold start-up/warm start-up determine flag (2, 3)	0: Cold start-up 1: Warm start-up	R/W
b1	HWR	Hardware reset detect flag	0: Not detected 1: Detected	R
b2	SWR	Software reset detect flag	0: Not detected 1: Detected	R
b3	WDR	Watchdog timer reset detect flag	0: Not detected 1: Detected	R
b4	—	Reserved bits	When read, the content is undefined.	R
b5	—			
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Notes:
1. The CWR bit is set to 0 (cold start-up) after power-on or voltage monitor 0 reset. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
2. If 1 is written to the CWR bit by a program, it is set to 1. (Writing 0 does not affect this bit.)
3. When the VW0C0 bit in the VW0C register is set to 0 (voltage monitor 0 reset disabled), the CWR bit value is undefined.

5.1.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: Do not set. 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   Initial value of OFS register is FFh. The value of OFS register changes as programmed by user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

5.1.4 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Settng Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   At shipment, the OFS2 register is set to FFh. It is set to the written value after written by the user.

   For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

5.2 Hardware Reset

A reset is applied using the $\overline{\text{RESET}}$ pin. When an “L” signal is applied to the $\overline{\text{RESET}}$ pin while the supply voltage meets the recommended operating conditions, pins, CPU, and SFRs are all reset (refer to **Table 5.2 Pin Functions while $\overline{\text{RESET}}$ Pin Level is “L”**, **Figure 5.2 CPU Register Status after Reset**, and **Table 4.1 to Table 4.11 SFR Information**).

When the input level applied to the $\overline{\text{RESET}}$ pin changes from “L” to “H”, a program is executed beginning with the address indicated by the reset vector. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.

Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after reset.

The internal RAM is not reset. If the $\overline{\text{RESET}}$ pin is pulled “L” while writing to the internal RAM is in progress, the contents of internal RAM will be undefined.

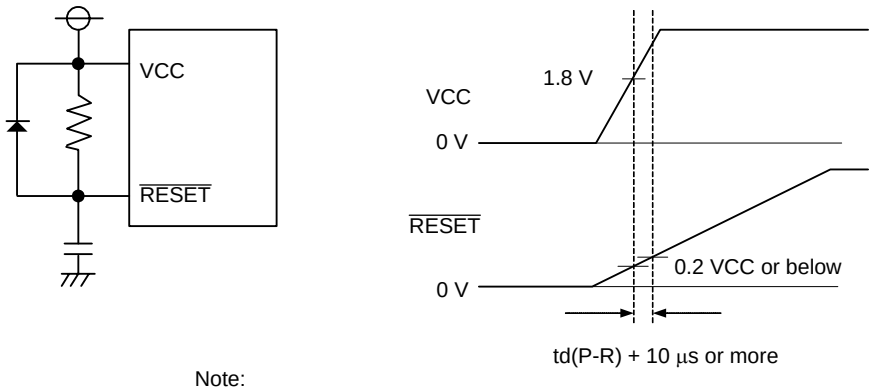
Figure 5.4 shows an Example of Hardware Reset Circuit and Operation and Figure 5.5 shows an Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation.

5.2.1 When Power Supply is Stable

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Wait for 10 µs.
(3) Apply “H” to the $\overline{\text{RESET}}$ pin.

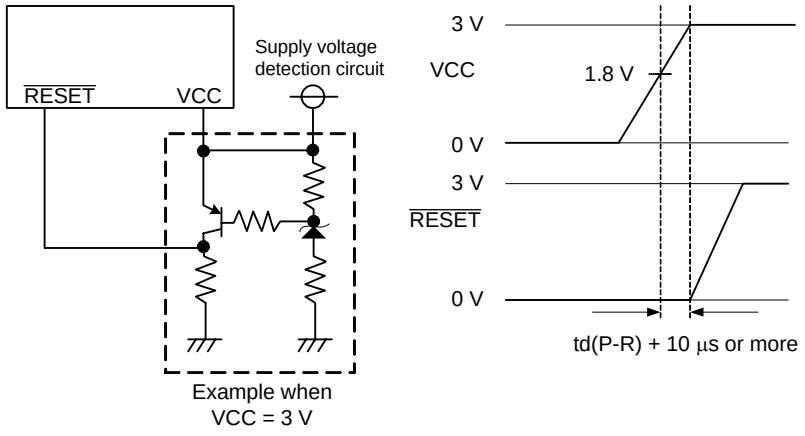
5.2.2 Power On

(1) Apply “L” to the $\overline{\text{RESET}}$ pin.
(2) Let the supply voltage increase until it meets the recommended operating conditions.
(3) Wait for td(P-R) or more to allow the internal power supply to stabilize (refer to **28. Electrical Characteristics**).
(4) Wait for 10 µs.
(5) Apply “H” to the $\overline{\text{RESET}}$ pin.



Note:
1. Refer to **28. Electrical Characteristics**.

Figure 5.4 Example of Hardware Reset Circuit and Operation

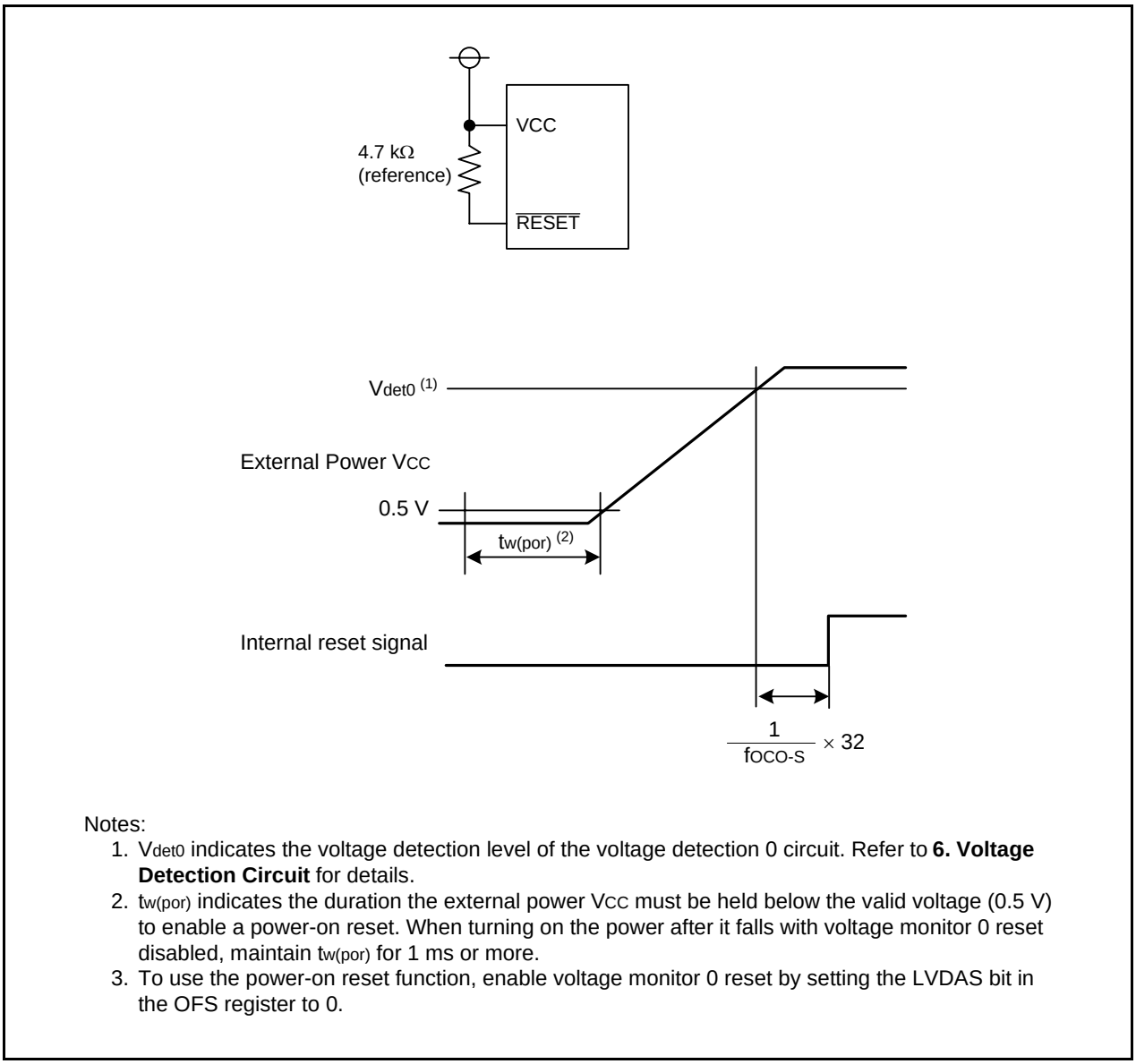


Note:
1. Refer to **28. Electrical Characteristics**.

Figure 5.5 Example of Hardware Reset Circuit (Usage Example of External Supply Voltage Detection Circuit) and Operation

5.3 Power-On Reset Function

When the $\overline{\text{RESET}}$ pin is connected to the VCC pin via a pull-up resistor, and the VCC pin voltage level rises, the power-on reset function is enabled and the MCU resets its pins, CPU, and SFRs. When a capacitor is connected to the $\overline{\text{RESET}}$ pin, too, always keep the voltage to the $\overline{\text{RESET}}$ pin 0.8 VCC or more.
When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held "H" and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after power-on reset.
To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.
Figure 5.6 shows an Example of Power-On Reset Circuit and Operation.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.
3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.6 Example of Power-On Reset Circuit and Operation

5.4 Voltage Monitor 0 Reset

A reset is applied using the on-chip voltage detection 0 circuit. The voltage detection 0 circuit monitors the input voltage to the VCC pin. The voltage to monitor is Vdet0. To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset). The Vdet0 voltage detection level can be changed by the settings of bits VDSEL0 to VDSEL1 in the OFS register.

When the input voltage to the VCC pin reaches the Vdet0 level or below, the pins, CPU, and SFRs are reset.

When the input voltage to the VCC pin reaches the Vdet0 level or above, the low-speed on-chip oscillator clock starts counting. When the low-speed on-chip oscillator clock count reaches 32, the internal reset signal is held “H” and the MCU enters the reset sequence (refer to **Figure 5.3**). The low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock after reset.

To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Bits VDSEL0 to VDSEL1 and LVDAS cannot be changed by a program. To set these bits, write values to b4 to b6 of address 0FFFFh using a flash programmer.

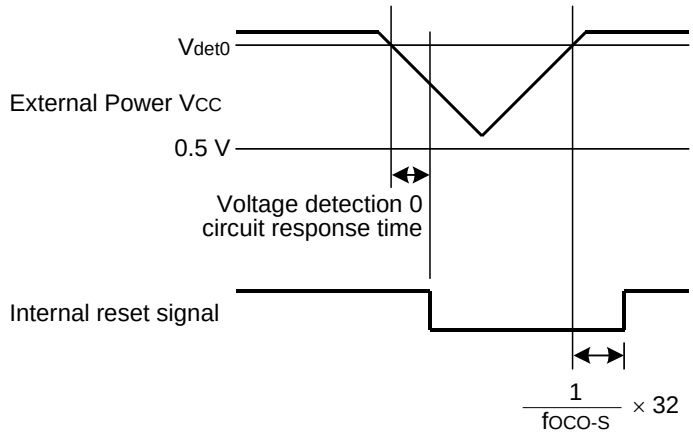
Refer to **5.1.3 Option Function Select Register (OFS)** for details of the OFS register.

Refer to **4. Special Function Registers (SFRs)** for the status of the SFRs after voltage monitor 0 reset.

The internal RAM is not reset. When the input voltage to the VCC pin reaches the Vdet0 level or below while writing to the internal RAM is in progress, the contents of internal RAM are undefined.

Refer to **6. Voltage Detection Circuit** for details of voltage monitor 0 reset.

Figure 5.7 shows an Operating Example of Voltage Monitor 0 Reset.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

Figure 5.7 Operating Example of Voltage Monitor 0 Reset

5.5 Watchdog Timer Reset

When the PM12 bit in the PM1 register is set to 1 (reset when watchdog timer underflows), the MCU resets its pins, CPU, and SFRs if the watchdog timer underflows. Then the program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock with no division is automatically selected as the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after watchdog timer reset.
The internal RAM is not reset. When the watchdog timer underflows while writing to the internal RAM is in progress, the contents of internal RAM are undefined.
The underflow period and refresh acknowledge period for the watchdog timer can be set by bits WDTUFS0 to WDTUFS1 and bits WDTRCS0 to WDTRCS1 in the OFS2 register, respectively.
Refer to **14. Watchdog Timer** for details of the watchdog timer.

5.6 Software Reset

When the PM03 bit in the PM0 register is set to 1 (MCU reset), the MCU resets its pins, CPU, and SFRs. The program beginning with the address indicated by the reset vector is executed. After reset, the low-speed on-chip oscillator clock with no division is automatically selected for the CPU clock.
Refer to **4. Special Function Registers (SFRs)** for the states of the SFRs after software reset.
The internal RAM is not reset.

5.7 Cold Start-Up/Warm Start-Up Determination Function

The cold start-up/warm start-up determination function uses the CWR bit in the RSTFR register to determine cold start-up (reset process) at power-on and warm start-up (reset process) when a reset occurred during operation.
The CWR bit is set to 0 (cold start-up) at power-on and also set to 0 at a voltage monitor 0 reset. If 1 is written to the CWR bit by a program, it is set to 1. This bit remains unchanged at a hardware reset, software reset, or watchdog timer reset.
The cold start-up/warm start-up determination function uses voltage monitor 0 reset.
Figure 5.8 shows an Operating Example of Cold Start-Up/Warm Start-Up Function

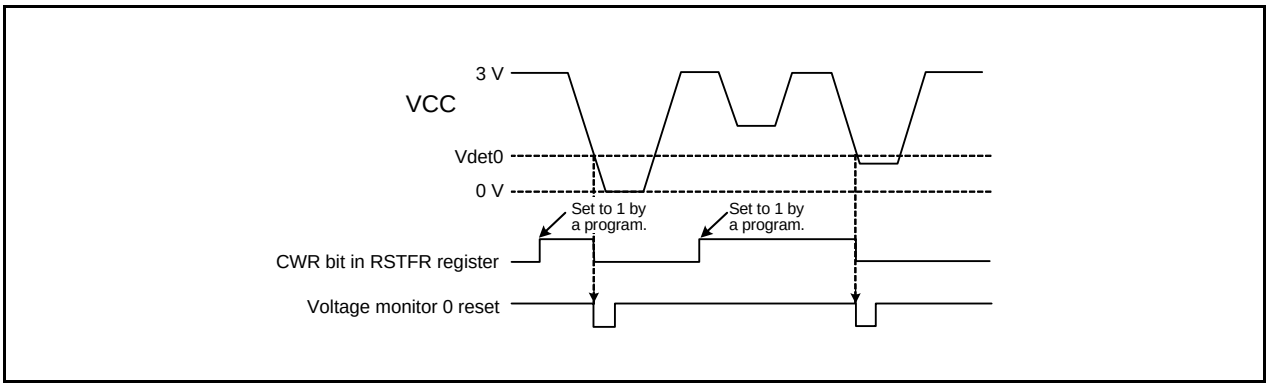


Figure 5.8 Operating Example of Cold Start-Up/Warm Start-Up Function

5.8 Reset Source Determination Function

The RSTFR register can be used to detect whether a hardware reset, software reset, or watchdog timer reset has occurred.
If a hardware reset occurs, the HWR bit is set to 1 (detected). If a software reset occurs, the SWR bit is set to 1 (detected). If a watchdog timer reset occurs, the WDR bit is set to 1 (detected).

6. Voltage Detection Circuit

The voltage detection circuit monitors the voltage input to the VCC pin. This circuit can be used to monitor the VCC input voltage by a program.

6.1 Overview

The detection voltage of voltage detection 0 can be selected among three levels using the OFS register.
The detection voltage of voltage detection 1 can be selected among two levels using the VD1LS register.
The voltage monitor 0 reset, and voltage monitor 1 interrupt can also be used.

Table 6.1 Voltage Detection Circuit Specifications

Item		Voltage Monitor 0	Voltage Monitor 1
VCC monitor	Voltage to monitor	Vdet0	Vdet1
	Detection target	Whether passing through Vdet0 by rising or falling	Whether passing through Vdet1 by rising or falling
	Detection voltage	Selectable among 3 levels using the OFS register.	Selectable among 2 levels using the VD1LS register.
	Monitor	None	The VW1C3 bit in the VW1C register
			Whether VCC is higher or lower than Vdet1
Process at voltage detection	Reset	Voltage monitor 0 reset	None
		Reset at Vdet0 > VCC; CPU operation restarts at VCC > Vdet0	
	Interrupts	None	Voltage monitor 1 interrupt
			Non-maskable or maskable selectable
			Interrupt request at: Vdet1 > VCC and/or VCC > Vdet1
Digital filter	Switching enable/ disable	No digital filter function	Supported
	Sampling time	—	(fOCO-S divided by n) × 2 n: 1, 2, 4, and 8

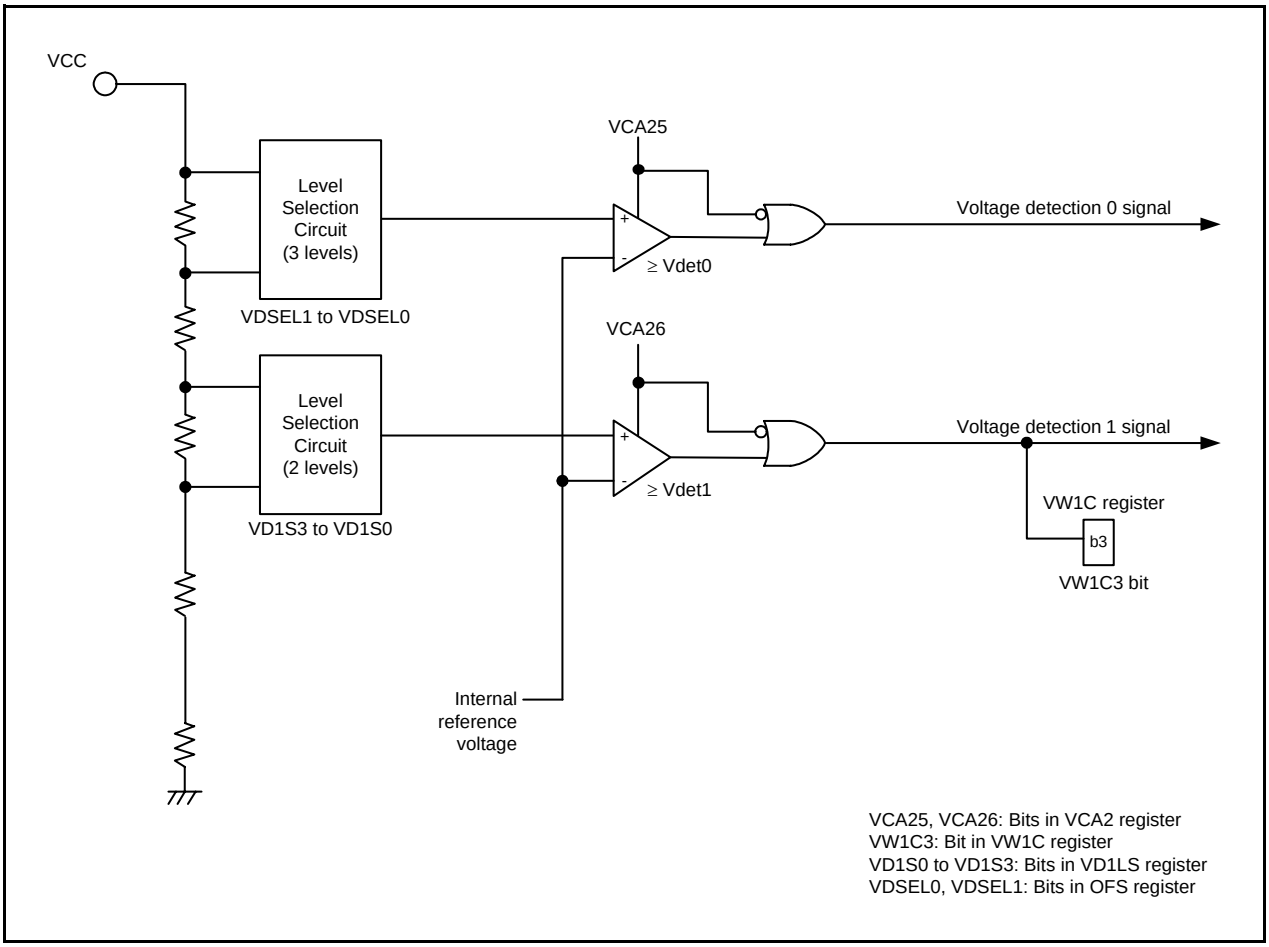


Figure 6.1 Voltage Detection Circuit Block Diagram

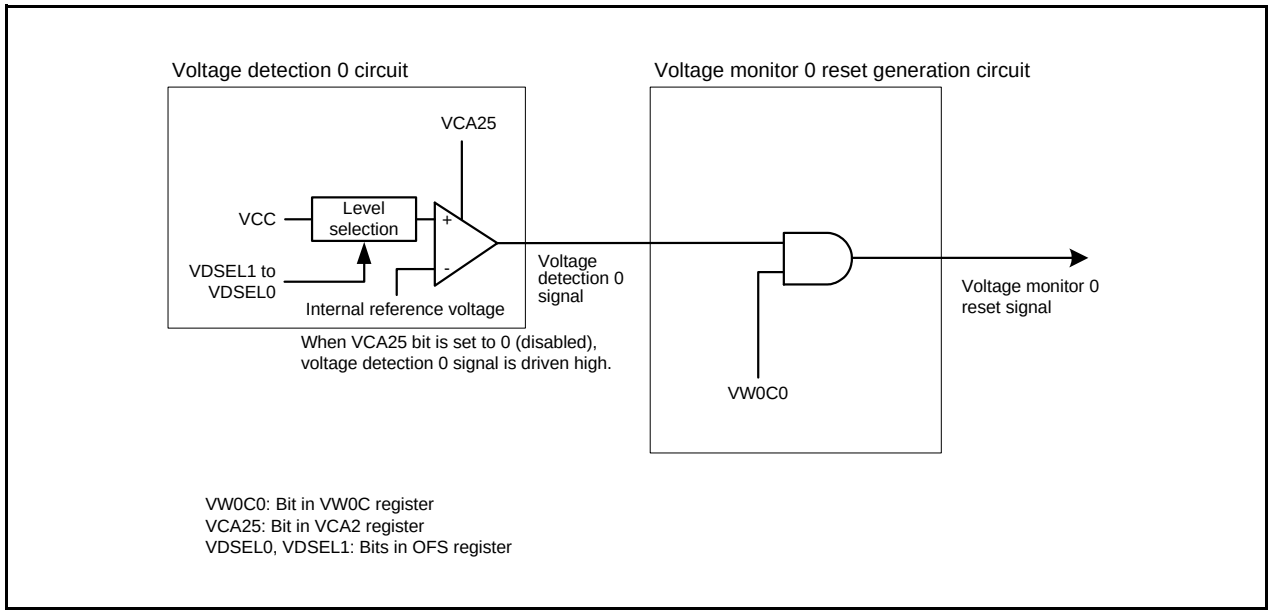


Figure 6.2 Block Diagram of Voltage Monitor 0 Reset Generation Circuit

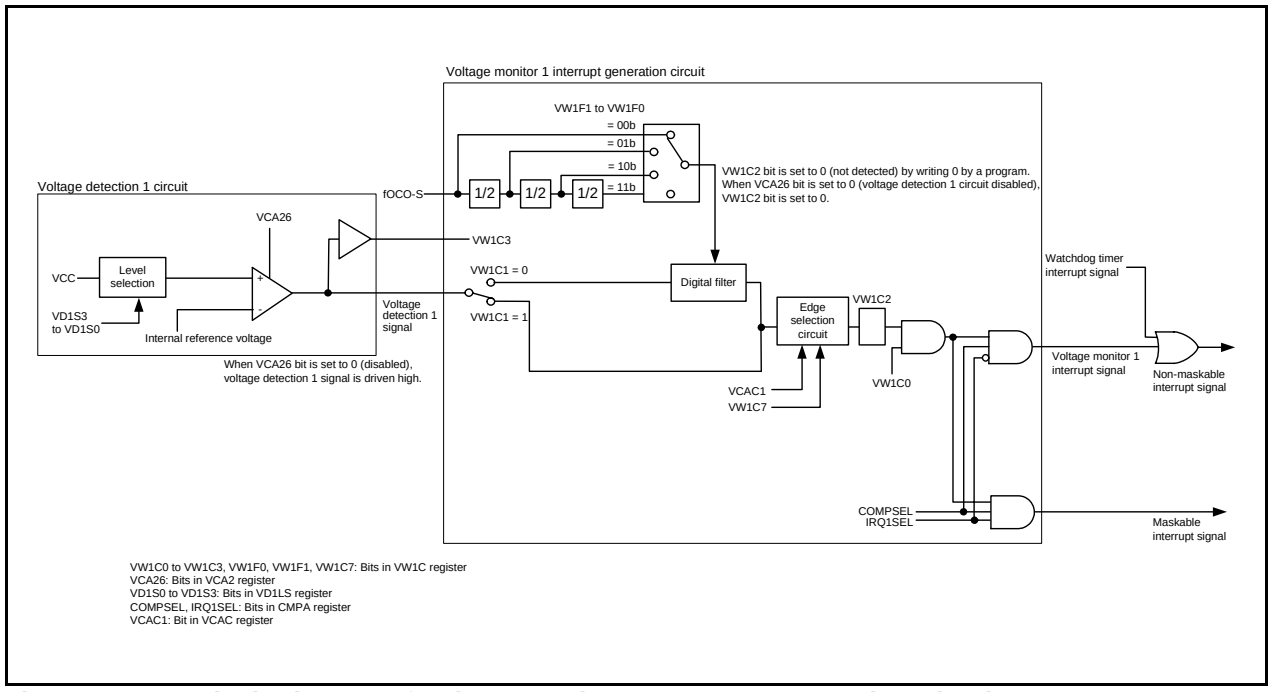


Figure 6.3 Block Diagram of Voltage Monitor 1 Interrupt Generation Circuit

6.2 Registers

6.2.1 Voltage Monitor Circuit Control Register (CMPA)

Address 0030h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	COMPSEL	—	—	IRQ1SEL	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	IRQ1SEL	Voltage monitor 1 interrupt type select bit (1)	0: Non-maskable interrupt 1: Maskable interrupt	R/W
b5	—	Reserved bits	Set to 0.	R/W
b6	—			
b7	COMPSEL	Voltage monitor interrupt type selection enable bit (1)	0: IRQ1SEL bit disabled 1: IRQ1SEL bit enabled	R/W

Note:
1. When the VW1C0 bit in the VW1C register is set to 1 (enabled), do not set bits IRQ1SEL and COMPSEL simultaneously (with one instruction).

6.2.2 Voltage Monitor Circuit Edge Select Register (VCAC)

Address 0031h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	VCAC1	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	VCAC1	Voltage monitor 1 circuit edge select bit (1)	0: One edge 1: Both edges	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When the VCAC1 bit is set to 0 (one edge), the VW1C7 bit in the VW1C register is enabled. Set the VW1C7 bit after setting the VCAC1 bit to 0.

6.2.3 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	VCA26	VCA25	—	—	—	—	VCA20
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (4)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	—	Reserved bit	Set to 0.	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **9.7.2.2 Reducing Internal Power Consumption Using VCA20 Bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

6.2.4 Voltage Detection 1 Level Select Register (VD1LS)

Address 0036h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VD1S3	VD1S2	VD1S1	VD1S0
After Reset	0	0	0	0	0	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	VD1S0	Voltage detection 1 level select bit (Reference voltage when the voltage falls)	b3 b2 b1 b0 0 0 1 0: 2.50 V (Vdet1_2) 0 1 0 1: 2.95 V (Vdet1_5) Other than above: Do not set.	R/W
b1	VD1S1			R/W
b2	VD1S2			R/W
b3	VD1S3			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VD1LS register.

Bits VD1S0 to VD1S3 (Voltage Detection 1 Level Select Bit)

The Vdet1 voltage to be monitored by the voltage detection 1 circuit is selected. When voltage monitor 1 interrupt is used, it is necessary to set either of Vdet1_2 or Vdet1_5. The value after reset is different from these set values, be careful.

6.2.5 Voltage Monitor 0 Circuit Control Register (VW0C)

Address 0038h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	VW0C0
After Reset	1	1	0	0	X	0	1	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	1	1	0	0	X	0	1	1

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VW0C0	Voltage monitor 0 reset enable bit (1)	0: Disabled 1: Enabled	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Reserved bit	When read, the content is undefined.	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—	Reserved bits	Set to 1.	R/W
b7	—			

Note:
1. The VW0C0 bit is enabled when the VCA25 bit in the VCA2 register is set to 1 (voltage detection 0 circuit enabled).
   When writing to the VW0C0 bit, set a value after reset.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW0C register.

6.2.6 Voltage Monitor 1 Circuit Control Register (VW1C)

Address 0039h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VW1C7	—	VW1F1	VW1F0	VW1C3	VW1C2	VW1C1	VW1C0
After Reset	1	0	0	0	1	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	VW1C0	Voltage monitor 1 interrupt enable bit (1)	0: Disabled 1: Enabled	R/W
b1	VW1C1	Voltage monitor 1 digital filter disable mode select bit (2, 6)	0: Digital filter enabled mode (digital filter circuit enabled) 1: Digital filter disable mode (digital filter circuit disabled)	R/W
b2	VW1C2	Voltage change detection flag (3, 4)	0: Not detected 1: Vdet1 passing detected	R/W
b3	VW1C3	Voltage detection 1 signal monitor flag (3)	0: VCC < Vdet1 1: VCC ≥ Vdet1 or voltage detection 1 circuit disabled	R
b4	VW1F0	Sampling clock select bit (6)	b5 b4 0 0: fOCO-S divided by 1 0 1: fOCO-S divided by 2 1 0: fOCO-S divided by 4 1 1: fOCO-S divided by 8	R/W
b5	VW1F1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	VW1C7	Voltage monitor 1 interrupt generation condition select bit (5)	0: When VCC reaches Vdet1 or above 1: When VCC reaches Vdet1 or below	R/W

Notes:

1. The VW1C0 is enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled). Set the VW1C0 bit to 0 (disabled) when the VCA26 bit is set to 0 (voltage detection 1 circuit disabled).
   To set the VW1C0 bit to 1 (enabled), follow the procedure shown in **Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt**.
2. When using the digital filter (while the VW1C1 bit is 0), set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on).
   To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
3. Bits VW1C2 and VW1C3 are enabled when the VCA26 bit in the VCA2 register is set to 1 (voltage detection 1 circuit enabled).
4. Set the VW1C2 bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).
5. The VW1C7 bit is enabled when the VCAC1 bit in the VCAC register is set to 0 (one edge). After setting the VCAC1 bit to 0, set the VW1C7 bit.
6. When the VW1C0 bit is set to 1 (enabled), do not set the VW1C1 bit and bits VW1F1 and VW1F0 simultaneously (with one instruction).

   Set the PRC3 bit in the PRCR register to 1 (write enabled) before writing the VW1C register.
   Rewriting the VW1C register may set the VW1C2 bit to 1. Set the VW1C2 bit to 0 after rewriting the VW1C register.

6.2.7 WDT Detection Flag (VW2C)

Address 003Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	VW2C3	—	—	—
After Reset	1	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	VW2C3	WDT detection monitor flag (1)	0: Not detected 1: Detected	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. Set this bit to 0 by a program. When 0 is written by a program, this bit is set to 0 (and remains unchanged even if 1 is written to it).

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VW2C register.

6.2.8 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: Do not set. 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   Initial value of OFS register is FFh. The value of OFS register changes as programmed by user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

6.3 VCC Input Voltage

6.3.1 Monitoring Vdet0

Vdet0 cannot be monitored.

6.3.2 Monitoring Vdet1

Once the following settings are made, the comparison result of voltage monitor 1 can be monitored by the VW1C3 bit in the VW1C register after td(E-A) has elapsed (refer to **28. Electrical Characteristics**).

(1) Set bits VD1S3 to VD1S0 in the VD1LS register (voltage detection 1 detection voltage).
(2) Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).

6.4 Voltage Monitor 0 Reset

To use voltage monitor 0 reset, set the LVDAS bit in the OFS register to 0 (voltage monitor 0 reset enabled after reset).

Figure 6.4 shows an Operating Example of Voltage Monitor 0 Reset.

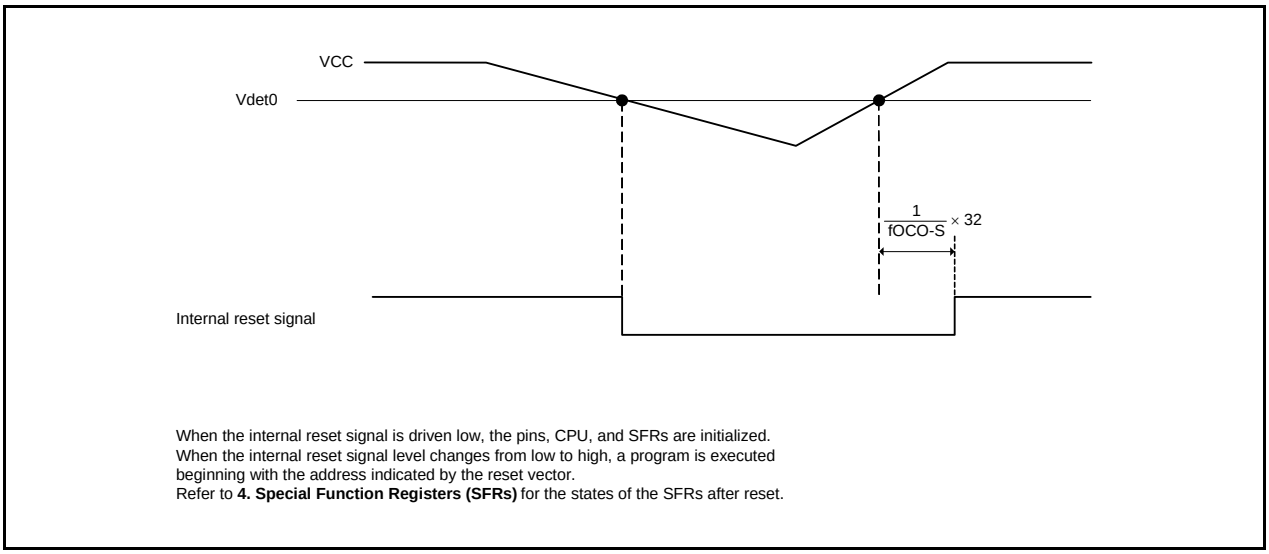


Figure 6.4 Operating Example of Voltage Monitor 0 Reset

6.5 Voltage Monitor 1 Interrupt

Table 6.2 lists the Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt. Figure 6.5 shows an Operating Example of Voltage Monitor 1 Interrupt.
To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).

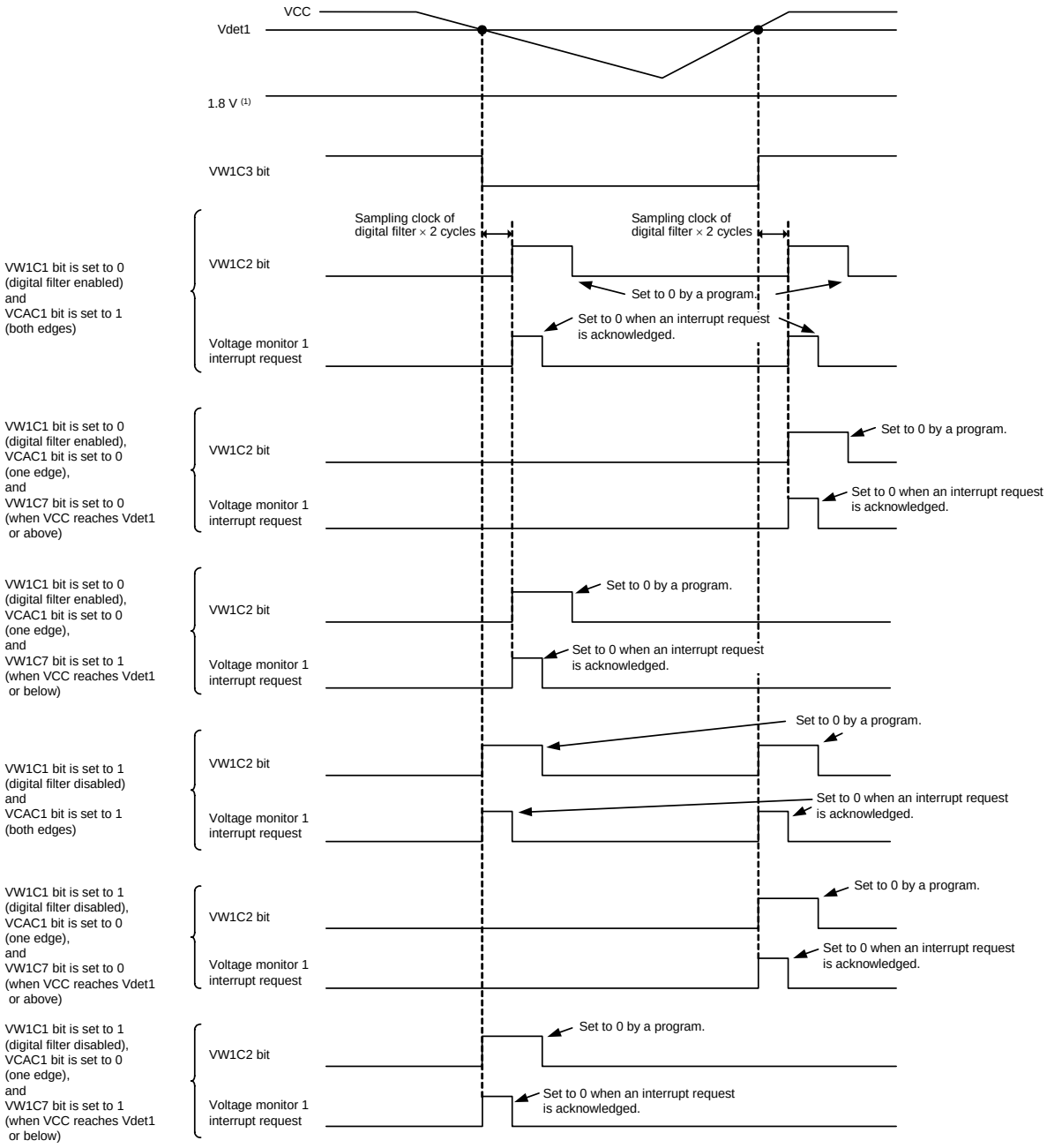
Table 6.2 Procedure for Setting Bits Associated with Voltage Monitor 1 Interrupt

Step	When Using Digital Filter	When Using No Digital Filter
1	Select the voltage detection 1 detection voltage by bits VD1S3 to VD1S0 in the VD1LS register.	
2	Set the VCA26 bit in the VCA2 register to 1 (voltage detection 1 circuit enabled).	
3	Wait for td(E-A).	
4	Set the COMPSEL bit in the CMPA register to 1.	
5 (1)	Select the interrupt type by the IRQ1SEL in the CMPA register.	
6	Select the sampling clock of the digital filter by bits VW1F0 and VW1F1 in the VW1C register.	Set the VW1C1 bit in the VW1C register to 1 (digital filter disabled).
7 (2)	Set the VW1C1 bit in the VW1C register to 0 (digital filter enabled).	—
8	Select the interrupt request timing by the VCAC1 bit in the VCAC register and the VW1C7 bit in the VW1C register.	
9	Set the VW1C2 bit in the VW1C register to 0.	
10	Set the CM14 bit in the CM1 register to 0 (low-speed on-chip oscillator on)	—
11	Wait for 2 cycles of the sampling clock of the digital filter	— (No wait time required)
12 (3)	Set the VW1C0 bit in the VW1C register to 1 (voltage monitor 1 interrupt enabled)	

Notes:
1. When the VW1C0 bit is set to 0, steps 4 and 5 can be executed simultaneously (with one instruction).
2. When the VW1C0 bit is set to 0, steps 6 and 7 can be executed simultaneously (with one instruction).
3. When the voltage detection 1 circuit is enabled while the voltage monitor 1 interrupt is disabled, low voltage is detected and the VW1C2 bit becomes 1.
   When low voltage is detected after the voltage detection 1 circuit is enabled until an interrupt is enabled for the setting procedure of bits associated with voltage monitor 1 interrupt, an interrupt is not generated. After an interrupt is enabled, read the VW1C2 bit. When the bit is read as 1, perform the process that occurs when low voltage is detected.

6.5.1 Digital Filter

When the VW1C1 bit in the VW1C register is set to 0 (digital filter enabled mode), the digital filter function to sample the voltage detection 1 signal is enabled. When the sampling results match twice in a row while the voltage detection 1 signal is sampled, its level will be held to be determined. Select the sampling clock using bits VW1F0 and VW1F1 in the VW1C register.
When using the digital filter (the VW1C1 bit is 0), set the CM14 bit in the CM1 register to (low-speed on-chip oscillator oscillation on).
To use the voltage monitor 1 interrupt to exit stop mode, set the VW1C1 bit to 1 (digital filter disabled mode).



VW1C1, VW1C2, VW1C3, VW1C7: Bits in VW1C register
VCAC1: Bit in VCAC register

The above applies when:
- VCA26 bit in VCA2 register = 1 (voltage detection 1 circuit enabled)
- VW1C0 bit in VW1C register = 1 (voltage monitor 1 interrupt enabled)

Note:
1. If voltage monitor 0 reset is not used, set the power supply to VCC ≥ 1.8 V.

Figure 6.5 Operating Example of Voltage Monitor 1 Interrupt

7. I/O Ports

There are 18 I/O ports P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5. (P4_3 and P4_4 can be used as I/O ports if the XCIN clock oscillation circuit is not used.)
Table 7.1 lists an Overview of I/O Ports.

Table 7.1 Overview of I/O Ports

Ports	I/O	Type of Output	I/O Setting	Internal Pull-Up Resister	Drive Capacity Switch	Input Level Switch
P0_4	I/O	CMOS3 state	Set in 1-bit units	Set in 1-bit units (1)	Set in 1-bit units (3)	Set in 1-bit units (4)
P1	I/O	CMOS3 state	Set in 1-bit units	Set in 4-bit units (1)	Set in 1-bit units (2)	Set in 8-bit units (4)
P3_0, P3_1, P3_3	I/O	CMOS3 state	Set in 1-bit units	Set in 3-bit units (1)	Set in 3-bit units (3)	Set in 6-bit units (4)
P3_4, P3_5, P3_7	I/O	CMOS3 state	Set in 1-bit units	Set in 3-bit units (1)	Set in 3-bit units (3)	
P4_3 (5)	I/O	CMOS3 state	Set in 1-bit units	Set in 1-bit units (1)	Set in 1-bit units (3)	Set in 3-bit units (4)
P4_4 (5), P4_5	I/O	CMOS3 state	Set in 1-bit units	Set in 2-bit units (1)	Set in 2-bit units (3)	

Notes:
1. In input mode, whether an internal pull-up resistor is connected or not can be selected by registers PUR0 and PUR1.
2. Whether the drive capacity of the output transistor is set to low or high can be selected using register P1DRR.
3. Whether the drive capacity of the output transistor is set to low or high can be selected using registers DRR0 and DRR1.
4. The input threshold value can be selected among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) using registers VLT0 and VLT1.
5. When the XCIN clock oscillation circuit is not used, these ports can be used as an I/O ports.

7.1 Functions of I/O Ports

The PDi_j (j = 0 to 7) bit in the PDi (i = 0, 1, 3, 4) register controls I/O of the ports P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5. The Pi register consists of a port latch to hold output data and a circuit to read pin states. Figures 7.1 to 7.9 show the Configurations of I/O Ports. Table 7.2 lists the Functions of I/O Ports.

Table 7.2 Functions of I/O Ports

Operation When Accessing Pi Register	Value of PDi_j Bit in PDi Register (1)	
	When PDi_j Bit is Set to 0 (Input Mode)	When PDi_j Bit is Set to 1 (Output Mode)
Read	Read the pin input level.	Read the port latch.
Write	Write to the port latch.	Write to the port latch. The value written to the port latch is output from the pin.

i = 0, 1, 3, 4, j = 0 to 7

Note:

1. Nothing is assigned to bits PD0_0 to PD0_3, PD0_5 to PD0_7, P3_2, P3_6, PD4_0 to PD4_2, PD4_6, P4_7.

7.2 Effect on Peripheral Functions

I/O ports function as I/O ports for peripheral functions (refer to **Table 1.5 Pin Name Information by Pin Number**).

Table 7.3 lists the Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0, 1, 3, 4, j = 0 to 7).

Refer to the description of each function for information on how to set peripheral functions.

Table 7.3 Setting of PDi_j Bit when Functioning as I/O Ports for Peripheral Functions (i = 0, 1, 3, 4, j = 0 to 7)

I/O of Peripheral Function	PDi_j Bit Settings for Shared Pin Function
Input	Set this bit to 0 (input mode).
Output	This bit can be set to either 0 or 1 (output regardless of the port setting).

7.3 Pins Other than I/O Ports

Figure 7.10 shows the Configuration of I/O Pins.

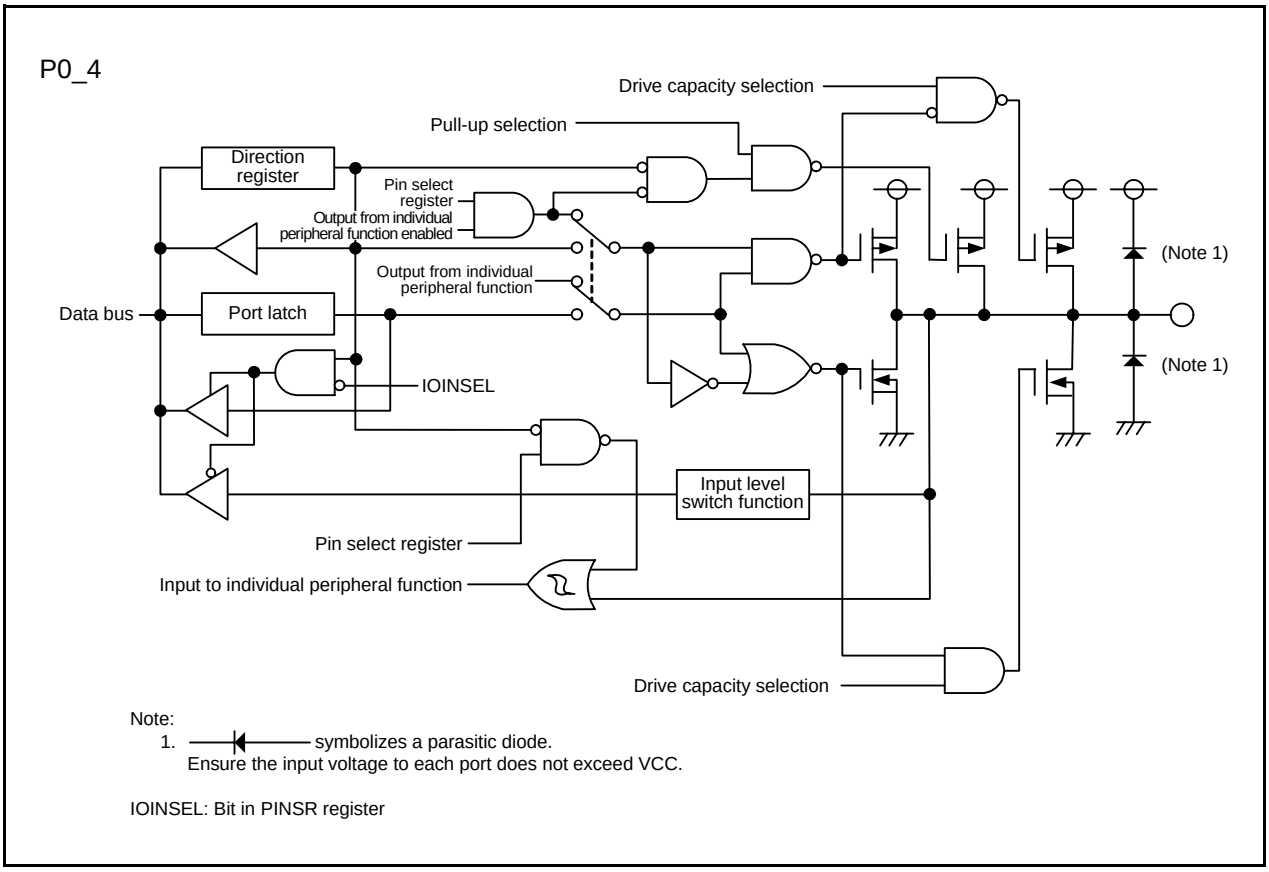


Figure 7.1 Configuration of I/O Ports (1)

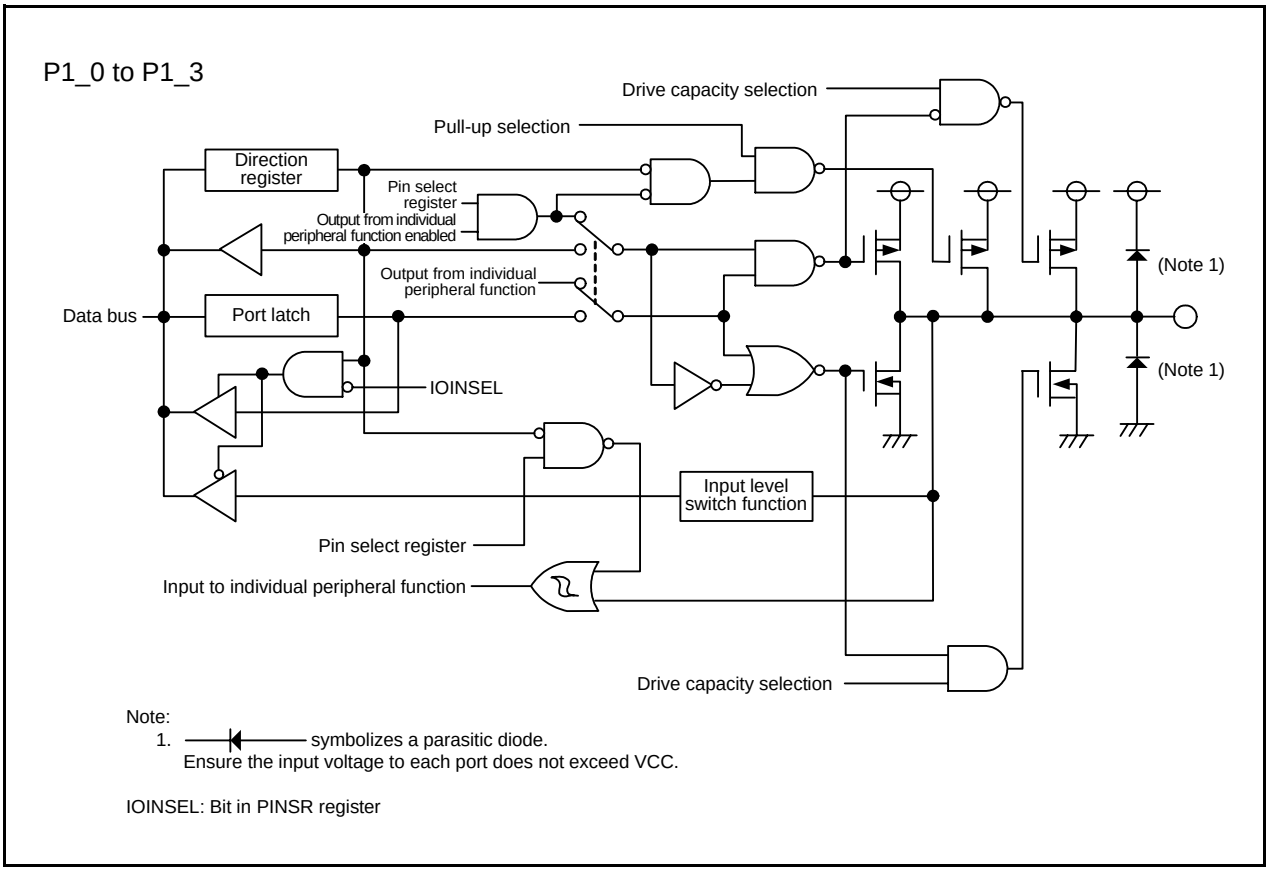


Figure 7.2 Configuration of I/O Ports (2)

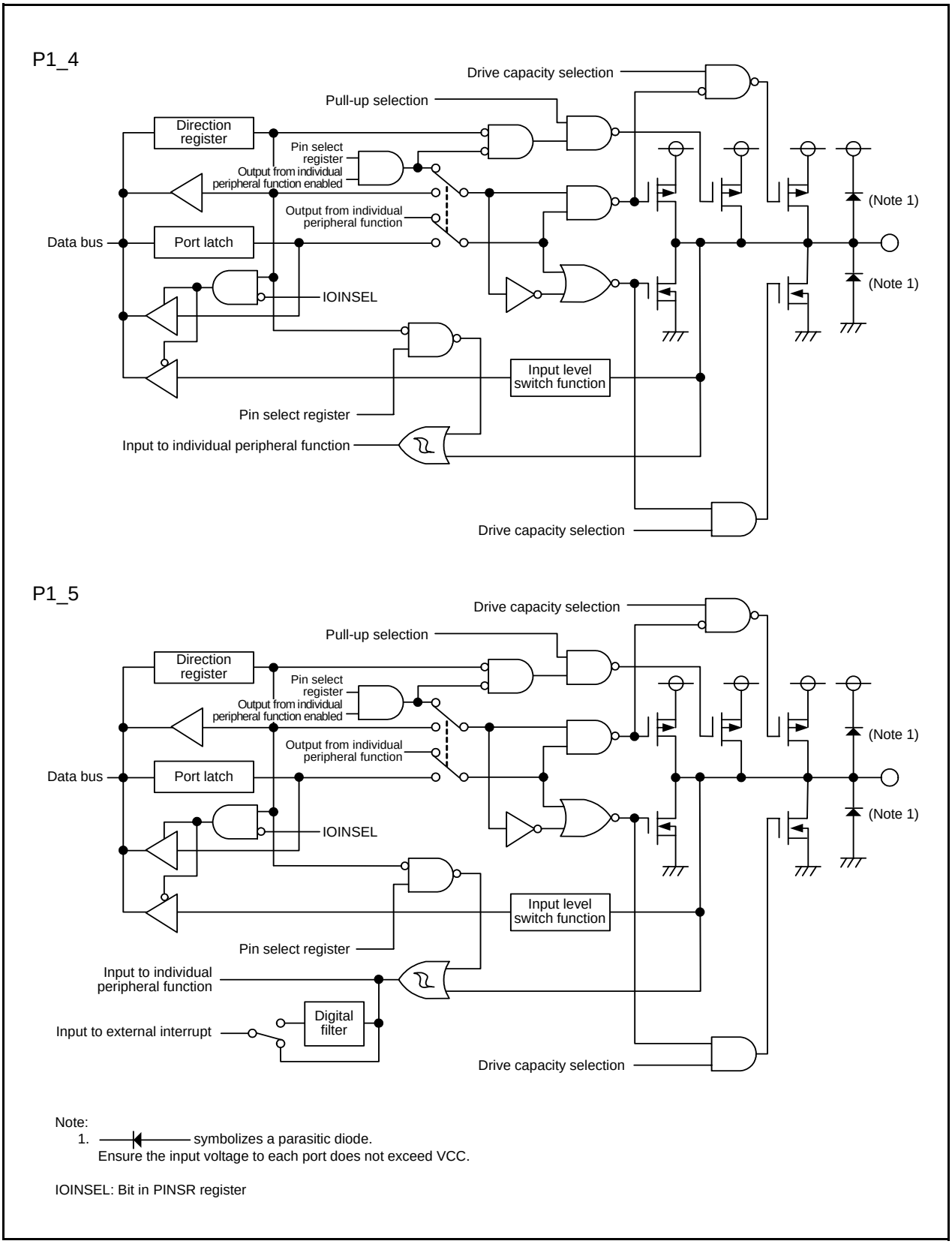


Figure 7.3 Configuration of I/O Ports (3)

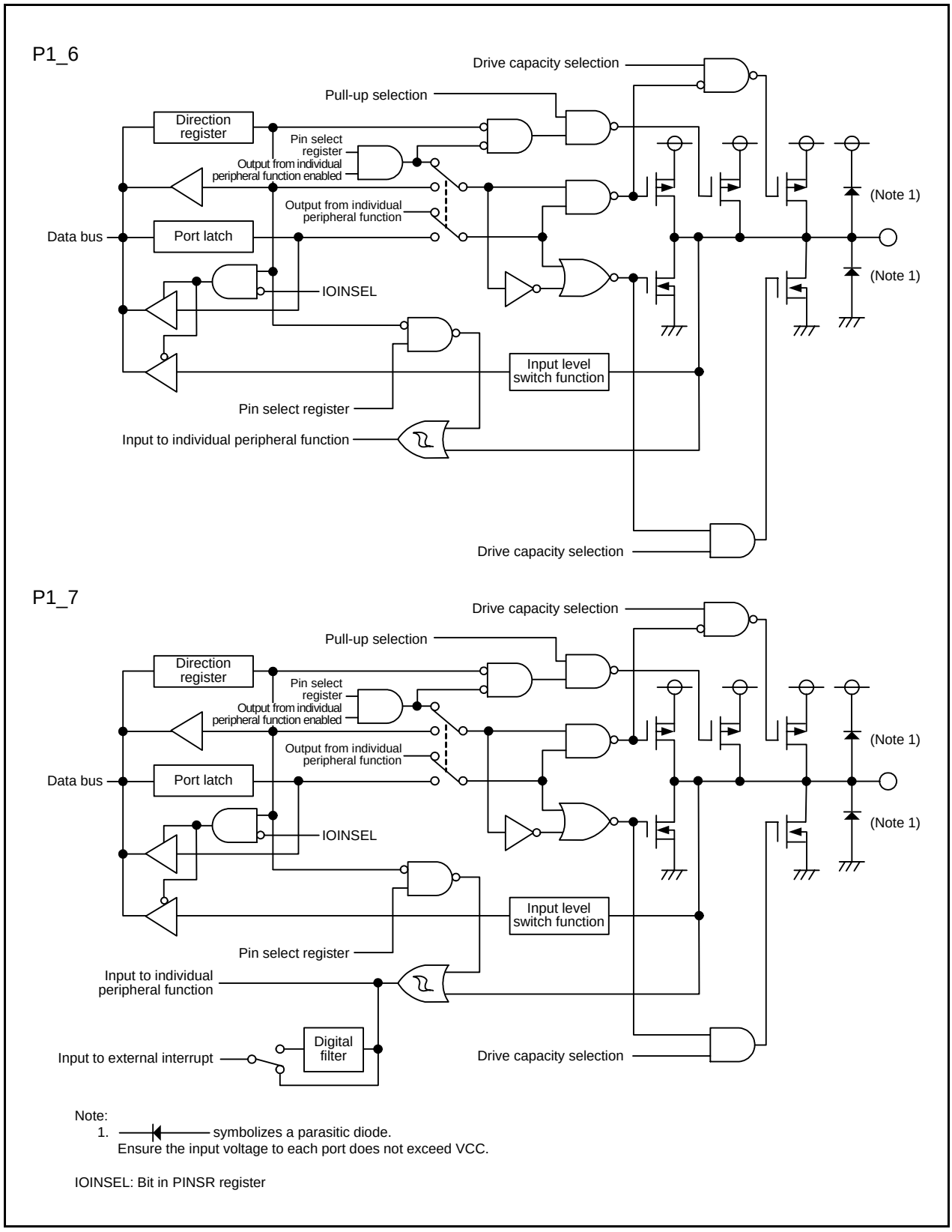


Figure 7.4 Configuration of I/O Ports (4)

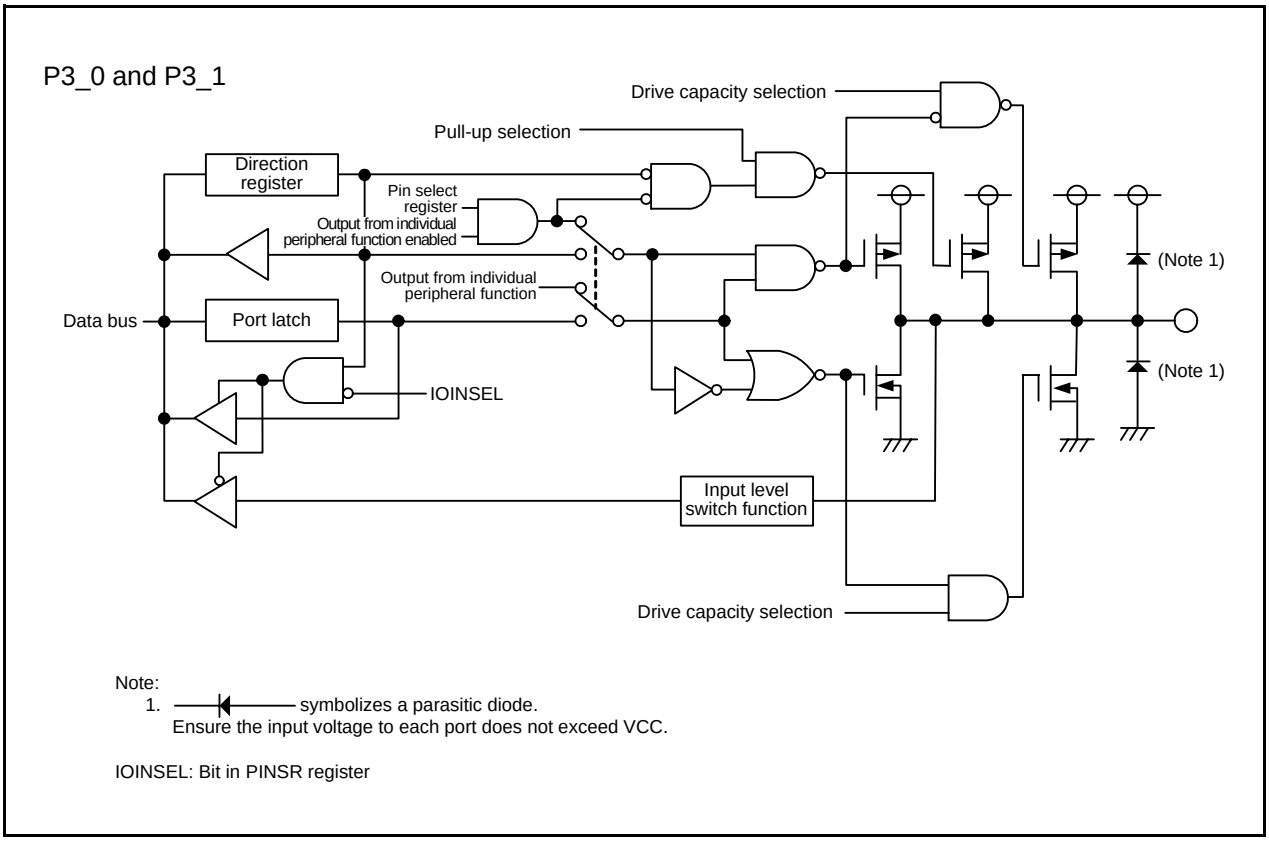
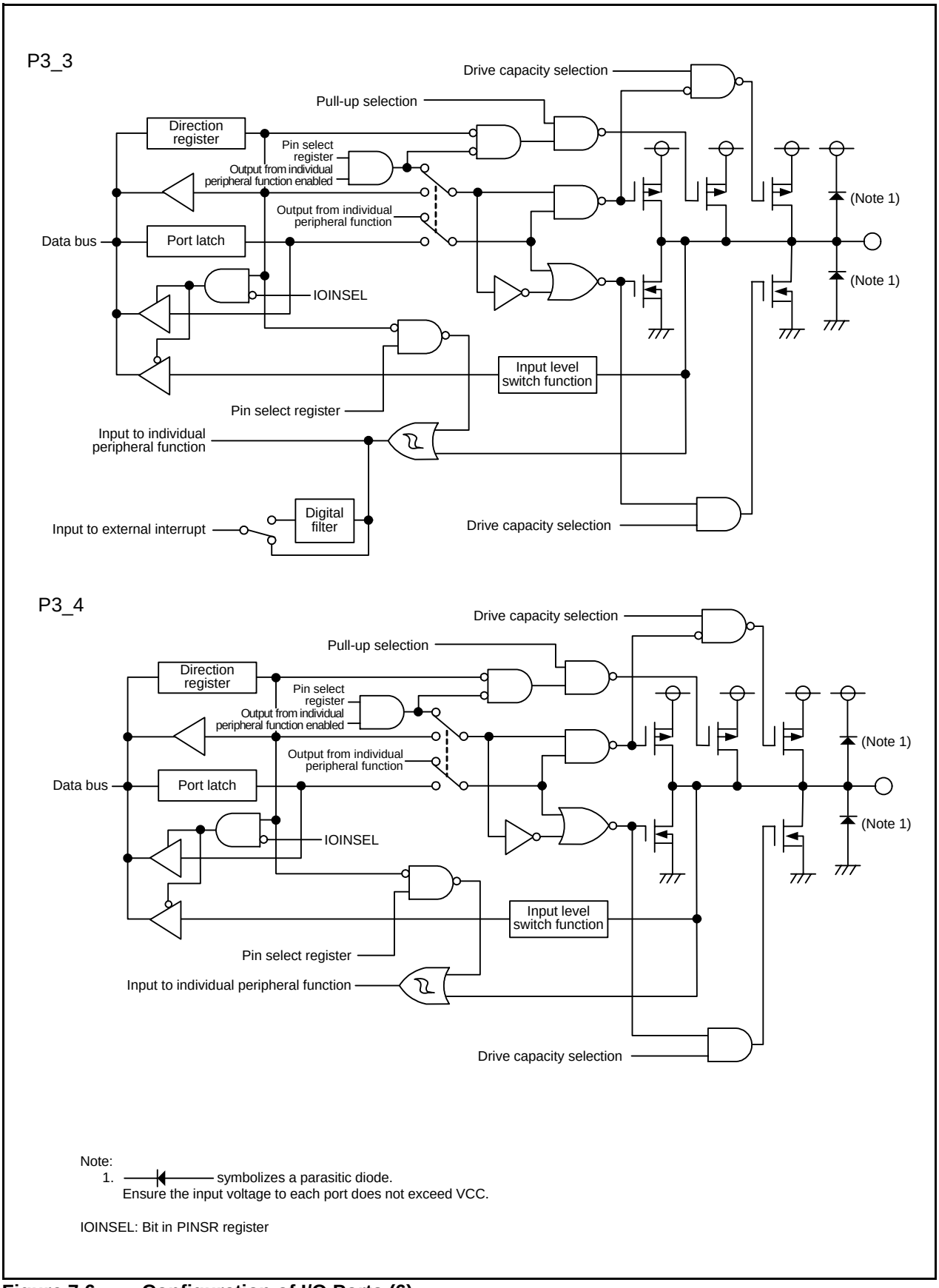


Figure 7.5 Configuration of I/O Ports (5)



Note:
1. ⟵| symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

IOINSEL: Bit in PINSR register

Figure 7.6 Configuration of I/O Ports (6)

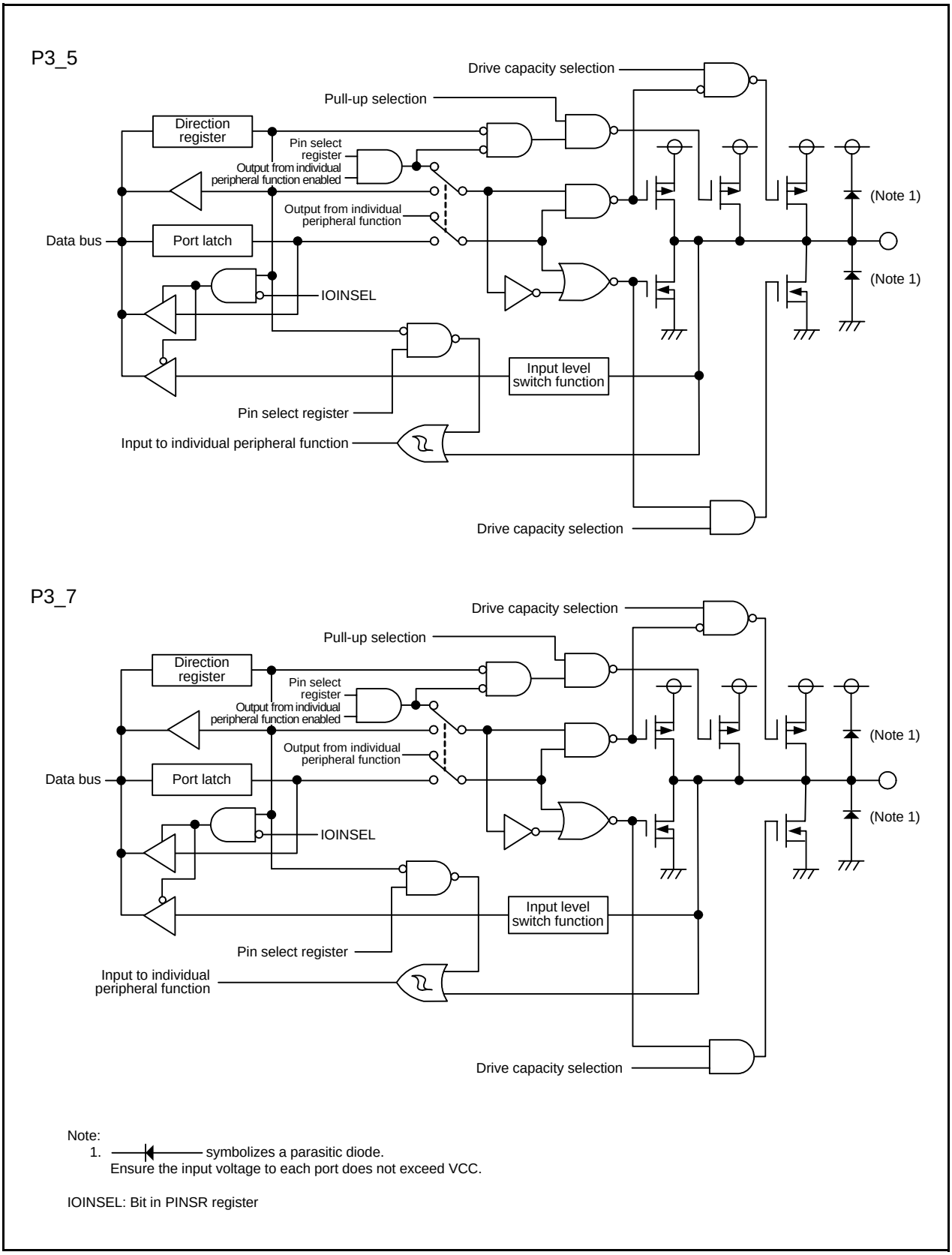
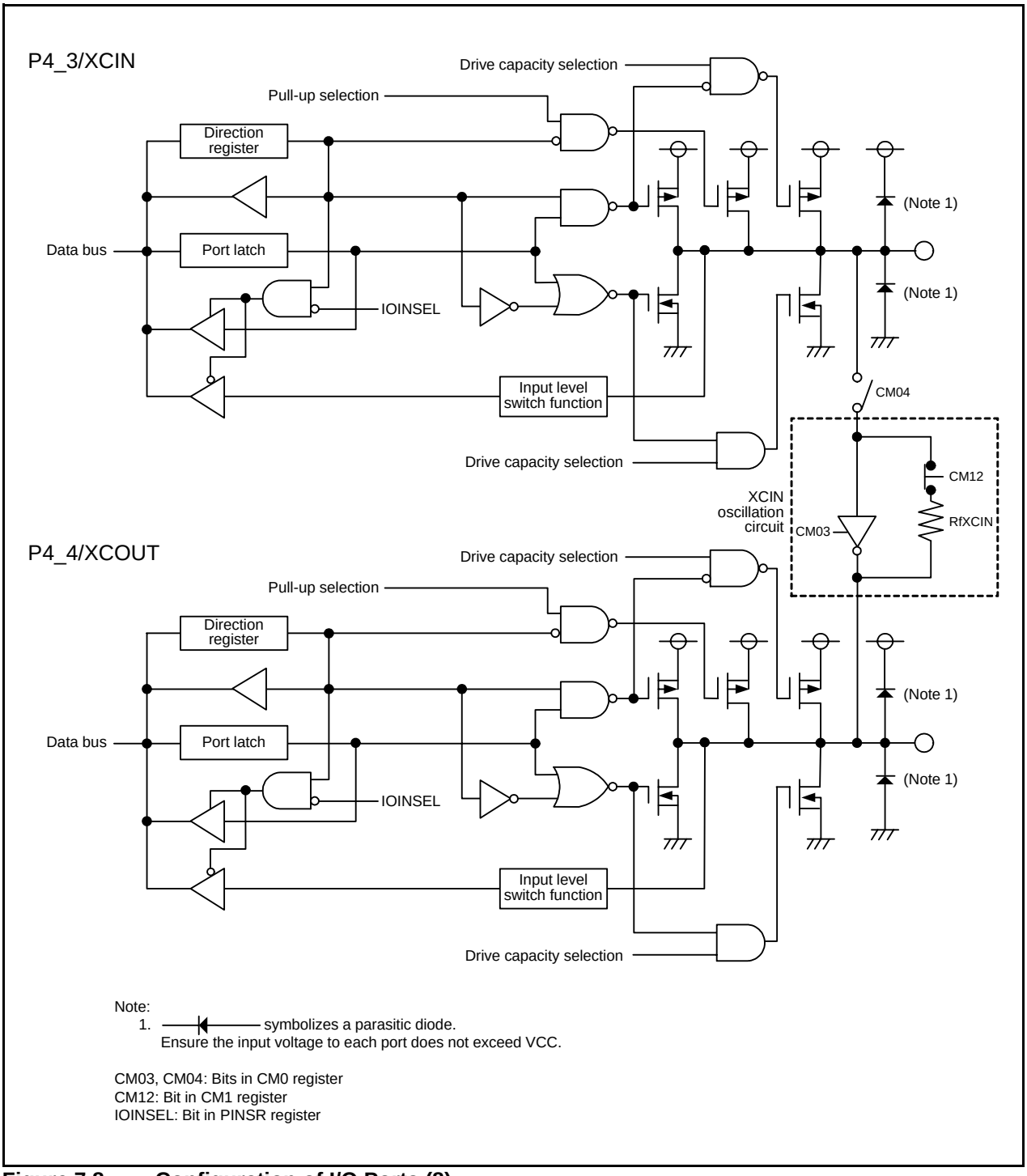


Figure 7.7 Configuration of I/O Ports (7)



Note:
1. ⟵ symbolizes a parasitic diode.
Ensure the input voltage to each port does not exceed VCC.

CM03, CM04: Bits in CM0 register
CM12: Bit in CM1 register
IOINSEL: Bit in PINSR register

Figure 7.8 Configuration of I/O Ports (8)

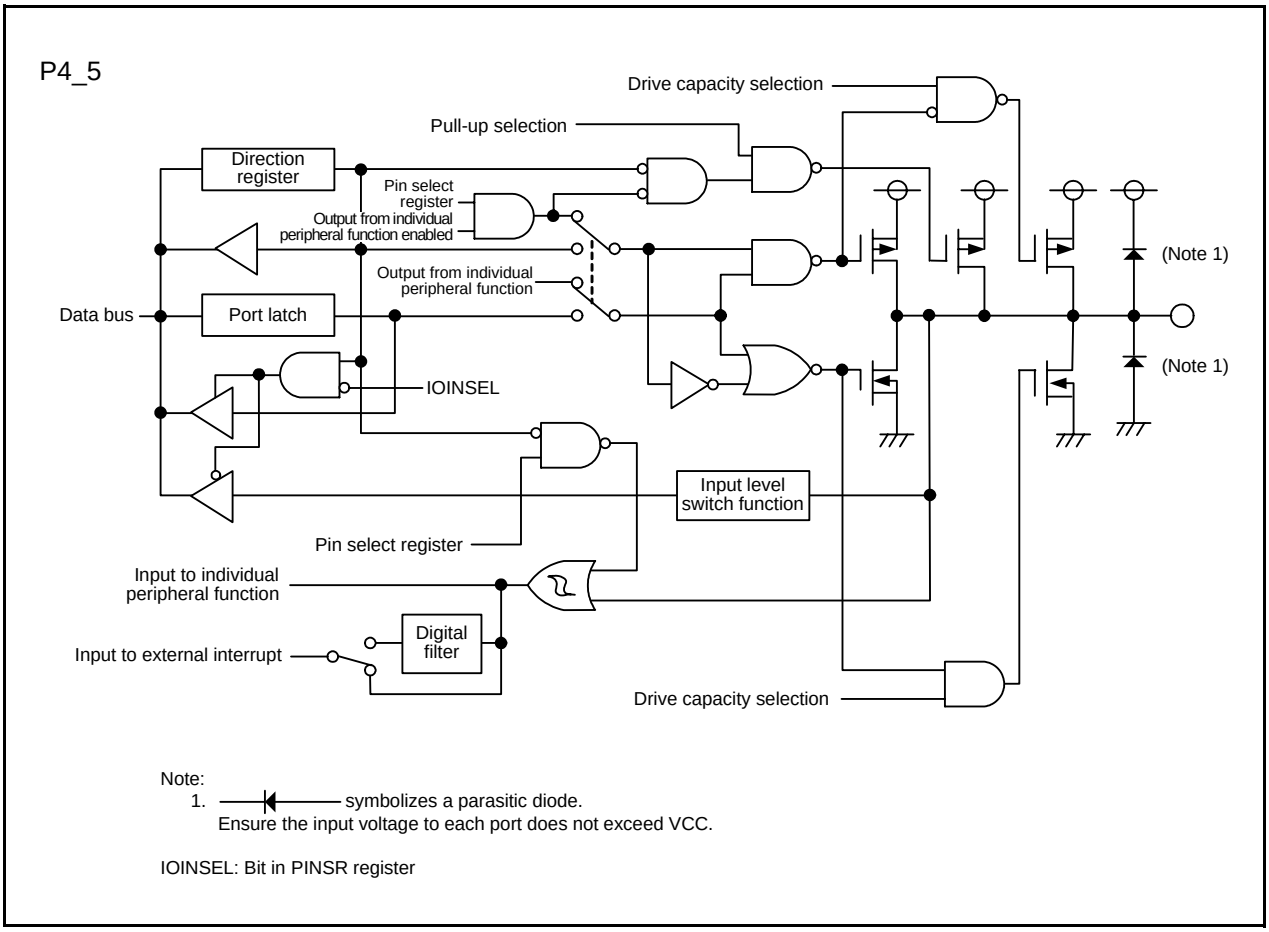


Figure 7.9 Configuration of I/O Ports (9)

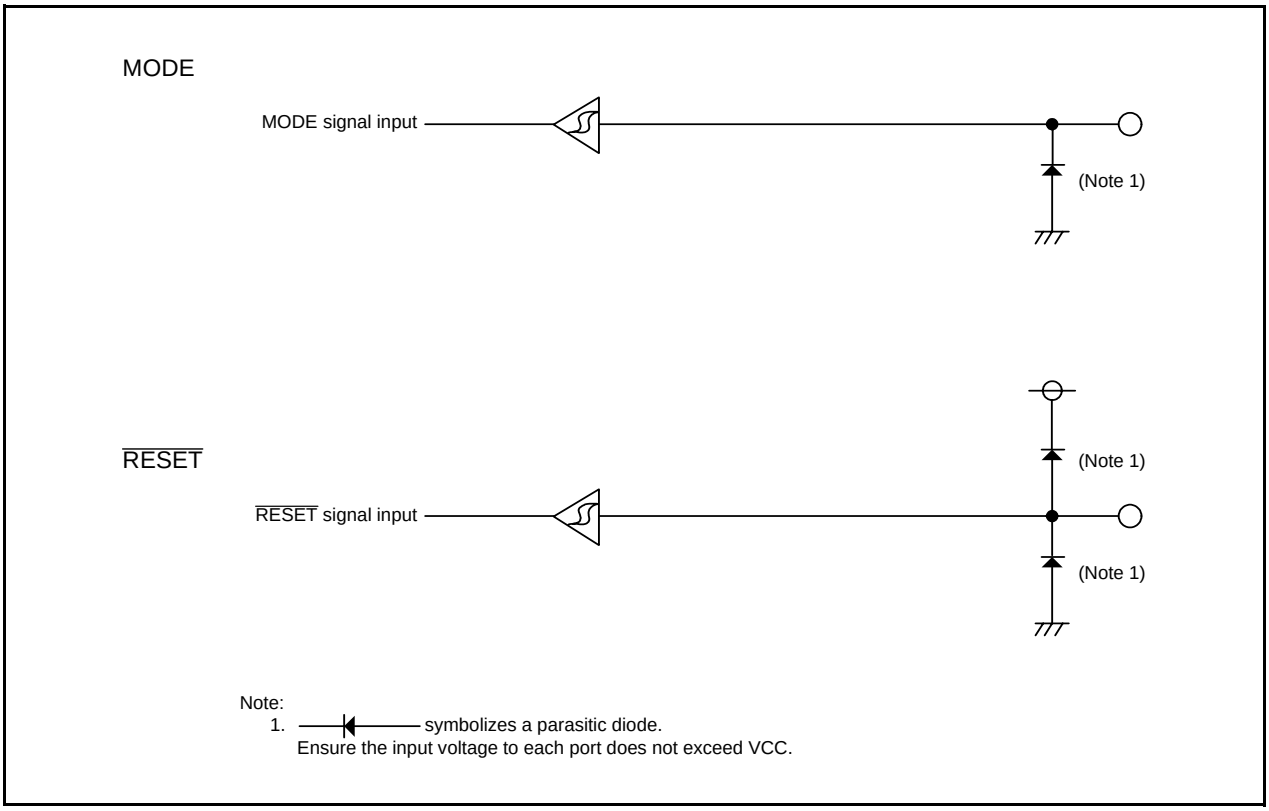


Figure 7.10 Configuration of I/O Pins

7.4 Registers

7.4.1 Port Pi Direction Register (PDi) (i = 0, 1, 3, 4)

Address 00E2h (PD0 (1, 2)), 00E3h (PD1), 00E7h (PD3 (3)), 00EAh (PD4 (4))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PDi_7	PDi_6	PDi_5	PDi_4	PDi_3	PDi_2	PDi_1	PDi_0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PDi_0	Port Pi_0 direction bit	0: Input mode (functions as an input port) 1: Output mode (functions as an output port)	R/W
b1	PDi_1	Port Pi_1 direction bit		R/W
b2	PDi_2	Port Pi_2 direction bit		R/W
b3	PDi_3	Port Pi_3 direction bit		R/W
b4	PDi_4	Port Pi_4 direction bit		R/W
b5	PDi_5	Port Pi_5 direction bit		R/W
b6	PDi_6	Port Pi_6 direction bit		R/W
b7	PDi_7	Port Pi_7 direction bit		R/W

Notes:
1. Write to the PD0 register with the next instruction after that used to set the PRC2 bit in the PRCR register to 1 (write enabled).
2. Bits PD0_0 to PD0_3, and PD0_5 to PD0_7 in the PD0 register are unavailable on this MCU.
   If it is necessary to set bits PD0_0 to PD0_3, PD0_5 to PD0_7 in the PD0 register, set to 0. When read, the content is 0.
3. Bits PD3_2 and PD3_6 in the PD3 register are unavailable on this MCU.
   If it is necessary to set bits PD3_2, PD3_6 in the PD3 register, set to 0. When read, the content is 0.
4. Bits PD4_0 to PD4_2, PD4_6 and PD4_7 in the PD4 register are unavailable on this MCU.
   If it is necessary to set bits PD4_0 to PD4_2, PD4_6 and PD4_7 in the PD4 register, set to 0. When read, the content is 0.

The PDi register selects whether I/O ports are used for input or output. Each bit in the PDi register corresponds to one port.

7.4.2 Port Pi Register (Pi) (i = 0, 1, 3, 4)

Address 00E0h (P0 (1)), 00E1h (P1), 00E5h (P3 (2)), 00E8h (P4 (3))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	Pi_7	Pi_6	Pi_5	Pi_4	Pi_3	Pi_2	Pi_1	Pi_0
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	Pi_0	Port Pi_0 bit	0: “L” level 1: “H” level	R/W
b1	Pi_1	Port Pi_1 bit		R/W
b2	Pi_2	Port Pi_2 bit		R/W
b3	Pi_3	Port Pi_3 bit		R/W
b4	Pi_4	Port Pi_4 bit		R/W
b5	Pi_5	Port Pi_5 bit		R/W
b6	Pi_6	Port Pi_6 bit		R/W
b7	Pi_7	Port Pi_7 bit		R/W

Notes:
1. Bits P0_0 to P0_3, and P0_5 to P0_7 in the P0 register are unavailable on this MCU.
   If it is necessary to set bits P0_0 to P0_3, P0_5 to P0_7 in the P0 register, set to 0. When read, the content is 0.
2. Bits P3_2 and P3_6 in the P3 register are unavailable on this MCU.
   If it is necessary to set bits P3_2, P3_6 in the P3 register, set to 0. When read, the content is 0.
3. Bits P4_0 to P4_2, P4_6 and P4_7 in the P4 register are unavailable on this MCU.
   If it is necessary to set bits P4_0 to P4_2, P4_6 and P4_7 in the P4 register, set to 0. When read, the content is 0.

Data input and output to and from external devices are accomplished by reading and writing to the Pi register. The Pi register consists of a port latch to retain output data and a circuit to read the pin status. The value written in the port latch is output from the pin. Each bit in the Pi register corresponds to one port.

Pi_j Bit (i = 0, 1, 3, 4, j = 0 to 7) (Port Pi_j Bit)

The pin level of any I/O port which is set to input mode can be read by reading the corresponding bit in this register. The pin level of any I/O port which is set to output mode can be controlled by writing to the corresponding bit in this register.

7.4.3 Timer RA Pin Select Register (TRASR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	TRAOSEL1	TRAOSEL0	—	TRAIOSEL1	TRAIOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO pin select bit	b1 b0 0 0: TRAIO pin not used 0 1: P1_7 assigned 1 0: P1_5 assigned 1 1: Do not set.	R/W
b1	TRAIOSEL1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	TRAOSEL0	TRAO pin select bit	b4 b3 0 0: P3_7 assigned 0 1: P3_0 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b4	TRAOSEL1			R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The TRASR register selects which pin is assigned to the timer RA I/O. To use the I/O pin for timer RA, set this register.
Set the TRASR register before setting the timer RA associated registers. Also, do not change the setting value in this register during timer RA operation.

7.4.4 Timer RB/RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCCLKSEL1	TRCCLKSEL0	—	—	—	TRBOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRBOSEL0	TRBO pin select bit	0: P1_3 assigned 1: P3_1 assigned	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	TRCCLKSEL0	TRCCLK pin select bit	b5 b4 0 0: TRCCLK pin not used 0 1: P1_4 assigned 1 0: P3_3 assigned 1 1: Do not set.	R/W
b5	TRCCLKSEL1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRBRCSR register selects which pin is assigned to the timer RB and timer RC I/O. To use the I/O pin for timer RB and timer RC, set this register.
Set the TRBOSEL0 bit before setting the timer RB associated registers. Set bits TRCCLKSEL0 to TRCCLKSEL1 before setting the timer RC associated registers. Also, do not change the setting values of the TRBOSEL0 bit during timer RB operation. Do not change the setting values of bits TRCCLKSEL0 to TRCCLKSEL1 during timer RC operation.

7.4.5 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIOBSEL2	TRCIOBSEL1	TRCIOBSEL0	—	TRCIOASEL2	TRCIOASEL1	TRCIOASEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b2 b1 b0 0 0 0: TRCIOA/TRCTRG pin not used 0 0 1: P1_1 assigned Other than above: Do not set.	R/W
b1	TRCIOASEL1			R/W
b2	TRCIOASEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIOBSEL0	TRCIOB pin select bit	b6 b5 b4 0 0 0: TRCIOB pin not used 0 0 1: P1_2 assigned 0 1 1: P0_4 assigned Other than above: Do not set.	R/W
b5	TRCIOBSEL1			R/W
b6	TRCIOBSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR0 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

7.4.6 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIODSEL2	TRCIODSEL1	TRCIODSEL0	—	TRCIOCSEL2	TRCIOCSEL1	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	b2 b1 b0 0 0 0: TRCIOC pin not used 0 0 1: P1_3 assigned 0 1 0: P3_4 assigned Other than above: Do not set.	R/W
b1	TRCIOCSEL1			R/W
b2	TRCIOCSEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIODSEL0	TRCIOD pin select bit	b6 b5 b4 0 0 0: TRCIOD pin not used 0 0 1: P1_0 assigned 0 1 0: P3_5 assigned Other than above: Do not set.	R/W
b5	TRCIODSEL1			R/W
b6	TRCIODSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR1 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

7.4.7 UART0 Pin Select Register (U0SR)

Address 0188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK0SEL0	—	RXD0SEL0	—	TXD0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	0: TXD0 pin not used 1: P1_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD0SEL0	RXD0 pin select bit	0: RXD0 pin not used 1: P1_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	CLK0SEL0	CLK0 pin select bit	0: CLK0 pin not used 1: P1_6 assigned	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U0SR register selects which pin is assigned to the UART0 I/O. To use the I/O pin for UART0, set this register.
Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value in this register during UART0 operation.

7.4.8 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I^{2}C bus switch bit	0: SSU function selected 1: I^{2}C bus function selected	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

7.4.9 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INT1SEL2	INT1SEL1	INT1SEL0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	b3 b2 b1 0 0 0: P1_7 assigned 0 0 1: P1_5 assigned Other than above: Do not set.	R/W
b2	INT1SEL1			R/W
b3	INT1SEL2			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

The INTSR register selects which pin is assigned to the $\overline{\text{INT1}}$ input. To use $\overline{\text{INT1}}$, set this register.
Set the INTSR register before setting the $\overline{\text{INT1}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INT1}}$ operation.

7.4.10 I/O Function Pin Select Register (PINSR)

Address 018Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SDADLY1	SDADLY0	IICTCHALF	IICTCTWI	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i =0, 1, 3, 4) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read. When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read. 1: The I/O port input function reads the pin input level regardless of the PDi register	R/W
b4	IICTCTWI	I^2C double transfer rate select bit (1)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is twice the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b5	IICTCHALF	I^2C half transfer rate select bit (1)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is half the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b6	SDADLY0	SDA digital delay select bit	b7 b6 0 0: Digital delay of 3 × f1 cycles 0 1: Digital delay of 11 × f1 cycles 1 0: Digital delay of 19 × f1 cycles 1 1: Do not set.	R/W
b7	SDADLY1			R/W

Note:
1. Do not set both the IICTCTWI and IICTCHALF bits to 1 when the I^2C bus function is used. Set these bits to 0 when the SSU function is used.

IOINSEL Bit (I/O port input function select bit)

The IOINSEL bit is used to select the pin level of an I/O port when the PDi_j (j = 0 to 7) bit in the PDi (i = 0, 1, 3, 4) register is set to 1 (output mode). When this bit is set to 1, the I/O port input function reads the pin input level regardless of the PDi register.

Table 7.4 lists I/O Port Values Read by Using IOINSEL Bit. The IOINSEL bit can be used to change the input function of all I/O ports.

Table 7.4 I/O Port Values Read by Using IOINSEL Bit

PDi_j bit in PDi register	0 (input mode)		1 (output mode)	
IOINSEL bit	0	1	0	1
I/O port values read	Pin input level		Port latch value	Pin input level

7.4.11 Pull-Up Control Register 0 (PUR0)

Address 01E0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PU07	PU06	—	—	PU03	PU02	PU01	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	PU01	P0_4 pull-up	0: Not pulled up 1: Pulled up (1)	R/W
b2	PU02	P1_0 to P1_3 pull-up		R/W
b3	PU03	P1_4 to P1_7 pull-up		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	PU06	P3_0, P3_1, and P3_3 pull-up	0: Not pulled up	R/W
b7	PU07	P3_4, P3_5, and P3_7 pull-up	1: Pulled up (1)	R/W

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

   For pins used as input, the setting values in the PUR0 register are valid.

7.4.12 Pull-Up Control Register 1 (PUR1)

Address 01E1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	PU11	PU10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PU10	P4_3 pull-up	0: Not pulled up	R/W
b1	PU11	P4_4, and P4_5 pull-up	1: Pulled up (1)	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When this bit is set to 1 (pulled up), the pin whose port direction bit is set to 0 (input mode) is pulled up.

   For pins used as input, the setting values in the PUR1 register are valid.

7.4.13 Port P1 Drive Capacity Control Register (P1DRR)

Address 01F0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	P1DRR7	P1DRR6	P1DRR5	P1DRR4	P1DRR3	P1DRR2	P1DRR1	P1DRR0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	P1DRR0	P1_0 drive capacity	0: Low 1: High (1)	R/W
b1	P1DRR1	P1_1 drive capacity		R/W
b2	P1DRR2	P1_2 drive capacity		R/W
b3	P1DRR3	P1_3 drive capacity		R/W
b4	P1DRR4	P1_4 drive capacity		R/W
b5	P1DRR5	P1_5 drive capacity		R/W
b6	P1DRR6	P1_6 drive capacity		R/W
b7	P1DRR7	P1_7 drive capacity		R/W

Note:
1. Both “H” and “L” output are set to high drive capacity.

The P1DRR register selects whether the drive capacity of the P1 output transistor is set to low or high.
The P1DRRi bit (i = 0 to 7) is used to select whether the drive capacity of the output transistor is set to low or high for each pin.
For pins used as output, the setting values in the P1DRR register are valid.

7.4.14 Drive Capacity Control Register 0 (DRR0)

Address 01F2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DRR07	DRR06	—	—	—	—	DRR01	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	DRR01	P0_4 drive capacity	0: Low 1: High (1)	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	DRR06	P3_0, P3_1, and P3_3 drive capacity	0: Low	R/W
b7	DRR07	P3_4, P3_5, and P3_7 drive capacity	1: High (1)	R/W

Note:
1. Both “H” and “L” output are set to high drive capacity.

For pins used as output, the setting values in the DRR0 register are valid.

DRR01 Bit (P0_4 drive capacity)

The DRR01 bit selects whether the drive capacity of the P0_4 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for one pin.

DRR06 Bit (P3_0, P3_1, P3_3 drive capacity)

The DRR06 bit selects whether the drive capacity of the P3_0, P3_1, P3_3 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for three pins.

DRR07 Bit (P3_4, P3_5, P3_7 drive capacity)

The DRR07 bit selects whether the drive capacity of the P3_4, P3_5, P3_7 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for three pins.

7.4.15 Drive Capacity Control Register 1 (DRR1)

Address 01F3h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	DRR11	DRR10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DRR10	P4_3 drive capacity	0: Low	R/W
b1	DRR11	P4_4 and P4_5 drive capacity	1: High (1)	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b7	—			

Note:
1. Both “H” and “L” output are set to high drive capacity.

For pins used as output, the setting values in the DRR1 register are valid.

DRR10 Bit (P4_3 drive capacity)

The DRR10 bit selects whether the drive capacity of the P4_3 output transistor is set to low or high. This bit is used to select whether the drive capacity of the output transistor is set to low or high for one pin.

DRR11 Bit (P4_4 and P4_5 drive capacity)

The DRR11 bit selects whether the drive capacity of the P4_4 and P4_5 output transistors is set to low or high. This bit is used to select whether the drive capacity of the output transistors is set to low or high for two pins.

7.4.16 Input Threshold Control Register 0 (VLT0)

Address 01F5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	VLT07	VLT06	—	—	VLT03	VLT02	VLT01	VLT00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT00	P0 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT01			R/W
b2	VLT02	P1 input level select bit	b3 b2 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b3	VLT03			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	VLT06	P3_0, P3_1, P3_3 to P3_5, and P3_7 input level select bit	b7 b6 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b7	VLT07			R/W

The VLT0 register selects the voltage level of the input threshold values for ports P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7. Bits VLT00 to VLT03 and VLT06, VLT07 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC) for every eight pins.

7.4.17 Input Threshold Control Register 1 (VLT1)

Address 01F6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	VLT11	VLT10
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	VLT10	P4_3 to P4_5 input level select bit	b1 b0 0 0: 0.50 × VCC 0 1: 0.35 × VCC 1 0: 0.70 × VCC 1 1: Do not set.	R/W
b1	VLT11			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b7	—			

The VLT1 register selects the voltage level of the input threshold values for ports P4_3 to P4_5. Bits VLT10 and VLT11 are used to select the input threshold values among three voltage levels (0.35 VCC, 0.50 VCC, and 0.70 VCC).

7.5 Port Settings

Tables 7.5 to 7.27 list the port settings.

Table 7.5 Port 0_4/TREO/TRCIOB/ASW

Register	PD0	TRECR1	TRCPSR0			BBANTSWCON	Timer RC Setting	Function
Bit	PD0_4	TOENA	TRCIOBSEL			ANTSWEN	—	
			2	1	0			
Setting Value	0	0	Other than 011b			0	X	Input port (1)
	1	0	Other than 011b			0	X	Output port (2)
	X	1	Other than 011b			0	X	TREO output (2)
	0	X	0	1	1	0	Refer to **Table 7.25 TRCIOB Pin Setting**	TRCIOB input (1)
	X	X	0	1	1	0	Refer to **Table 7.25 TRCIOB Pin Setting**	TRCIOB output (2)
	0	X	X	X	X	1	X	ANTSW output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU01 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR01 bit in the DRR0 register to 1.

Table 7.6 Port 1_0/$\overline{\text{KI0}}$/TRCIOD

Register	PD1	KIEN	TRCPSR1			Timer RC Setting	Function
Bit	PD1_0	KI0EN	TRCIODSEL			—	
			2	1	0		
Setting Value	0	X	Other than 001b			X	Input port (1)
	1	X	Other than 001b			X	Output port (2)
	0	1	Other than 001b			X	$\overline{\text{KI0}}$ input (1)
	0	X	0	0	1	Refer to **Table 7.27 TRCIOD Pin Setting**	TRCIOD input (1)
	X	X	0	0	1	Refer to **Table 7.27 TRCIOD Pin Setting**	TRCIOD output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR0 bit in the P1DRR register to 1.

Table 7.7 Port 1_1/$\overline{\text{KI1}}$/TRCIOA/TRCTRG

Register	PD1	KIEN	TRCPSR0			Timer RC Setting	Function
Bit	PD1_1	KI1EN	TRCIOASEL			—	
			2	1	0		
Setting Value	0	X	Other than 001b			X	Input port (1)
	1	X	Other than 001b			X	Output port (2)
	0	1	Other than 001b			X	$\overline{\text{KI1}}$ input (1)
	0	X	0	0	1	Refer to **Table 7.24 TRCIOA Pin Setting**	TRCIOA input (1)
	X	X	0	0	1	Refer to **Table 7.24 TRCIOA Pin Setting**	TRCIOA output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR1 bit in the P1DRR register to 1.

Table 7.8 Port 1_2/$\overline{\text{KI2}}$//TRCIOB

Register	PD1	KIEN	TRCPSR0			Timer RC Setting	Function
Bit	PD1_2	KI2EN	TRCIOBSEL			—	
			2	1	0		
Setting Value	0	X	Other than 001b			X	Input port (1)
	1	X	Other than 001b			X	Output port (2)
	0	1	Other than 001b			X	$\overline{\text{KI2}}$ input (1)
	0	X	0	0	1	Refer to **Table 7.25 TRCIOB Pin Setting**	TRCIOB input (1)
	X	X	0	0	1	Refer to **Table 7.25 TRCIOB Pin Setting**	TRCIOB output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR2 bit in the P1DRR register to 1.

Table 7.9 Port 1_3/$\overline{\text{KI3}}$/TRBO/TRCIOC

Register	PD1	KIEN	TRBRCSR	TRCPSR1			Timer RB Setting	Timer RC Setting	Function
Bit	PD1_3	KI3EN	TRBOSEL0	TRCIOCSEL			—	—	
				2	1	0			
Setting Value	0	X	1	Other than 001b			X	X	Input port (1)
			X				Other than TRBO usage conditions		
	1	X	1	Other than 001b			X	X	Output port (2)
			X				Other than TRBO usage conditions		
	0	1	1	Other than 001b			X	X	$\overline{\text{KI3}}$ input (1)
			X				Other than TRBO usage conditions		
	X	X	0	X	X	X	Refer to **Table 7.23 TRBO Pin Setting**	X	TRBO output (2)
	0	X	1	0	0	1	X	Refer to **Table 7.26 TRCIOC Pin Setting**	TRCIOC input (1)
			X				Other than TRBO usage conditions		
	X	X	1	0	0	1	X	Refer to **Table 7.26 TRCIOC Pin Setting**	TRCIOC output (2)
			X				Other than TRBO usage conditions		

X: 0 or 1

Notes:
1. Pulled up by setting the PU02 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR3 bit in the P1DRR register to 1.

Table 7.10 Port 1_4/$\overline{\text{KI4}}$/TXD0/TRCCLK

Register	PD1	KIEN	U0SR	U0MR			TRBRCSR		TRCCR1			Function
Bit	PD1_4	KI4EN	TXD0SEL0	SMD			TRCCLKSEL		TCK			
				2	1	0	1	0	2	1	0	
Setting Value	0	X	0	X	X	X	X	X	X	X	X	Input port (1)
	1	X	0	X	X	X	X	X	X	X	X	Output port (2)
	0	1	0	X	X	X	X	X	X	X	X	$\overline{\text{KI4}}$ input (1)
	X	X	1	1	0	1	X	X	X	X	X	TXD0 output (2, 3)
						0						
						1						
					1	0						
	0	X	0	X	X	X	0	1	1	0	1	TRCCLK input (1)

X: 0 or 1

Notes:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR4 bit in the P1DRR register to 1.
3. N-channel open-drain output by setting the NCH bit in the U0C0 register to 1.

Table 7.11 Port 1_5/$\overline{\text{KI5}}$/RXD0/TRAIO/$\overline{\text{INT1}}$

Register	PD1	KIEN1	U0SR	TRASR		TRAIOC	TRAMR			INTSR			INTEN	Function
Bit	PD1_5	KI5EN	RXD0SEL0	TRAIOSEL		TOPCR	TMOD			INT1SEL			INT1EN	
				1	0		2	1	0	2	1	0		
Setting Value	0	X	X	Other than 10b		X	X	X	X	X	X	X	X	Input port (1)
	1	X	X	Other than 10b		X	X	X	X	X	X	X	X	Output port (2)
	0	1	X	Other than 010b		X	X	X	X	X	X	X	X	$\overline{\text{KI5}}$ input (1)
	0	X	1	Other than 10b		X	X	X	X	X	X	X	X	RXD0 input (1)
	0	X	X	1	0	0	Other than 000b, 001b			X	X	X	X	TRAIO input (1)
	0	X	X	Other than 10b		X	X	X	X	0	0	1	1	$\overline{\text{INT1}}$ input (1)
	0	X	X	1	0	0	Other than 000b, 001b			0	0	1	1	TRAIO/$\overline{\text{INT1}}$ input (1)
	X	X	X	1	0	0	0	0	1	X	X	X	X	TRAIO pulse output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR5 bit in the P1DRR register to 1.

Table 7.12 Port 1_6/$\overline{\text{KI6}}$/CLK0

Register	PD1	KIEN1	U0SR	U0MR				Function
Bit	PD1_6	KI6EN	CLK0SEL0	SMD			CKDIR	
				2	1	0		
Setting Value	0	X	0	X	X	X	X	Input port (1)
	1	X	0	X	X	X	X	Output port (2)
	0	1	0	X	X	X	X	$\overline{\text{KI6}}$ input (1)
	0	X	1	X	X	X	1	CLK0 (external clock) input (1)
	X	X	1	0	0	1	0	CLK0 (internal clock) output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR6 bit in the P1DRR register to 1.

Table 7.13 Port 1_7/$\overline{\text{KI7}}$/$\overline{\text{INT1}}$/TRAIO

Register	PD1	KIEN1	TRASR		TRAIOC	TRAMR			INTSR			INTEN	Function
Bit	PD1_7	KI7EN	TRAIOSEL		TOPCR	TMOD			INT1SEL			INT1EN	
			1	0		2	1	0	2	1	0		
Setting Value	0	X	Other than 01b		X	X	X	X	X	X	X	X	Input port (1)
	1	X	Other than 01b		X	X	X	X	X	X	X	X	Output port (2)
	0	1	Other than 01b		X	X	X	X	X	X	X	X	$\overline{\text{KI7}}$ input
	0	X	0	1	0	Other than 000b, 001b			X	X	X	X	TRAIO input (1)
	0	X	Other than 01b		X	X	X	X	0	0	0	1	$\overline{\text{INT1}}$ input (1)
	0	X	0	1	0	Other than 000b, 001b			0	0	0	1	TRAIO/$\overline{\text{INT1}}$ input (1)
	X	X	0	1	0	0	0	1	X	X	X	X	TRAIO pulse output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU03 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the P1DRR7 bit in the P1DRR register to 1.

Table 7.14 Port 3_0/TRAO

Register	PD3	TRASR		TRAIOC	Function
Bit	PD3_0	TRAOSEL		TOENA	
		1	0		
Setting Value	0	Other than 01b		X	Input port (1)
	1	Other than 01b		X	Output port (2)
	X	0	1	1	TRAO output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR06 bit in the DRR0 register to 1.

Table 7.15 Port 3_1/TRBO

Register	PD3	TRBRCSR	Timer RB Setting	Function
Bit	PD3_1	TRBOSEL0	—	
Setting Value	0	0	X	Input port (1)
	1	0	X	Output port (2)
	X	1	Refer to **Table 7.23 TRBO Pin Setting**	TRBO output (2)

X: 0 or 1

Notes:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR06 bit in the DRR0 register to 1.

Table 7.16 Port 3_3/$\overline{\text{INT3}}$/TRCCLK/$\overline{\text{SCS}}$

Register	PD3	SSMR2		INTSR		INTEN	TRBRCSR		TRCCR1			Function
Bit	PD3_3	CSS		INT3SEL		INT3EN	TRCCLKSEL		TCK			
		1	0	1	0		1	0	2	1	0	
Setting Value	0	0	0	X	X	X	X	X	X	X	X	Input port (1)
	1	0	0	X	X	X	X	X	X	X	X	Output port (2)
	0	0	0	0	0	1	X	X	X	X	X	$\overline{\text{INT3}}$ input (1)
	0	0	0	X	X	X	1	0	1	0	1	TRCCLK input (1)
	X	0	1	X	X	X	X	X	X	X	X	$\overline{\text{SCS}}$ input (1)
	X	1	0	X	X	X	X	X	X	X	X	$\overline{\text{SCS}}$ output (2, 3)
		1	1									

X: 0 or 1

Notes:
1. Pulled up by setting the PU06 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR06 bit in the DRR0 register to 1.
3. N-channel open-drain output by setting the CSOS bit in the SSMR2 register to 1 (N-channel open-drain output).

Table 7.17 Port 3_4/TRCIOC/SSI

Register	PD3	SSUIICSR	Synchronous Serial Communication Unit (refer to **Table 23.4 Association between Communication Modes and I/O Pins**)		TRCPSR1			Timer RC Setting	Function
Bit	PD3_4	IICSEL	SSI output control	SSI input control	TRCIOCSEL 2	1	0	—	
Setting Value	0	X	0	0	Other than 010b			X	Input port (1)
	1	X	0	0	Other than 010b			X	Output port (2)
	0	X	0	0	0	1	0	Refer to **Table 7.26 TRCIOC Pin Setting**	TRCIOC input (1)
	X	X	0	0	0	1	0	Refer to **Table 7.26 TRCIOC Pin Setting**	TRCIOC output (2)
	X	0	0	1	X	X	X	X	SSI input (1)
	X	0	1	0	X	X	X	X	SSI output (2, 3)

X: 0 or 1

Notes:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR07 bit in the DRR0 register to 1.
3. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output) and setting the BIDE bit in the SSMR2 register to 0 (standard mode).

Table 7.18 Port 3_5/SCL/SSCK/TRCIOD

Register	PD3	SSUIICSR	ICCR1	Synchronous Serial Communication Unit (refer to **Table 23.4 Association between Communication Modes and I/O Pins**)		TRCPSR1			Timer RC Setting	Function
Bit	PD3_5	IICSEL	ICE	SSCK output control	SSCK input control	TRCIODSEL 2	1	0	—	
Setting Value	0	0	X	0	0	Other than 010b			X	Input port (1)
		1	0	X	X					
	1	0	X	0	0	Other than 010b			X	Output port (2)
		1	0	X	X					
	X	1	1	X	X	X	X	X	X	SCL input/output (2)
	X	0	X	0	1	X	X	X	X	SSCK input (1)
	X	0	X	1	0	X	X	X	X	SSCK output (2, 3)
	0	0	X	0	0	0	1	0	Refer to **Table 7.27 TRCIOD Pin Setting**	TRCIOD input (1)
		1	0	X	X					
	X	0	X	0	0	0	1	0	Refer to **Table 7.27 TRCIOD Pin Setting**	TRCIOD output (2)
		1	0	X	X					

X: 0 or 1

Notes:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR07 bit in the DRR0 register to 1.
3. N-channel open-drain output by setting the SCKOS bit in the SSMR2 register to 1 (N-channel open-drain output).

Table 7.19 Port 3_7/SSO/TRAO/SDA

Register	PD3	SSUIICSR	ICCR1	Synchronous Serial Communication Unit (refer to **Table 23.4 Association between Communication Modes and I/O Pins**)		TRASR		TRAIOC	Function
Bit	PD3_7	IICSEL	ICE	SSO output control	SSO input control	TRAOSEL 1	TRAOSEL 0	TOENA	
Setting Value	0	1	0	X	X	Other than 001b			Input port (1)
		0	X	0	0				
	1	1	0	X	X	Other than 001b			Output port (2)
		0	X	0	0				
	X	1	1	X	X	X	X	X	SDA input/output (2)
	X	0	X	0	1	X	X	X	SSO input (1)
	X	0	X	1	0	X	X	X	SSO output (2, 3)
	X	1	0	X	X	0	0	1	TRAO output (2)
		0	X	0	0				

X: 0 or 1

Notes:
1. Pulled up by setting the PU07 bit in the PUR0 register to 1.
2. Output drive capacity high by setting the DRR07 bit in the DRR0 register to 1.
3. N-channel open-drain output by setting the SOOS bit in the SSMR2 register to 1 (N-channel open-drain output).

Table 7.20 Port 4_3/XCIN

Register	PD4	CM0		CM1		Circuit specifications		Function
Bit	PD4_3	CM03	CM04	CM10	CM12	Oscillation buffer	Feedback resistor	
Setting Value	0	X	X	X	X	OFF	OFF	Input port (1)
			0					
	1	X	X	X	X	OFF	OFF	Output port (2)
			0					
	0	0	1	0	0	ON	ON	XCIN-XCOUT oscillation (on-chip feedback resistor enabled) (3)
					1	ON	OFF	XCIN-XCOUT oscillation (on-chip feedback resistor disabled) (3)
		1			0	OFF	ON	XCIN-XCOUT oscillation stop (on-chip feedback resistor enabled)
					1	OFF	OFF	XCIN-XCOUT oscillation stop (on-chip feedback resistor disabled)
	X	X	X	1	X	OFF	OFF	XCIN-XCOUT oscillation stop (STOP mode)

X: 0 or 1

Notes:
1. Pulled up by setting the PU10 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR10 bit in the DRR1 register to 1.
3. When the XCIN clock is used, set the PU10 bit in the PUR1 register to 0 (not pulled up).

Table 7.21 Port 4_4/XCOUT

Register	PD4	CM0		CM1		Circuit specifications		Function
Bit	PD4_4	CM03	CM04	CM10	CM12	Oscillation buffer	Feedback resistor	
Setting Value	0	X	X / 0	X	X	OFF	OFF	Input port (1)
	1	X	X / 0	X	X	OFF	OFF	Output port (2)
	0	0	1	0	0	ON	ON	XCIN-XCOUT oscillation (on-chip feedback resistor enabled) (3, 4)
					1	ON	OFF	XCIN-XCOUT oscillation (on-chip feedback resistor disabled) (3, 4)
		1			0	OFF	ON	XCIN-XCOUT oscillation stop (on-chip feedback resistor enabled)
					1	OFF	OFF	XCIN-XCOUT oscillation stop (on-chip feedback resistor disabled)
	X	X	X	1	X	OFF	OFF	XCIN-XCOUT oscillation stop (STOP mode)

X: 0 or 1

Notes:

1. Pulled up by setting the PU11 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR11 bit in the DRR1 register to 1.
3. Since the XCIN-XCOUT oscillation buffer operates with internal step-down power, the XCOUT output level cannot be used as the CMOS level signal directly.
4. When the XCIN clock is used, set the PU11 bit in the PUR1 register to 0 (not pulled up).

Table 7.22 Port 4_5/$\overline{\text{INT0}}$

Register	PD4	INTEN	Function
Bit	PD4_5	INT0EN	
Setting Value	0	X	Input port (1)
	1	X	Output port (2)
	0	1	$\overline{\text{INT0}}$ input (1)

X: 0 or 1

Notes:

1. Pulled up by setting the PU11 bit in the PUR1 register to 1.
2. Output drive capacity high by setting the DRR11 bit in the DRR1 register to 1.

Table 7.23 TRBO Pin Setting

Register	TRBIOC	TRBMR		Function
Bit	TOCNT	TMOD1	TMOD0	
Setting Value	0	0	1	Programmable waveform generation mode (pulse output)
	1	0	1	Programmable waveform generation mode (programmable output)
	0	1	0	Programmable one-shot generation mode
	0	1	1	Programmable wait one-shot generation mode

Table 7.24 TRCIOA Pin Setting

Register	TRCOER	TRCMR	TRCIOR0			TRCCR2		Function
Bit	EA	PWM2	IOA2	IOA1	IOA0	TCEG1	TCEG0	
Setting Value	0	1	0	0	1	X	X	Timer waveform output (output compare function)
				1	X			
	0	1	1	X	X	X	X	Timer mode (input capture function)
	1							
	1	0	X	X	X	0	1	PWM2 mode TRCTRG input
						1	X	

X: 0 or 1

Table 7.25 TRCIOB Pin Setting

Register	TRCOER	TRCMR		TRCIOR0			Function
Bit	EB	PWM2	PWMB	IOB2	IOB1	IOB0	
Setting Value	0	0	0	X	X	X	PWM2 mode waveform output
	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 7.26 TRCIOC Pin Setting

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	EC	PWM2	PWMC	IOC2	IOC1	IOC0	
Setting Value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

Table 7.27 TRCIOD Pin Setting

Register	TRCOER	TRCMR		TRCIOR1			Function
Bit	ED	PWM2	PWMD	IOD2	IOD1	IOD0	
Setting Value	0	1	1	X	X	X	PWM mode waveform output
	0	1	0	0	0	1	Timer waveform output (output compare function)
					1	X	
	0	1	0	1	X	X	Timer mode (input capture function)
	1						

X: 0 or 1

7.6 Unassigned Pin Handling

Table 7.28 lists Unassigned Pin Handling.

Table 7.28 Unassigned Pin Handling

Pin Name	Connection
Ports P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	• After setting to input mode, connect each pin to VSS via a resistor (pull-down) or connect each pin to VCC via a resistor (pull-up). (2) • After setting to output mode, leave these pins open. (1, 2)
$\overline{\text{RESET}}$ (3)	Connect to VCC via a pull-up resistor (2)

Notes:
1. If these ports are set to output mode and left open, they remain in input mode until they are switched to output mode by a program. The voltage level of these pins may be undefined and the power current may increase while the ports remain in input mode.
   The content of the direction registers may change due to noise or program runaway caused by noise. In order to enhance program reliability, the program should periodically repeat the setting of the direction registers.
2. Connect these unassigned pins to the MCU using the shortest wire length (2 cm or less) possible.
3. When the power-on reset function is in use.

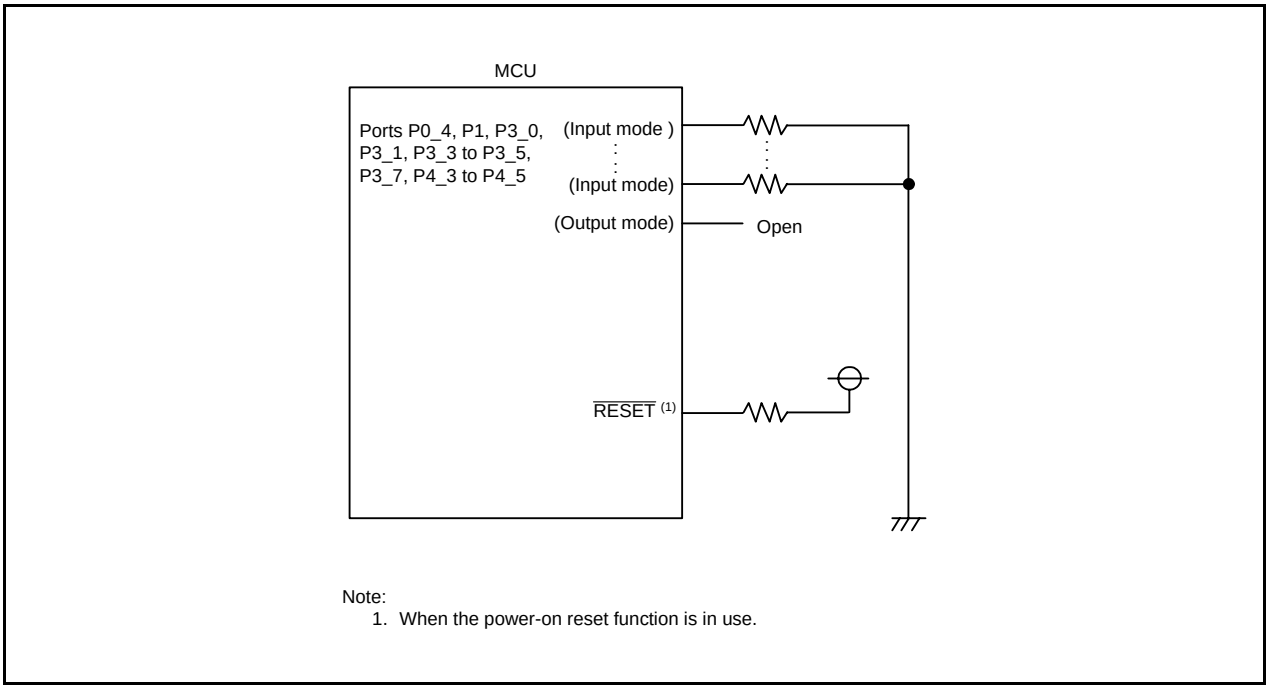


Figure 7.11 Unassigned Pin Handling

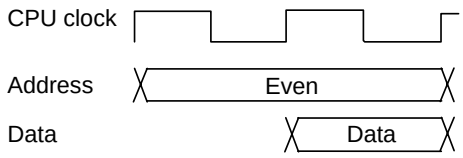
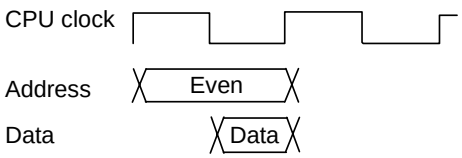
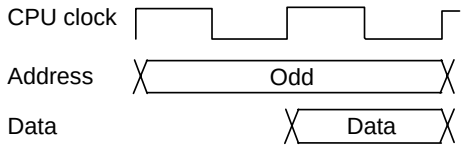
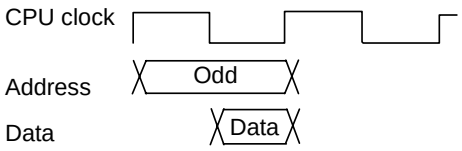
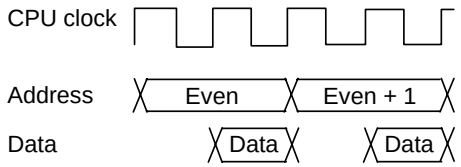
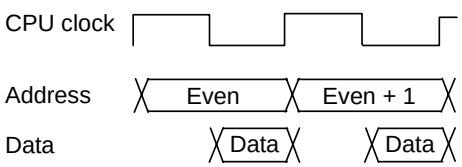
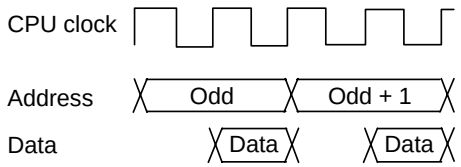
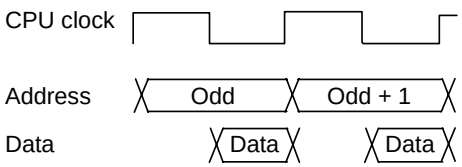
8. Bus

The bus cycles differ when accessing ROM, RAM, DTC vector area, DTC control data and when accessing SFR. Table 8.1 lists Bus Cycles by Access Area of R8C/3MQ Group.
ROM, RAM, DTC vector area, DTC control data and SFR are connected to the CPU by an 8-bit bus. When accessing in word (16-bit) units, these areas are accessed twice in 8-bit units.
Table 8.2 shows Access Units and Bus Operations.

Table 8.1 Bus Cycles by Access Area of R8C/3MQ Group

Access Area	Bus Cycle
SFR, Data flash	2 cycles of CPU clock
Program ROM, RAM	1 cycle of CPU clock

Table 8.2 Access Units and Bus Operations

Area	SFR, Data flash	ROM (program ROM), RAM, DTC vector area, DTC control data
Even address Byte access		
Odd address Byte access		
Even address Word access		
Odd address Word access		

However, only the following SFRs are connected with the 16-bit bus:

Interrupts: Each interrupt control register
Timer RC: Registers TRC, TRCGRA, TRCGRB, TRCGRC, and TRCGRD
SSU: Registers SSTDR, SSTDRH, SSRDR, and SSRDRH
Address match interrupt: Registers RMAD0, AIER0, RMAD1, and AIER1
Therefore, they are accessed once in 16-bit units. The bus operation is the same as “Area: SFR, Data flash, Even address Byte Access” in **Table 8.2 Access Units and Bus Operations**, and 16-bit data is accessed at a time.

9. Clock Generation Circuit

The following four circuits are incorporated in the clock generation circuit:
- XIN clock oscillation circuit
- XCIN clock oscillation circuit
- Low-speed on-chip oscillator
- Low-speed on-chip oscillator for watchdog timer

9.1 Overview

Table 9.1 lists the Specification Overview of Clock Generation Circuit. Figure 9.1 shows a Clock Generation Circuit. Figure 9.2 shows a Peripheral Function Clock.

Table 9.1 Specification Overview of Clock Generation Circuit

Item	XIN Clock Oscillation Circuit	XCIN Clock Oscillation Circuit	Low-Speed On-Chip Oscillator	Low-Speed On-Chip Oscillator for Watchdog Timer
Applications	• CPU clock source • Peripheral function clock source • Transceiver reference clock source	• CPU clock source • Peripheral function clock source	• CPU clock source • Peripheral function clock source • CPU and peripheral function clock source when XIN clock stops oscillating	Watchdog timer clock source
Clock frequency	16 MHz (fixed) (4)	32.768 kHz	Approx. 125 kHz	Approx. 125 kHz
Connectable oscillator	Crystal oscillator	Crystal oscillator	—	—
Oscillator connect pins	XIN, XOUT	XCIN, XCOUT (1)	—	—
Oscillation stop, restart function	Usable	Usable	Usable	Usable
Oscillator status after reset	Stop	Stop	Oscillate	Stop (2) Oscillate (3)
Others	—	On-chip feedback resistor Rf (connected/not connected selectable)	—	—

Notes:
1. These pins can be used as P4_3 and P4_4 when using the XIN clock oscillation circuit or on-chip oscillator clock as the CPU clock while the XCIN clock oscillation circuit is not used.
2. This applies when the CSPROINI bit in the OFS register is set to 1 (count source protection mode disabled after reset).
3. This applies when the CSPROINI bit in the OFS register is set to 0 (count source protection mode enabled after reset).
4. The XIN clock is fixed at 16 MHz because it is also used as the reference clock for the transceiver. A crystal oscillator should be selected to ensure the frequency tolerance is ±40 ppm or less.

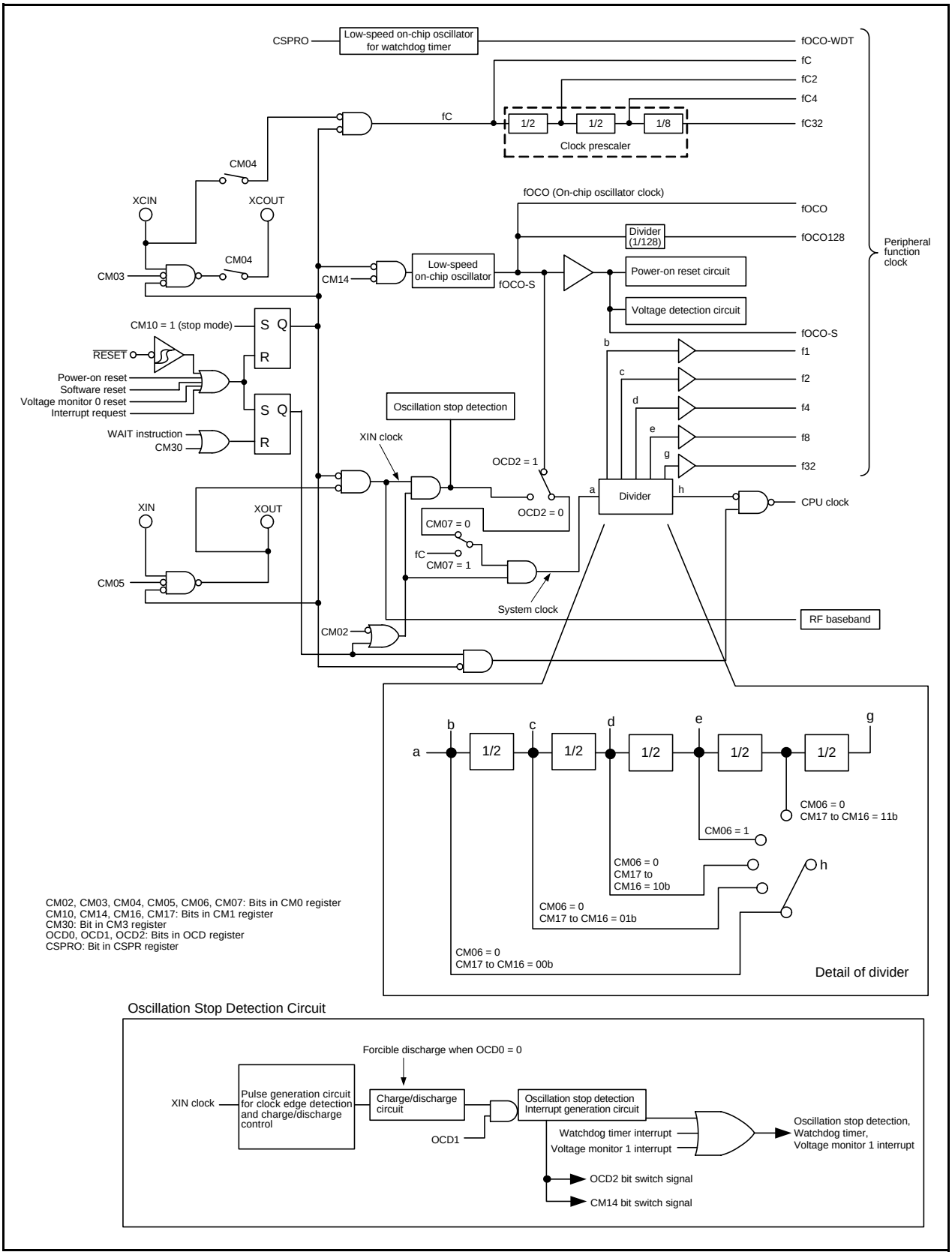


Figure 9.1 Clock Generation Circuit

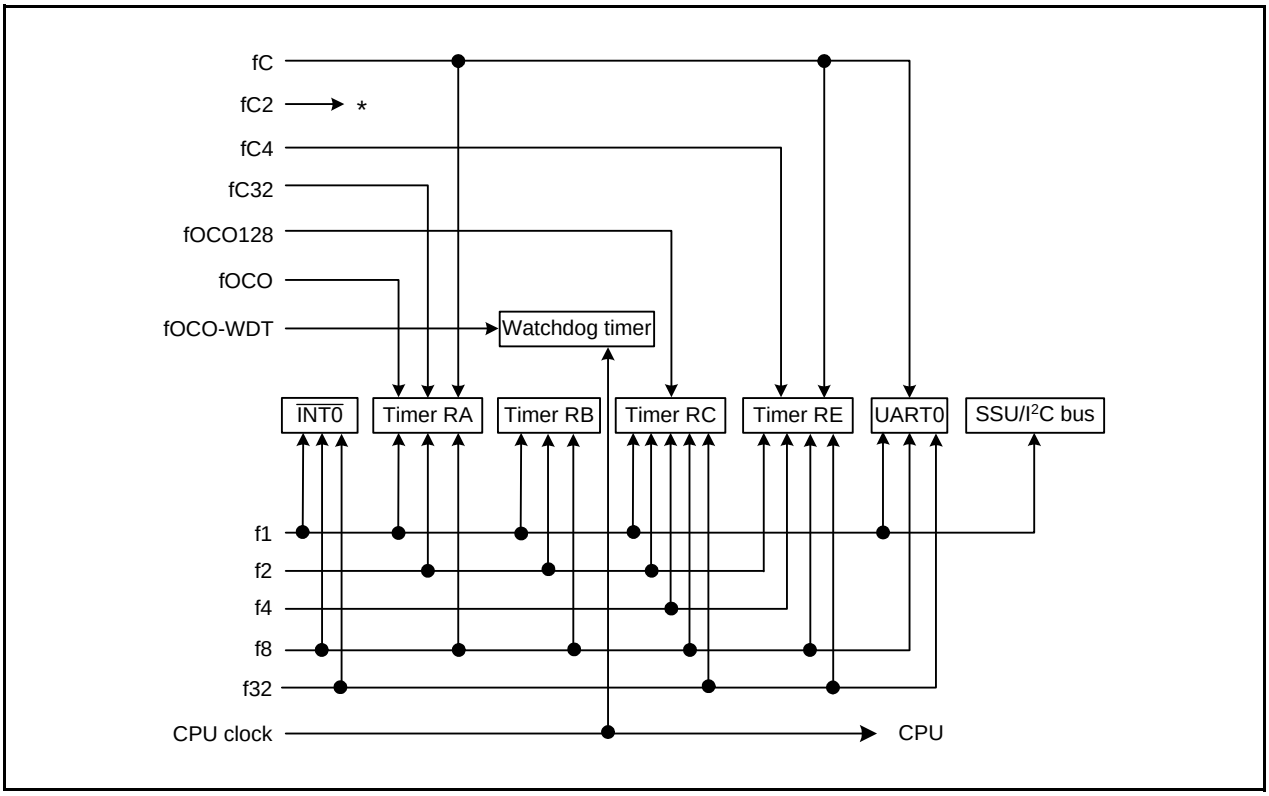


Figure 9.2 Peripheral Function Clock

9.2 Registers

9.2.1 System Clock Control Register 0 (CM0)

Address 0006h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM07	CM06	CM05	CM04	CM03	CM02	—	—
After Reset	0	0	1	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	CM02	Wait mode peripheral function clock stop bit	0: Peripheral function clock does not stop in wait mode 1: Peripheral function clock stops in wait mode	R/W
b3	CM03	XCIN clock stop bit	0: XCIN clock oscillates 1: XCIN clock stops	R/W
b4	CM04	Port/XCIN-XCOUT switch bit (3)	0: I/O ports P4_3 and P4_4 1: XCIN-XCOUT pin (4)	R/W
b5	CM05	XIN clock (XIN-XOUT) stop bit (1)	0: XIN clock oscillates 1: XIN clock stops	R/W
b6	CM06	CPU clock division select bit 0 (2)	0: Bits CM16 and CM17 in CM1 register enabled 1: Divide-by-8 mode	R/W
b7	CM07	XIN, XCIN clock select bit (5)	0: XIN clock 1: XCIN clock	R/W

Notes:

1. The CM05 bit can be used to stop the XIN clock when the system clock is other than the XIN clock. This bit cannot be used to detect whether the XIN clock has stopped. To stop the XIN clock, set the bits in the following order:
   (1) Set bits OCD1 to OCD0 in the OCD register to 00b.
   (2) Set the OCD2 bit to 1 (on-chip oscillator clock selected).
2. When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode).
3. The CM04 bit can be set to 1 by a program but cannot be set to 0.
4. To use the XCIN clock, set the CM04 bit to 1. Also, set ports P4_3 and P4_4 as input ports without pull-up.
5. Set the CM07 bit to 1 (XCIN clock) from 0 after setting the CM04 bit to 1 (XCIN-XCOUT pin) and allowing XCIN clock oscillation to stabilize.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM0 register.

9.2.2 System Clock Control Register 1 (CM1)

Address 0007h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM17	CM16	—	CM14	—	CM12	CM11	CM10
After Reset	0	0	1	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM10	All clock stop control bit (2, 5)	0: Clock oscillates 1: All clocks stop (stop mode)	R/W
b1	CM11	XIN-XOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b2	CM12	XCIN-XCOUT on-chip feedback resistor select bit	0: On-chip feedback resistor enabled 1: On-chip feedback resistor disabled	R/W
b3	—	Reserved bit	Set to 1.	R/W
b4	CM14	Low-speed on-chip oscillator stop bit (3, 4)	0: Low-speed on-chip oscillator on 1: Low-speed on-chip oscillator off	R/W
b5	—	Reserved bit	Set to 1.	R/W
b6	CM16	CPU clock division select bit 1 (1)	b7 b6 0 0: No division mode 0 1: Divide-by-2 mode 1 0: Divide-by-4 mode 1 1: Divide-by-16 mode	R/W
b7	CM17			R/W

Notes:
1. When the CM06 bit is set to 0 (bits CM16 and CM17 enabled), bits CM16 and CM17 are enabled.
2. If the CM10 bit is set to 1 (stop mode), the on-chip feedback resistor is disabled.
3. When the OCD2 bit is set to 0 (XIN clock selected), the CM14 bit can be set to 1 (low-speed on-chip oscillator off). When the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on). It remains unchanged even if 1 is written to it.
4. To use the voltage monitor 1 interrupt (when the digital filter is used), set the CM14 bit to 0 (low-speed on-chip oscillator on).
5. Do not set the CM10 bit to 1 (stop mode) when the VCA20 bit in the VCA2 register to 1 (low consumption enabled).

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM1 register.

9.2.3 System Clock Control Register 3 (CM3)

Address 0009h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CM37	CM36	CM35	—	—	—	—	CM30
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CM30	Wait control bit (1)	0: Other than wait mode 1: MCU enters wait mode	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	CM35	CPU clock division when exiting wait mode select bit (2)	0: Following settings are enabled: CM06 bit in CM0 register Bits CM16 and CM17 in CM1 register 1: No division	R/W
b6	CM36	System clock when exiting wait mode or stop mode select bit	b7 b6 0 0: MCU exits with the CPU clock immediately before entering wait or stop mode. 0 1: Do not set. 1 0: Do not set. 1 1: XIN clock selected (3)	R/W
b7	CM37			R/W

Notes:
1. When the MCU exits wait mode by a peripheral function interrupt, the CM30 bit is set to 0 (other than wait mode).
2. Set the CM35 bit to 0 in stop mode. When the MCU enters wait mode, if the CM35 bit is set to 1 (no division), the CM06 bit in the CM0 register is set to 0 (bits CM16 and CM17 enabled) and bits CM17 and CM16 in the CM1 register are set to 00b (no division mode).
3. When bits CM37 and CM36 are set to 11b (XIN clock selected), the following will be set when the MCU exits wait mode or stop mode.
   • CM05 bit in CM0 register = 0 (XIN clock oscillates)
   • OCD2 bit in OCD register = 0 (XIN clock selected)
   When the MCU enters wait mode while the CM05 bit in the CM0 register is 1 (XIN clock stops), if the XIN clock is selected as the CPU clock when exiting wait mode, set the CM06 bit to 1 (divide-by-8 mode) and the CM35 bit to 0.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the CM3 register.

CM30 bit (Wait Control Bit)

When the CM30 bit is set to 1 (MCU enters wait mode), the CPU clock stops (wait mode). Since the XIN clock, XCIN clock, and the on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating. To set the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).

The MCU exits wait mode by a reset or peripheral function interrupt. When the MCU exits wait mode by a peripheral function interrupt, it resumes executing the instruction immediately after the instruction to set the CM30 bit to 1.

When the MCU enters wait mode with the WAIT instruction, make sure to set the I flag to 1 (maskable interrupt enabled). With this setting, interrupt handling is performed by the CPU when the MCU exits wait mode.

9.2.4 Oscillation Stop Detection Register (OCD)

Address 000Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	OCD3	OCD2	OCD1	OCD0
After Reset	0	0	0	0	0	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	OCD0	Oscillation stop detection enable bit (6)	0: Oscillation stop detection function disabled (1) 1: Oscillation stop detection function enabled	R/W
b1	OCD1	Oscillation stop detection interrupt enable bit	0: Disabled (1) 1: Enabled	R/W
b2	OCD2	System clock select bit (3)	0: XIN clock selected (6) 1: On-chip oscillator clock selected (2)	R/W
b3	OCD3	Clock monitor bit (4, 5)	0: XIN clock oscillates 1: XIN clock stops	R
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

Notes:
1. Set bits OCD1 to OCD0 to 00b before the MCU enters stop mode, or low-speed on-chip oscillator mode (XIN clock stops).
2. If the OCD2 bit is set to 1 (on-chip oscillator clock selected), the CM14 bit is set to 0 (low-speed on-chip oscillator on).
3. The OCD2 bit is automatically set to 1 (on-chip oscillator clock selected) if XIN clock oscillation stop is detected while bits OCD1 to OCD0 are set to 11b. If the OCD3 bit is set to 1 (XIN clock stops), the OCD2 bit remains unchanged even when set to 0 (XIN clock selected).
4. The OCD3 bit is enabled when the OCD0 bit is set to 1 (oscillation stop detection function enabled). In addition, this bit cannot be used to confirm whether the XIN clock oscillation is stable.
5. The OCD3 bit remains 0 (XIN clock oscillates) if bits OCD1 to OCD0 are set to 00b.
6. Refer to **Figure 9.11 Procedure for Switching to XIN Clock when XIN Clock Re-Oscillates after Oscillation Stop is Detected** for the switching procedure when the XIN clock re-oscillates after detecting oscillation stop.

Set the PRC0 bit in the PRCR register to 1 (write enabled) before rewriting the OCD register.

9.2.5 Clock Prescaler Reset Flag (CPSRF)

Address 0028h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CPSR	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CPSR	Clock prescaler reset flag	Setting this bit to 1 initializes the clock prescaler. (When read, the content is 0.)	R/W

9.2.6 Voltage Detect Register 2 (VCA2)

Address 0034h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	VCA26	VCA25	—	—	—	—	VCA20
After Reset	0	0	0	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 1.

After Reset	0	0	1	0	0	0	0	0

The above applies when the LVDAS bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	VCA20	Internal power low consumption enable bit (1)	0: Low consumption disabled 1: Low consumption enabled (2)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	VCA25	Voltage detection 0 enable bit (3)	0: Voltage detection 0 circuit disabled 1: Voltage detection 0 circuit enabled	R/W
b6	VCA26	Voltage detection 1 enable bit (4)	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled	R/W
b7	—	Reserved bit	Set to 0.	R/W

Notes:
1. Use the VCA20 bit only when the MCU enters wait mode. To set the VCA20 bit, follow the procedure shown in **9.7.2.2 Reducing Internal Power Consumption Using VCA20 Bit**.
2. When the VCA20 bit is set to 1 (low consumption enabled), do not set the CM10 bit in the CM1 register to 1 (stop mode).
3. When writing to the VCA25 bit, set a value after reset.
4. To use the voltage detection 1 interrupt or the VW1C3 bit in the VW1C register, set the VCA26 bit to 1. After the VCA26 bit is set to 1 from 0, allow td(E-A) to elapse before the voltage detection 1 circuit starts operation.

Set the PRC3 bit in the PRCR register to 1 (write enabled) before rewriting the VCA2 register.

9.2.7 I/O Function Pin Select Register (PINSR)

Address 018Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SDADLY1	SDADLY0	IICTCHALF	IICTCTWI	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i =0, 1, 3, 4) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read. When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read. 1: The I/O port input function reads the pin input level regardless of the PDi register	R/W
b4	IICTCTWI	I^2C double transfer rate select bit (1)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is twice the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b5	IICTCHALF	I^2C half transfer rate select bit (1)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is half the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b6	SDADLY0	SDA digital delay select bit	b7 b6 0 0: Digital delay of 3 × f1 cycles 0 1: Digital delay of 11 × f1 cycles 1 0: Digital delay of 19 × f1 cycles 1 1: Do not set.	R/W
b7	SDADLY1			R/W

Note:
1. Do not set both the IICTCTWI and IICTCHALF bits to 1 when the I^2C bus function is used. Set these bits to 0 when the SSU function is used.

IOINSEL Bit (I/O port input function select bit)

The IOINSEL bit is used to select the pin level of an I/O port when the PDi_j (j = 0 to 7) bit in the PDi (i = 0, 1, 3, 4) register is set to 1 (output mode). When this bit is set to 1, the I/O port input function reads the pin input level regardless of the PDi register.

Table 9.2 lists I/O Port Values Read by Using IOINSEL Bit. The IOINSEL bit can be used to change the input function of all I/O ports.

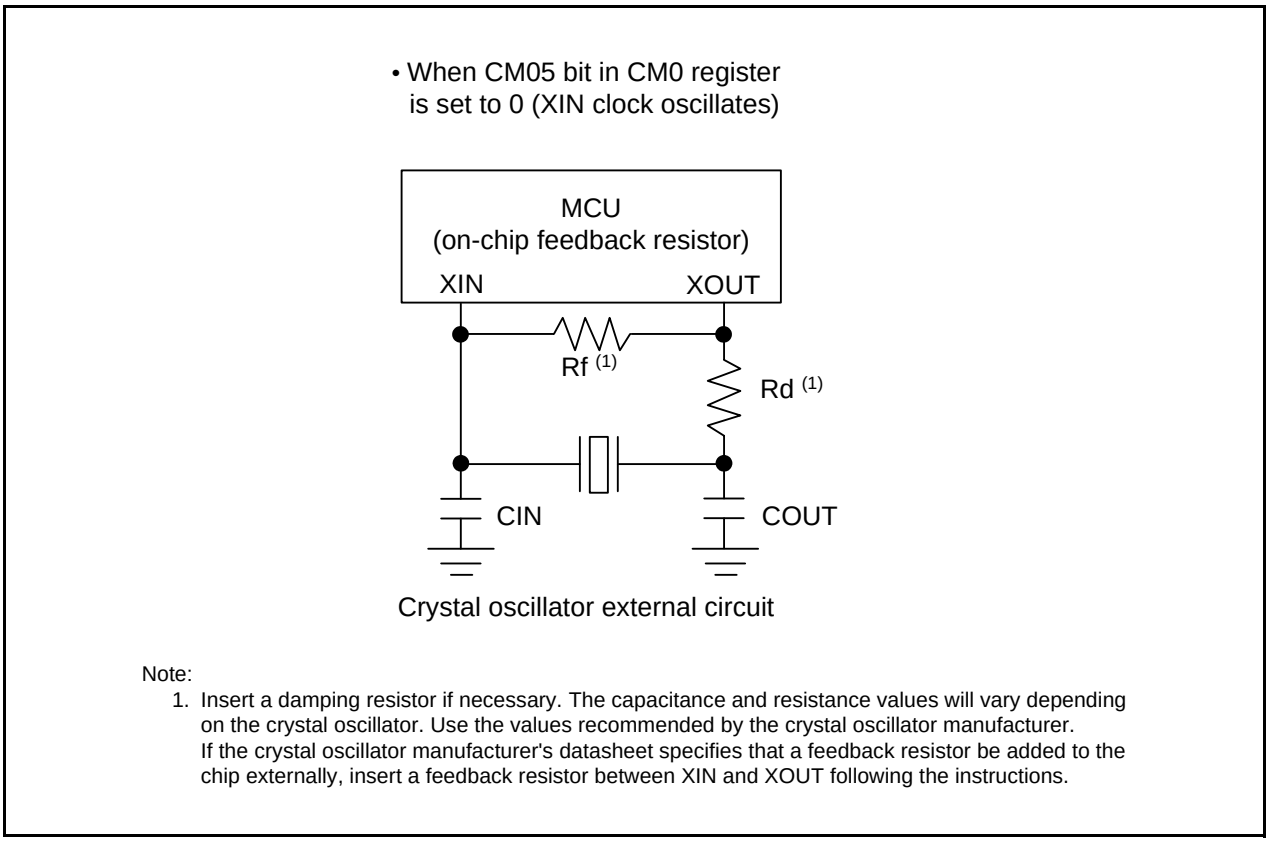
Table 9.2 I/O Port Values Read by Using IOINSEL Bit

PDi_j bit in PDi register	0 (input mode)		1 (output mode)	
IOINSEL bit	0	1	0	1
I/O port values read	Pin input level		Port latch value	Pin input level

The clocks generated by the clock generation circuits are described below.

9.3 XIN Clock

The XIN clock is supplied by the XIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XIN clock oscillation circuit is configured by connecting a resonator between pins XIN and XOUT. The XIN clock oscillation circuit includes an on-chip feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip.
Figure 9.3 shows Examples of XIN Clock Connection Circuit.
During and after a reset, the XIN clock stops.
The XIN clock starts oscillating when the CM05 bit in the CM0 register is set to 0 (XIN clock oscillates). After the XIN clock oscillation stabilizes, the XIN clock is used as the CPU clock source when the OCD2 bit in the OCD register is set to 0 (XIN clock selected).
The power consumption can be reduced by setting the CM05 bit in the CM0 register to 1 (XIN clock stops) if the OCD2 bit is set to 1 (on-chip oscillator clock selected).
In stop mode, all clocks including the XIN clock stop. Refer to **9.7 Power Control** for details.



Note:
1. Insert a damping resistor if necessary. The capacitance and resistance values will vary depending on the crystal oscillator. Use the values recommended by the crystal oscillator manufacturer. If the crystal oscillator manufacturer's datasheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XIN and XOUT following the instructions.

Figure 9.3 Examples of XIN Clock Connection Circuit

9.4 On-Chip Oscillator Clock

The on-chip oscillator clock is supplied by the low-speed on-chip oscillator.

9.4.1 Low-Speed On-Chip Oscillator Clock

The clock generated by the low-speed on-chip oscillator is used as the clock source for the CPU clock, peripheral function clock, fOCO, fOCO-S, and fOCO128.

After a reset, the on-chip oscillator clock generated by the low-speed on-chip oscillator divided by 1 (no division) is selected as the CPU clock.

If the XIN clock stops oscillating when bits OCD1 to OCD0 in the OCD register are set to 11b, the low-speed on-chip oscillator automatically starts operating and supplies the necessary clock for the MCU.

The frequency of the low-speed on-chip oscillator varies depending on the supply voltage and the operating ambient temperature. Application products must be designed with sufficient margin to allow for frequency changes.

9.5 XCIN Clock

The XCIN clock is supplied by the XCIN clock oscillation circuit. This clock is used as the clock source for the CPU and peripheral function clocks. The XCIN clock oscillation circuit is configured by connecting a resonator between the XCIN and XCOUT pins. The XCIN clock oscillation circuit includes an on-chip a feedback resistor, which is disconnected from the oscillation circuit in stop mode in order to reduce the amount of power consumed by the chip.

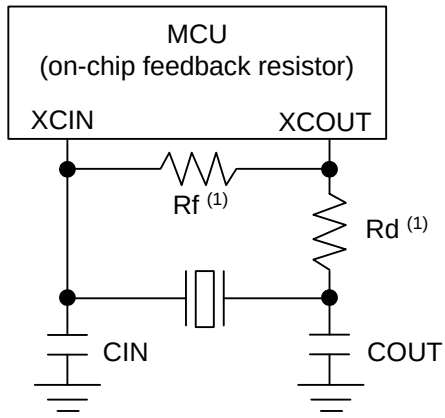
Figure 9.4 shows Examples of XCIN Clock Connection Circuits.

During and after a reset, the XCIN clock stops.

When the CM04 bit in the CM0 register is set to 1 (XCIN-XCOUT pin) and the CM03 bit in the CM0 register is set to 0 (XCIN clock oscillates), the XCIN clock starts oscillating. After the XCIN clock oscillation stabilizes, the XCIN clock is used as the CPU clock source when the CM07 bit in the CM0 register is set to 1 (XCIN clock).

This MCU has an on-chip feedback resistor, which can be disabled/enabled by the CM12 bit in the CM1 register. In stop mode, all clocks including the XCIN clock stop. Refer to **9.7 Power Control** for details.

When CM03 bit in CM0 register is set to 0 (XCIN clock oscillates) and CM04 bit is set to 1 (XCIN-XCOUT pin)



External crystal oscillator circuit

Note:
1. Insert a damping resistor and feedback resistor if required. The resistance will vary depending on the oscillator and the oscillation drive capacity setting. Use the value recommended by the oscillator manufacturer.
   If the oscillator manufacturer's datasheet specifies that a feedback resistor be added to the chip externally, insert a feedback resistor between XCIN and XCOUT following the instructions.

Figure 9.4 Examples of XCIN Clock Connection Circuits

9.6 CPU Clock and Peripheral Function Clock

There are a CPU clock to operate the CPU and a peripheral function clock to operate the peripheral functions (refer to **Figure 9.1 Clock Generation Circuit**).

9.6.1 System Clock

The system clock is the clock source for the CPU and peripheral function clocks. The XIN clock, the XCIN clock, or the on-chip oscillator clock can be selected.

9.6.2 CPU Clock

The CPU clock is an operating clock for the CPU and the watchdog timer.
The system clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. Use the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register to select the value of the division.
Also, use the XCIN clock while the XCIN clock oscillation stabilizes.
After a reset, the low-speed on-chip oscillator clock divided by 1 (no division) is used as the CPU clock.
When the MCU enters stop mode, the CM06 bit is set to 1 (divide-by-8 mode). To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 in CM0 register and bits CM16 and CM17 in CM1 register enabled).

9.6.3 Peripheral Function Clock (f1, f2, f4, f8, and f32)

The peripheral function clock is an operating clock for the peripheral functions.
The fi (i = 1, 2, 4, 8, and 32) clock is generated by the system clock divided by i. It is used for timers RA, RB, RC, RE, and the serial interface.
If the MCU enters wait mode after the CM02 bit in the CM0 register is set to 1 (peripheral function clock stops in wait mode), the fi clock stops.

9.6.4 fOCO

fOCO is an operating clock for the peripheral functions.
This clock runs at the same frequency as the on-chip oscillator clock and can be used as the source for timer RA.
In wait mode, the fOCO clock does not stop.

9.6.5 fOCO-S

fOCO-S is an operating clock for the voltage detection circuit.
This clock is generated by the low-speed on-chip oscillator and supplied by setting the CM14 bit to 0 (low-speed on-chip oscillator on).
In wait mode, the fOCO-S clock does not stop.

9.6.6 fOCO128

fOCO128 is a clock generated by dividing fOCO-S by 128.
fOCO128 is configured as the capture signal used in the TRCGRA register for timer RC.

9.6.7 fC, fC2, fC4, and fC32

fC, fC2, fC4, and fC32 are used for timers RA, RE, and the serial interface.
Use theses clocks while the XCIN clock oscillation stabilizes.

9.6.8 fOCO-WDT

fOCO-WDT is an operating clock for the watchdog timer.
This clock is generated by the low-speed on-chip oscillator for the watchdog timer and supplied by setting the CSPRO bit in the CSPR register to 1 (count source protect mode enabled).
In count source protection mode for the watchdog timer, the fOCO-WDT clock does not stop.

9.7 Power Control

There are three power control modes. All modes other than wait mode and stop mode are referred to as standard operating mode.

9.7.1 Standard Operating Mode

Standard operating mode is further separated into three modes.
In standard operating mode, the CPU and peripheral function clocks are supplied to operate the CPU and the peripheral functions. Power consumption control is enabled by controlling the CPU clock frequency. The higher the CPU clock frequency, the more processing power increases. The lower the CPU clock frequency, the more power consumption decreases. If unnecessary oscillator circuits stop, power consumption is further reduced.
Before the clock sources for the CPU clock can be switched over, the new clock source needs to be oscillating and stable. Allow sufficient wait time in a program until oscillation stabilizes before switching the clock.

Table 9.3 Settings and Modes of Clock Associated Bits

Modes		OCD Register	CM1 Register		CM0 Register				
		OCD2	CM17, CM16	CM14	CM07	CM06	CM05	CM04	CM03
High-speed clock mode	No division	0	00b	—	0	0	0	—	—
	Divide-by-2	0	01b	—	0	0	0	—	—
	Divide-by-4	0	10b	—	0	0	0	—	—
	Divide-by-8	0	—	—	0	1	0	—	—
	Divide-by-16	0	11b	—	0	0	0	—	—
Low-speed clock mode	No division	—	00b	—	1	0	—	1	0
	Divide-by-2	—	01b	—	1	0	—	1	0
	Divide-by-4	—	10b	—	1	0	—	1	0
	Divide-by-8	—	—	—	1	1	—	1	0
	Divide-by-16	—	11b	—	1	0	—	1	0
Low-speed on-chip oscillator mode	No division	1	00b	0	0	0	—	—	—
	Divide-by-2	1	01b	0	0	0	—	—	—
	Divide-by-4	1	10b	0	0	0	—	—	—
	Divide-by-8	1	—	0	0	1	—	—	—
	Divide-by-16	1	11b	0	0	0	—	—	—

—: Indicates that either 0 or 1 can be set.

9.7.1.1 High-Speed Clock Mode

The XIN clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock. If the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO can be used for timer RA.
If the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.

9.7.1.2 Low-Speed Clock Mode

The XCIN clock divided by 1 (no division), 2, 4, 8, or 16 is used as the CPU clock.
In this mode, low consumption operation is enabled by stopping the XIN clock, and by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled). When the CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8, low-current-consumption read mode can be used. However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
If the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.
To enter wait mode from low-speed clock mode, lower consumption current in wait mode is enabled by setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled).
To reduce the power consumption, refer to **27. Reducing Power Consumption**.

9.7.1.3 Low-Speed On-Chip Oscillator Mode

If the CM14 bit in the CM1 register is set to 0 (low-speed on-chip oscillator on), the low-speed on-chip oscillator is used as the on-chip oscillator clock. At this time, the on-chip oscillator clock divided by 1 (no division), 2, 4, 8 or 16 is used as the CPU clock. The on-chip oscillator clock is also the clock source for the peripheral function clocks.
Also, if the CM14 bit is set to 0 (low-speed on-chip oscillator on), fOCO-S can be used for the voltage detection circuit.
In this mode, low consumption operation is enabled by stopping the XIN clock, and by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled). When the CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16, low-current-consumption read mode can be used. After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
To enter wait mode from low-speed on-chip oscillator mode, lower consumption current in wait mode is enabled by setting the VCA20 bit in the VCA2 register to 1 (internal power low consumption enabled).
To reduce the power consumption, refer to **27. Reducing Power Consumption**.

9.7.2 Wait Mode

Since the CPU clock stops in wait mode, the CPU operating with the CPU clock and the watchdog timer when count source protection mode is disabled stop. Since the XIN clock, XCIN clock, and on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating.

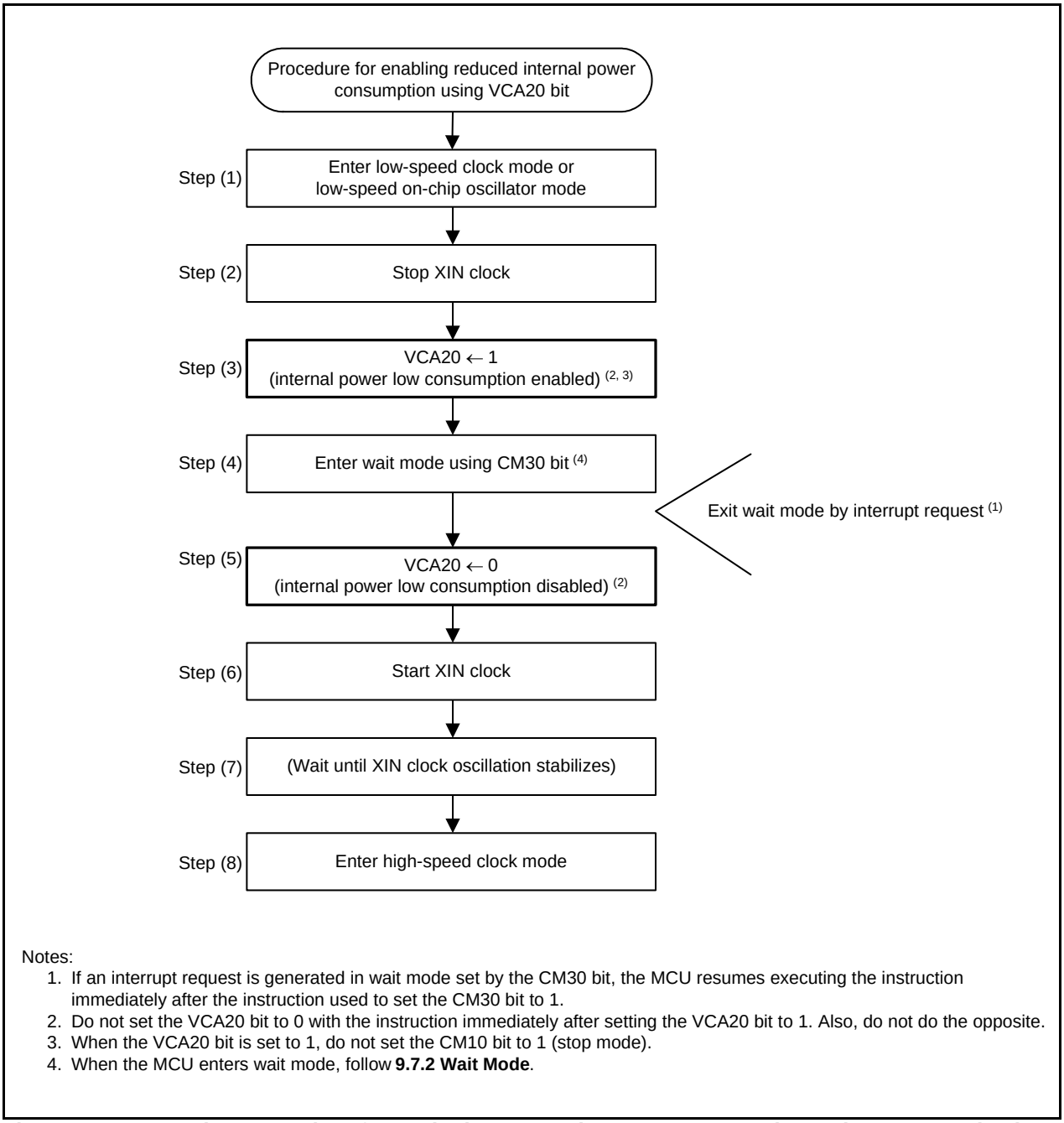
9.7.2.1 Peripheral Function Clock Stop Function

If the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the f1, f2, f4, f8, and f32 clocks stop in wait mode. This reduces power consumption.

9.7.2.2 Reducing Internal Power Consumption Using VCA20 Bit

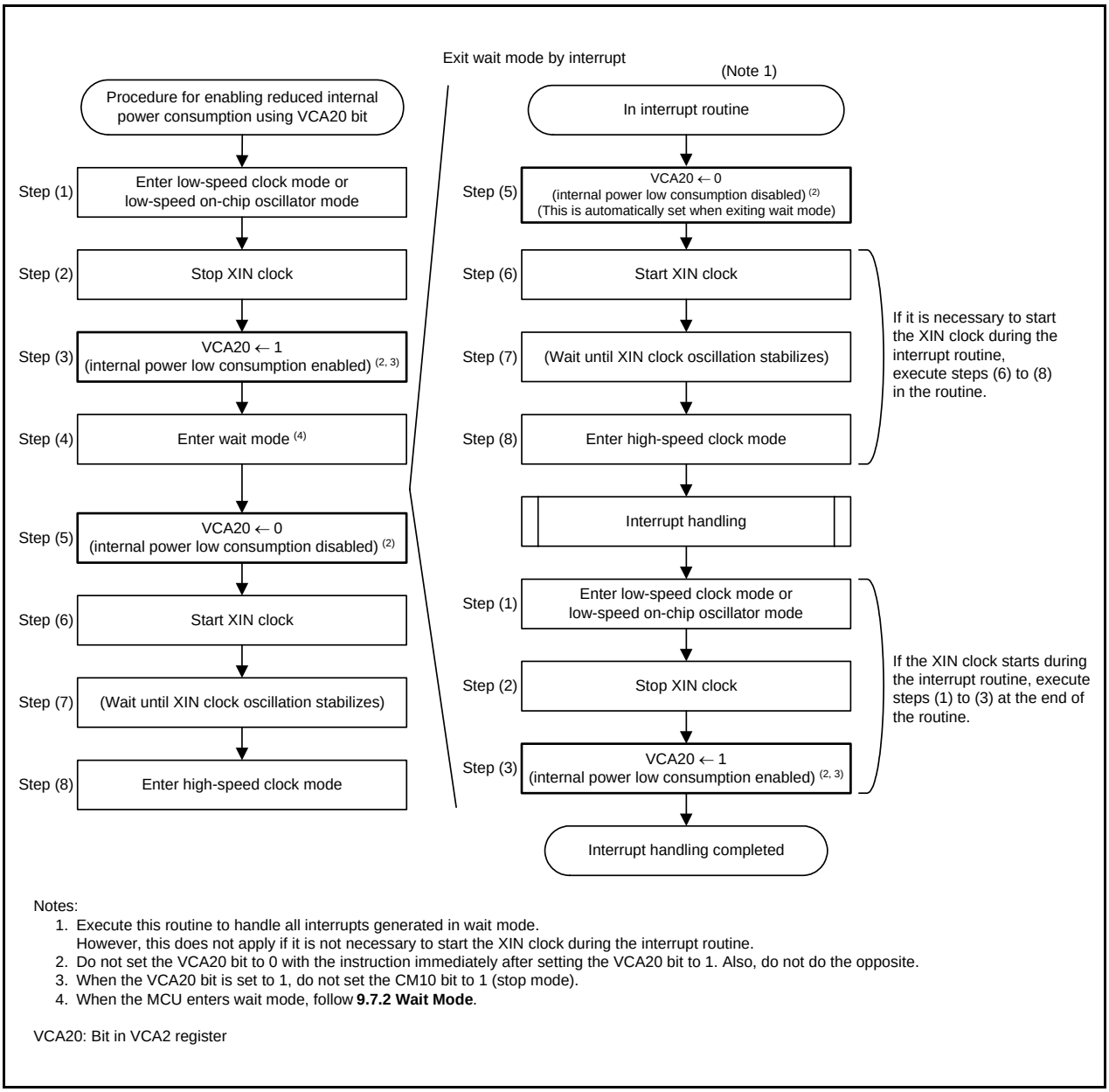
The electric current in wait mode can be further reduced by setting the VCA20 bit in the VCA2 register to 1 (low consumption enabled). Set the VCA20 bit to 1 in low-speed clock mode or low-speed on-chip oscillator mode before entering wait mode.

The setting procedure for reducing internal power consumption using the VCA20 bit differs when the CM30 bit in the CM3 register is set to 1 (MCU enters wait mode) to enter wait mode and when the WAIT instruction is executed to enter wait mode. Figure 9.5 shows the Setting Procedure for Reducing Internal Power Consumption Using VCA20 Bit when CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode) to Enter Wait Mode. Figure 9.6 shows the Setting Procedure for Reducing Internal Power Consumption Using VCA20 Bit when WAIT Instruction is Executed to Enter Wait Mode.



Notes:
1. If an interrupt request is generated in wait mode set by the CM30 bit, the MCU resumes executing the instruction immediately after the instruction used to set the CM30 bit to 1.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When the MCU enters wait mode, follow **9.7.2 Wait Mode**.

Figure 9.5 Setting Procedure for Reducing Internal Power Consumption Using VCA20 Bit when CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode) to Enter Wait Mode



Notes:
1. Execute this routine to handle all interrupts generated in wait mode.
   However, this does not apply if it is not necessary to start the XIN clock during the interrupt routine.
2. Do not set the VCA20 bit to 0 with the instruction immediately after setting the VCA20 bit to 1. Also, do not do the opposite.
3. When the VCA20 bit is set to 1, do not set the CM10 bit to 1 (stop mode).
4. When the MCU enters wait mode, follow **9.7.2 Wait Mode**.

VCA20: Bit in VCA2 register

Figure 9.6 Setting Procedure for Reducing Internal Power Consumption Using VCA20 Bit when WAIT Instruction is Executed to Enter Wait Mode

9.7.2.3 Entering Wait Mode

The MCU enters wait mode by executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).
When the OCD2 bit in the OCD register is set to 1 (on-chip oscillator selected as system clock), set the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before executing the WAIT instruction or setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode).
If the MCU enters wait mode while the OCD1 bit is set to 1 (oscillation stop detection interrupt enabled), current consumption is not reduced because the CPU clock does not stop.
When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the FMR27 bit to 0 (low-current-consumption read mode disabled) before entering the mode.
Do not enter wait mode while the FMR01 bit is 1 (CPU rewrite mode enabled) or the FMR27 bit is 1 (low-current-consumption read mode enabled).
To enter wait mode by setting the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled). To enter wait mode using the WAIT instruction, set the I flag to 1 (maskable interrupt enabled).

9.7.2.4 Pin Status in Wait Mode

The I/O ports retain the status immediately before the MCU enters wait mode.

9.7.2.5 Exiting Wait Mode

The MCU exits wait mode by a reset or peripheral function interrupt.
The peripheral function interrupts are affected by the CM02 bit. When the CM02 bit is set to 0 (peripheral function clock does not stop in wait mode), the peripheral function interrupts can be used to exit wait mode. When the CM02 bit is set to 1 (peripheral function clock stops in wait mode), the peripheral functions using the peripheral function clock stop and the peripheral functions operating with external signals or the on-chip oscillator clock can be used to exit wait mode.
Table 9.4 lists Interrupts to Exit Wait Mode and Usage Conditions.

Table 9.4 Interrupts to Exit Wait Mode and Usage Conditions

Interrupt	CM02 = 0	CM02 = 1
Serial interface interrupt	Usable when operating with internal or external clock	Usable when operating with external clock
Synchronous serial communication unit interrupt/ I^2C bus interface interrupt	Usable in all modes	(Do not use)
Key input interrupt	Usable	Usable
Timer RA interrupt	Usable in all modes	Usable if there is no filter in event counter mode. Usable by selecting fOCO, fC, or fC32 as count source.
Timer RB interrupt	Usable in all modes	Usable by selecting fOCO as timer RA count source and timer RA underflow as timer RB count source
Timer RC interrupt	Usable in all modes	(Do not use)
Timer RE interrupt	Usable in all modes	Usable when operating in real time clock mode
$\overline{INT}$ interrupt	Usable	Usable if there is no filter.
Voltage monitor 1 interrupt	Usable	Usable
Oscillation stop detection interrupt	Usable	(Do not use)

9.7.2.6 Exiting Wait Mode after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode)

Figure 9.7 shows the Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode).

To use a peripheral function interrupt to exit wait mode, set up the following before setting the CM30 bit to 1.

(1) Set the I flag to 0 (maskable interrupt disabled)
(2) Set the interrupt priority level in bits ILVL2 to ILVL0 in the interrupt control registers of the peripheral function interrupts to be used for exiting wait mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting wait mode to 000b (interrupt disabled).
(3) Operate the peripheral function to be used for exiting wait mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 9.7.

The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register	VCA2 Register	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Remarks
FMSTP Bit	VCA20 Bit				
0 (flash memory operates)	0 (internal power low consumption disabled)	0 μs	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	The total of T0 to T2 is the time from wait mode to first instruction execution following exit.
	1 (internal power low consumption enabled)	100 μs (max.)			
1 (flash memory stops)	0 (internal power low consumption disabled	0 μs	Period of system clock × 1 cycle	Same as above	
	1 (internal power low consumption enabled)	100 μs (max.)			

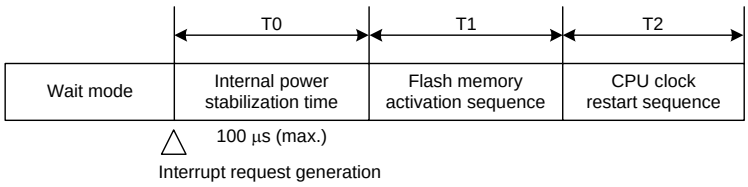


Figure 9.7 Time from Wait Mode to First Instruction Execution following Exit after CM30 Bit in CM3 Register is Set to 1 (MCU Enters Wait Mode)

9.7.2.7 Exiting Wait Mode after WAIT Instruction is Executed

Figure 9.8 shows the Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed. To use a peripheral function interrupt to exit wait mode, set up the following before executing the WAIT instruction.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 in the interrupt control registers of the peripheral function interrupts to be used for exiting wait mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting wait mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting wait mode.

When the MCU exits by a peripheral function interrupt, the time (number of cycles) between interrupt request generation and interrupt routine execution is determined by the settings of the FMSTP bit in the FMR0 register and the VCA20 bit in the VCA2 register, as shown in Figure 9.8.
The clock set by bits CM35, CM36, and CM37 in the CM3 register is used as the CPU clock when the MCU exits wait mode by a peripheral function interrupt. At this time, the CM06 bit in the CM0 register and bits CM16 and CM17 in the CM1 register automatically change.

FMR0 Register FMSTP Bit	VCA2 Register VCA20 Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T1)	Time until CPU Clock Supply (T2)	Time for Interrupt Sequence (T3)	Remarks
0 (flash memory operates)	0 (internal power low consumption disabled)	0 μs	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T3 is the time from wait mode to interrupt routine execution.
	1 (internal power low consumption enabled)	100 μs (max.)				
1 (flash memory stops)	0 (internal power low consumption disabled	0 μs	Period of system clock × 1 cycle	Same as above	Same as above	
	1 (internal power low consumption enabled)	100 μs (max.)				

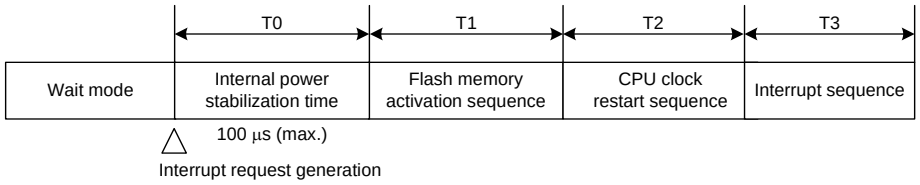


Figure 9.8 Time from Wait Mode to Interrupt Routine Execution after WAIT instruction is Executed

9.7.3 Stop Mode

Since all oscillator circuits except fOCO-WDT stop in stop mode, the CPU and peripheral function clocks stop and the CPU and the peripheral functions operating with these clocks also stop. The least power required to operate the MCU is in stop mode. If the voltage applied to the VCC pin is VRAM or more, the contents of internal RAM is retained.
The peripheral functions clocked by external signals continue operating.
Table 9.5 lists Interrupts to Exit Stop Mode and Usage Conditions.

Table 9.5 Interrupts to Exit Stop Mode and Usage Conditions

Interrupt	Usage Conditions
Key input interrupt	Usable
$\overline{\text{INT}}$ interrupt	Usable if there is no filter
Timer RA interrupt	Usable if there is no filter when external pulse is counted in event counter mode
Serial interface interrupt	When external clock selected
Voltage monitor 1 interrupt	Usable in digital filter disabled mode (VW1C1 bit in VW1C register is set to 1)

9.7.3.1 Entering Stop Mode

The MCU enters stop mode when the CM10 bit in the CM1 register is set to 1 (all clocks stop). At the same time, the CM06 bit in the CM0 register is set to 1 (divide-by-8 mode).
To use stop mode, set the following before the MCU enters stop mode:

- Bits OCD1 to OCD0 in the OCD register = 00b
- CM35 bit in CM3 register = 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

Enter stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled). Do not enter stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

9.7.3.2 Pin Status in Stop Mode

The I/O ports retain the status before the MCU enters stop mode.
The XOUT pin is held “H”.

9.7.3.3 Exiting Stop Mode

The MCU exits stop mode by a reset or peripheral function interrupt.
Figure 9.9 shows the Time from Stop Mode to Interrupt Routine Execution.
To use a peripheral function interrupt to exit stop mode, set up the following before setting the CM10 bit to 1.

(1) Set the interrupt priority level in bits ILVL2 to ILVL0 of the peripheral function interrupts to be used for exiting stop mode. Set bits ILVL2 to ILVL0 of the peripheral function interrupts that are not to be used for exiting stop mode to 000b (interrupt disabled).
(2) Set the I flag to 1.
(3) Operate the peripheral function to be used for exiting stop mode.
When the MCU exits stop mode by a peripheral function interrupt, the interrupt sequence is executed when an interrupt request is generated and the CPU clock supply starts.

The clock used immediately before stop mode divided by 8 is used as the CPU clock when the MCU exits stop mode by a peripheral function interrupt. To enter stop mode, set the CM35 bit in the CM3 register to 0 (settings of CM06 bit in CM0 register and bits CM16 and CM17 in CM1 register enabled)

FMR0 Register / FMSTP Bit	Internal Power Stabilization Time (T0)	Time until Flash Memory Activation (T2)	Time until CPU Clock Supply (T3)	Time for Interrupt Sequence (T4)	Remarks
0 (flash memory operates)	100 μs (max.)	Period of system clock × 1 cycle + 60 μs (max.)	Period of CPU clock × 2 cycles	Period of CPU clock × 20 cycles	The total of T0 to T4 is the time from stop mode to interrupt routine execution.
1 (flash memory stops)	100 μs (max.)	Period of system clock × 1 cycle	Same as above	Same as above	

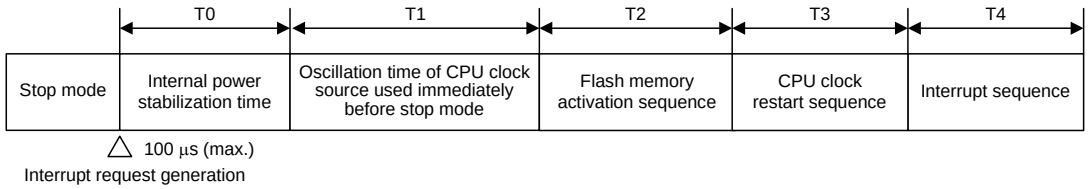


Figure 9.9 Time from Stop Mode to Interrupt Routine Execution

Figure 9.10 shows the State Transitions in Power Control Mode.

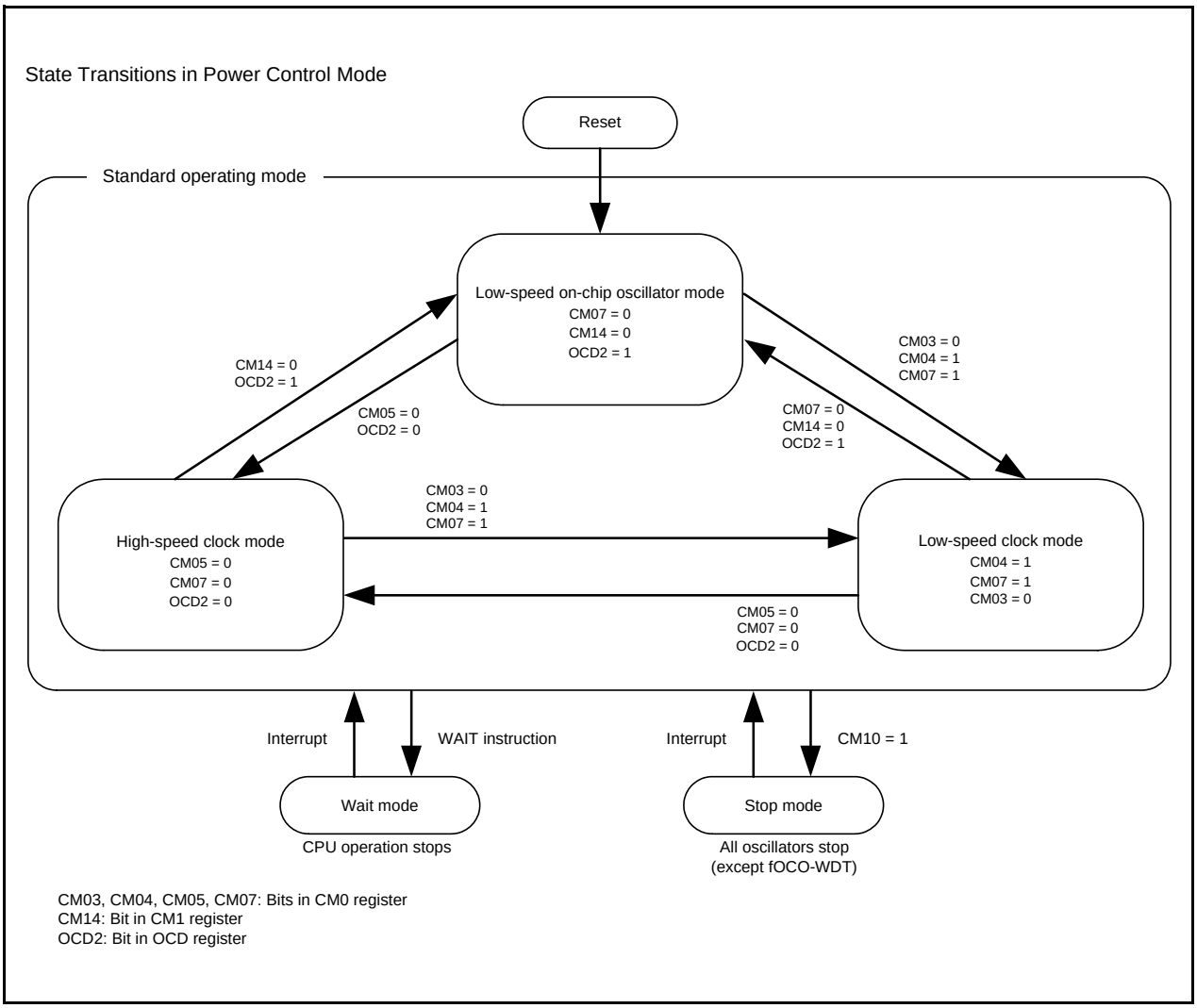


Figure 9.10 State Transitions in Power Control Mode

9.8 Oscillation Stop Detection Function

The oscillation stop detection function detects the stop of the XIN clock oscillating circuit.
The oscillation stop detection function can be enabled and disabled by the OCD0 bit in the OCD register.
Table 9.6 lists the Specifications of Oscillation Stop Detection Function.

When the XIN clock is the CPU clock source and bits OCD1 to OCD0 are set to 11b, the MCU is placed in the following state if the XIN clock stops.

- OCD2 bit in OCD register = 1 (on-chip oscillator clock selected)
- OCD3 bit in OCD register = 1 (XIN clock stops)
- CM14 bit in CM1 register = 0 (low-speed on-chip oscillator oscillates)
- Oscillation stop detection interrupt request is generated

Table 9.6 Specifications of Oscillation Stop Detection Function

Item	Specification
Oscillation stop detection clock and frequency bandwidth	f(XIN) ≥ 2 MHz
Enabled condition for oscillation stop detection function	Bits OCD1 to OCD0 set to 11b
Operation at oscillation stop detection	Oscillation stop detection interrupt generated

9.8.1 How to Use Oscillation Stop Detection Function

- The oscillation stop detection interrupt shares a vector with the watchdog timer interrupt, and the voltage monitor interrupt. To use the oscillation stop detection interrupt and watchdog timer interrupt, the interrupt source needs to be determined.
- When the XIN clock restarts after oscillation stop, switch the XIN clock to the clock source for the CPU clock and the peripheral functions by a program.
  Figure 9.11 shows the Procedure for Switching to XIN Clock when XIN Clock Re-Oscillates after Oscillation Stop is Detected.
- To enter wait mode while the oscillation stop detection function is used, set the CM02 bit to 0 (peripheral function clock does not stop in wait mode).
- Since the oscillation stop detection function is a function for cases where the XIN clock is stopped by an external cause, set bits OCD1 to OCD0 to 00b to stop or start the XIN clock by a program (select stop mode or change the CM05 bit).
- This function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 to OCD0 to 00b.
- To use the low-speed on-chip oscillator clock as the clock source for the CPU clock and the peripheral functions after detecting the oscillation stop, set bits OCD1 to OCD0 to 11b.

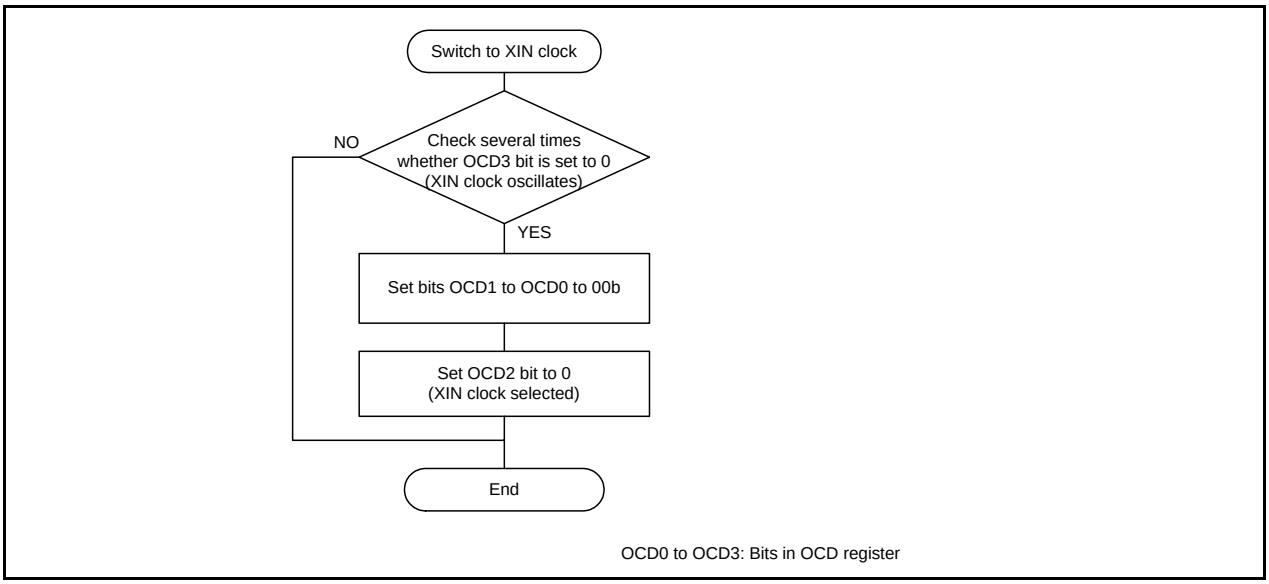


Figure 9.11 Procedure for Switching to XIN Clock when XIN Clock Re-Oscillates after Oscillation Stop is Detected

9.9 Notes on Clock Generation Circuit

9.9.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

- Program example to enter stop mode

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7, FMR2     ; Low-current-consumption read mode disabled
        BSET    0, PRCR     ; Writing to CM1 register enabled
        FSET    I           ; Interrupt enabled
        BSET    0, CM1      ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

9.9.2 Wait Mode

When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the FMR27 bit to 0 (low-current-consumption read mode disabled) before entering the mode. Do not enter wait mode while the FMR01 bit is 1 (CPU rewrite mode enabled) or the FMR27 bit is 1 (low-current-consumption read mode enabled).
To enter wait mode by setting the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).
To enter wait mode using the WAIT instruction, set the I flag to 1 (maskable interrupt enabled). An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

- Program example to execute the WAIT instruction

```
BCLR    1, FMR0     ; CPU rewrite mode disabled
BCLR    7, FMR2     ; Low-current-consumption read mode disabled
FSET    I           ; Interrupt enabled
WAIT                ; Wait mode
NOP
NOP
NOP
NOP
```

- Program example to execute the instruction to set the CM30 bit to 1

```
BCLR    1, FMR0     ; CPU rewrite mode disabled
BCLR    7, FMR2     ; Low-current-consumption read mode disabled
BSET    0, PRCR     ; Writing to CM3 register enabled
FCLR    I           ; Interrupt disabled
BSET    0, CM3      ; Wait mode
NOP
NOP
NOP
NOP
BCLR    0, PRCR     ; Writing to CM3 register disabled
FSET    I           ; Interrupt enabled
```

9.9.3 Reducing Internal Power Using VCA20 Bit

Set the VCA20 bit to 1 in low-speed clock mode or low-speed on-chip oscillator mode before entering wait mode.
To enter wait mode by setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode), follow the procedure shown in Figure 9.5 to set the procedure for reducing internal power consumption using the VCA20 bit.
To enter wait mode by executing WAIT instruction, follow the procedure shown in Figure 9.6 to set the procedure for reducing internal power consumption using the VCA20 bit.

9.9.4 Oscillator Stop Detection Function

The oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 to OCD0 in the OCD register to 00b. In addition, the OCD3 bit cannot be used to confirm whether the XIN clock oscillation is stable.

9.9.5 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

10. Protection

The protection function protects important registers from being easily overwritten if a program runs out of control. The registers protected by the PRCR register are as follows:

- Registers protected by PRC0 bit: Registers CM0, CM1, CM3, OCD
- Registers protected by PRC1 bit: Registers PM0 and PM1
- Registers protected by PRC2 bit: PD0 register
- Registers protected by PRC3 bit: Registers VCA2, VD1LS, VW0C, VW1C, and VW2C

10.1 Register

10.1.1 Protect Register (PRCR)

Address 000Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	PRC3	PRC2	PRC1	PRC0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD. 0: Write disabled 1: Write enabled (2)	R/W
b1	PRC1	Protect bit 1	Enables writing to registers PM0 and PM1. 0: Write disabled 1: Write enabled (2)	R/W
b2	PRC2	Protect bit 2	Enables writing to the PD0 register. 0: Write disabled 1: Write enabled (1)	R/W
b3	PRC3	Protect bit 3	Enables writing to registers VCA2, VD1LS, VW0C, VW1C, and VW2C. 0: Write disabled 1: Write enabled (2)	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:

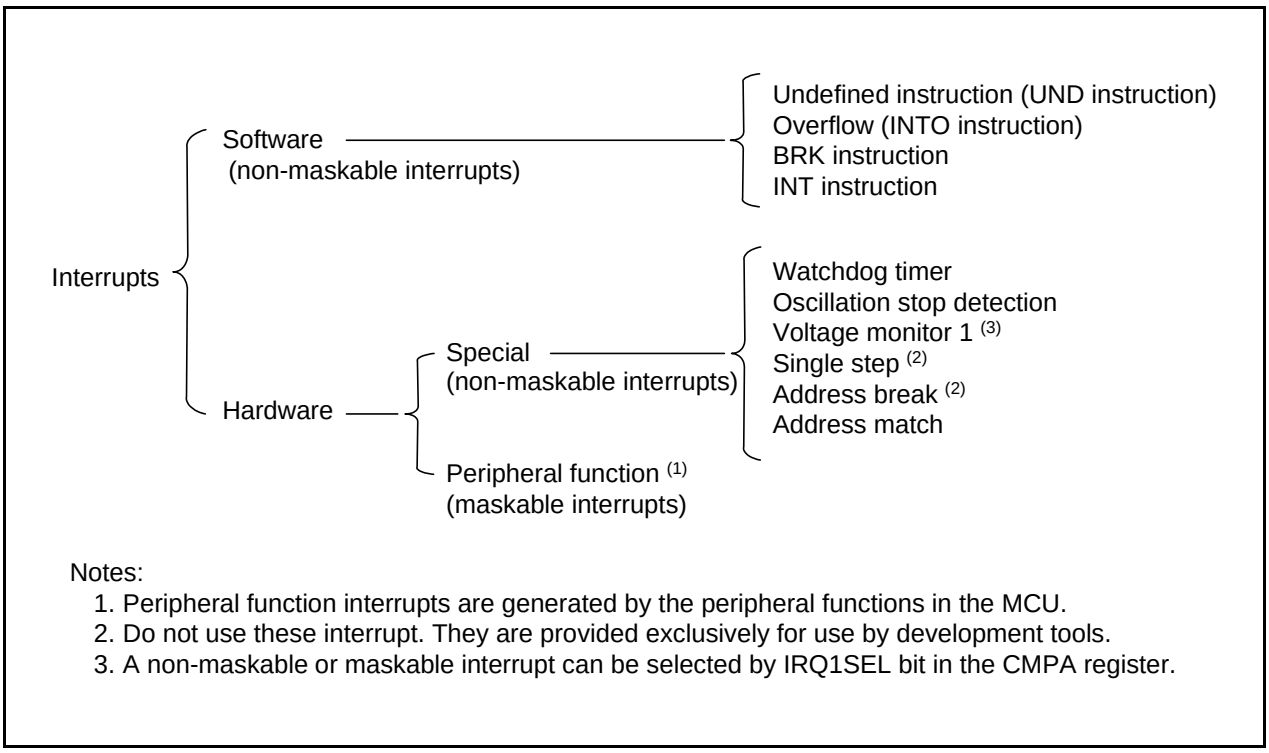
1. The PRC2 bit is set to 0 after setting it to 1 (write enabled) and writing to the SFR area. Change the register protected by the PRC2 bit with the next instruction after that used to set the PRC2 bit to 1. Do not allow interrupts or DTC activation between the instruction to set to the PRC2 bit to 1 and the next instruction.
2. Bits PRC0, PRC1, and PRC3 are not set to 0 even after setting them to 1 (write enabled) and writing to the SFR areas. Set these bits to 0 by a program.

11. Interrupts

11.1 Overview

11.1.1 Types of Interrupts

Figure 11.1 shows the Types of Interrupts.



Notes:
1. Peripheral function interrupts are generated by the peripheral functions in the MCU.
2. Do not use these interrupt. They are provided exclusively for use by development tools.
3. A non-maskable or maskable interrupt can be selected by IRQ1SEL bit in the CMPA register.

Figure 11.1 Types of Interrupts

- Maskable interrupts: These interrupts are enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **can be changed** based on the interrupt priority level.
- Non-maskable interrupts: These interrupts are not enabled or disabled by the interrupt enable flag (I flag). The interrupt priority **cannot be changed** based on the interrupt priority level.

11.1.2 Software Interrupts

A software interrupt is generated when an instruction is executed. Software interrupts are non-maskable.

11.1.2.1 Undefined Instruction Interrupt

An undefined instruction interrupt is generated when the UND instruction is executed.

11.1.2.2 Overflow Interrupt

An overflow interrupt is generated when the O flag is set to 1 (arithmetic operation overflow) and the INTO instruction is executed. Instructions that set the O flag are as follows:
ABS, ADC, ADCF, ADD, CMP, DIV, DIVU, DIVX, NEG, RMPA, SBB, SHA, and SUB.

11.1.2.3 BRK Interrupt

A BRK interrupt is generated when the BRK instruction is executed.

11.1.2.4 INT Instruction Interrupt

An INT instruction interrupt is generated when the INT instruction is executed. Software interrupt numbers 0 to 63 can be specified with the INT instruction. Because some software interrupt numbers are assigned to peripheral function interrupts, the same interrupt routine as for peripheral function interrupts can be executed by executing the INT instruction.
For software interrupt numbers 0 to 31, the U flag is saved on the stack during instruction execution and the U flag is set to 0 (ISP selected) before the interrupt sequence is executed. The U flag is restored from the stack when returning from the interrupt routine. For software interrupt numbers 32 to 63, the U flag does not change state during instruction execution, and the selected SP is used.

11.1.3 Special Interrupts

Special interrupts are non-maskable.

11.1.3.1 Watchdog Timer Interrupt

A watchdog timer interrupt is generated by the watchdog timer. For details, refer to **14. Watchdog Timer**.

11.1.3.2 Oscillation Stop Detection Interrupt

An oscillation stop detection interrupt is generated by the oscillation stop detection function. For details of the oscillation stop detection function, refer to **9. Clock Generation Circuit**.

11.1.3.3 Voltage Monitor 1 Interrupt

A voltage monitor 1 interrupt is generated by the voltage detection circuit. A non-maskable or maskable interrupt can be selected by IRQ1SEL bit in the CMPA register. When the IRQ1SEL bit in the CMPA register is set to 0, a non-maskable interrupt (fixed vector table) is selected. When this bit is set to 1, a maskable interrupt (variable vector table) is selected. For details of the voltage detection circuit, refer to **6. Voltage Detection Circuit**.

11.1.3.4 Single-Step Interrupt, and Address Break Interrupt

Do not use these interrupts. They are provided exclusively for use by development tools.

11.1.3.5 Address Match Interrupt

An address match interrupt is generated immediately before executing an instruction that is stored at an address indicated by registers RMAD0 to RMAD1 if the AIER00 bit in the AIER0 register or the AIER10 bit in the AIER1 register is set to 1 (address match interrupt enabled).
For details of the address match interrupt, refer to **11.6 Address Match Interrupt**.

11.1.4 Peripheral Function Interrupts

A peripheral function interrupt is generated by a peripheral function in the MCU. Peripheral function interrupts are maskable. Refer to **Tables 11.2 and 11.3 Relocatable Vector Tables** for sources of the corresponding peripheral function interrupt. For details of peripheral functions, refer to the descriptions of individual peripheral functions.

11.1.5 Interrupts and Interrupt Vectors

There are 4 bytes in each vector. Set the starting address of an interrupt routine in each interrupt vector. When an interrupt request is acknowledged, the CPU branches to the address set in the corresponding interrupt vector. Figure 11.2 shows an Interrupt Vector.

Figure 11.2 Interrupt Vector

11.1.5.1 Fixed Vector Tables

The fixed vector tables are allocated addresses 0FFDCh to 0FFFFh.
Table 11.1 lists the Fixed Vector Tables. The vector addresses (H) of fixed vectors are used by the ID code check function. For details, refer to **26.3 Functions to Prevent Flash Memory from being Rewritten**.

Table 11.1 Fixed Vector Tables

Interrupt Source	Vector Addresses Address (L) to (H)	Remarks	Reference
Undefined instruction	0FFDCh to 0FFDFh	Interrupt with UND instruction	R8C/Tiny Series Software Manual
Overflow	0FFE0h to 0FFE3h	Interrupt with INTO instruction	
BRK instruction	0FFE4h to 0FFE7h	If the content of address 0FFE6h is FFh, program execution starts from the address shown by the vector in the relocatable vector table.	
Address match	0FFE8h to 0FFEBh		11.6 Address Match Interrupt
Single step (1)	0FFECh to 0FFEFh		
Watchdog timer, Oscillation stop detection, Voltage monitor 1 (2)	0FFF0h to 0FFF3h		14. Watchdog Timer 9. Clock Generation Circuit 6. Voltage Detection Circuit
Address break (1)	0FFF4h to 0FFF7h		
(Reserved)	0FFF8h to 0FFFBh		
Reset	0FFFCh to 0FFFFh		5. Resets

Notes:
1. Do not use these interrupts. They are provided exclusively for use by development tools.
2. Voltage monitor 1 interrupt is selected when the IRQ1SEL bit in the CMPA register is set to 0 (non-maskable interrupt).

11.1.5.2 Relocatable Vector Tables

The relocatable vector tables occupy 256 bytes beginning from the starting address set in the INTB register. Tables 11.2 and 11.3 list the Relocatable Vector Tables.

Table 11.2 Relocatable Vector Tables (1)

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
BRK instruction (3)	+0 to +3 (0000h to 0003h)	0	—	R8C/Tiny Series Software Manual
Flash memory ready	+4 to +7 (0004h to 0007h)	1	FMRDYIC	26. Flash Memory
BB Timer compare 2	+ 8 to +12 (0008h to 000Bh)	2	BBTIM2IC	25. Baseband Functionality
(Reserved)		3 to 5	—	—
(Reserved)		6	—	—
Timer RC	+28 to +31 (001Ch to 001Fh)	7	TRCIC	19. Timer RC
(Reserved)		8	—	—
(Reserved)		9	—	—
Timer RE	+40 to +43 (0028h to 002Bh)	10	TREIC	20. Timer RE
(Reserved)		11	—	—
(Reserved)		12	—	—
Key input	+52 to +55 (0034h to 0037h)	13	KUPIC	11.5 Key Input Interrupt
(Reserved)		14	—	—
Synchronous serial communication unit/ I^2C bus interface (2)	+60 to +63 (003Ch to 003Fh)	15	SSUIC/IICIC	23. Synchronous Serial Communication Unit (SSU), 24. I^2C bus Interface
(Reserved)		16	—	—
UART0 transmit	+68 to +71 (0044h to 0047h)	17	S0TIC	21. Serial Interface (UART0)
UART0 receive	+72 to +75 (0048h to 004Bh)	18	S0RIC	
(Reserved)		19	—	—
Bank 0 reception complete, IDLE (3)	+80 to +83 (0050h to 0053h)	20	BBRX0IC/ BBIDLEIC	25. Baseband Functionality
(Reserved)		21	—	—
Timer RA	+88 to +91 (0058h to 005Bh)	22	TRAIC	17. Timer RA
(Reserved)		23	—	—
Timer RB	+96 to +99 (0060h to 0063h)	24	TRBIC	18. Timer RB
$\overline{INT1}$	+100 to +103 (0064h to 0067h)	25	INT1IC	11.4 $\overline{INT}$ Interrupt
$\overline{INT3}$	+104 to +107 (0068h to 006Bh)	26	INT3IC	
(Reserved)		27	—	—
BB Timer compare 1	+112 to +115 (0070h to 0073h)	28	BBTIM1IC	25. Baseband Functionality
$\overline{INT0}$	+116 to +119 (0074h to 0077h)	29	INT0IC	11.4 $\overline{INT}$ Interrupt
CCA complete	+120 to +123 (0078h to 007Bh)	30	BBCCAIC	25. Baseband Functionality
BB Timer compare 0	+124 to +127 (007Ch to 007Fh)	31	BBTIM0IC	25. Baseband Functionality

Notes:
1. These addresses are relative to those in the INTB register.
2. Selectable by the IICSEL bit in the SSUIICSR register.
3. Selectable by the BANK0INTSEL bit in the BBTXRXMODE4 register.

Table 11.3 Relocatable Vector Tables (2)

Interrupt Source	Vector Addresses (1) Address (L) to Address (H)	Software Interrupt Number	Interrupt Control Register	Reference
Software (2)	+128 to +131 (0080h to 0083h) to +164 to +167 (00A4h to 00A7h)	32 to 41	—	R8C/Tiny Series Software Manual
(Reserved)		42 to 43	—	—
Address filter	+176 to +179 (00B0h to 00B3h)	44	BBADFIC	25. Baseband Functionality
Transmit overrun	+180 to +183 (00B4h to 00B7h))	45	BBTXORIC	25. Baseband Functionality
Transmission complete	+184 to +187 (00B8h to 00BBh)	46	BBTXIC	25. Baseband Functionality
Receive overrun 1	+188 to +191 (00BCh to 00BFh)	47	BBRXOR1IC	25. Baseband Functionality
PLL lock/ unlock detection	+192 to +195 (00C0h to 00C3h)	48	BBPLLIC	25. Baseband Functionality
Receive overrun 0/ calibration complete (5)	+196 to +199 (00C4h to 00C7h)	49	BBRXOR0IC/ BBCALIC	25. Baseband Functionality
Voltage monitor 1 (4)	+200 to +203 (00C8h to 00CBh)	50	VCMP1IC	6. Voltage Detection Circuit
Bank 1 reception complete/ clock regulator (3)	+204 to +207 (00CCh to 00CFh)	51	BBRX1IC/ BBCREGIC	25. Baseband Functionality
(Reserved)		52 to 55	—	—
Software (2)	+224 to +227 (00E0h to 00E3h) to +252 to +255 (00FCh to 00FFh)	56 to 63		R8C/Tiny Series Software Manual

Notes:
1. These addresses are relative to those in the INTB register.
2. These interrupts are not disabled by the I flag.
3. Selectable by the BANK1INTSEL bit in the BBTXRXMODE4 register.
4. Voltage monitor 1 interrupt is selected when the IRQ1SEL bit in the CMPA register is set to 1 (maskable interrupt).
5. Can be selected by the ROR0INTSEL bit in the BBTXRXMODE4 register.

11.2 Registers

11.2.1 Interrupt Control Register (BBTIM2IC, TREIC, KUPIC, S0TIC, S0RIC, BBRX0IC/BBIDLEIC, TRAIC, TRBIC, BBTIM1IC, BBCCAIC, BBTIM0IC, BBADFIC, BBTXORIC, BBTXIC, BBRXOR1IC, BBPLLIC, BBRXOR0IC/BBCALIC, VCMP1IC, BBRX1IC/BBCREGIC)

Address 0042h (BBTIM2IC), 004Ah (TREIC), 004Dh (KUPIC), 0051h (S0TIC), 0052h (S0RIC), 0054h (BBRX0IC/BBIDLEIC), 0056h (TRAIC), 0058h (TRBIC), 005Ch (BBTIM1IC), 005Eh (BBCCAIC), 005Fh (BBTIM0IC), 006Ch (BBADFIC), 006Dh (BBTXORIC), 006Eh (BBTXIC), 006Fh (BBRXOR1IC), 0070h (BBPLLIC), 0071h (BBRXOR0IC/BBCALIC), 0072h (VCMP1IC) (2), 0073h (BBRX1IC/BBCREGIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Notes:
1. Only 0 can be written to the IR bit. (Do not write 1 to this bit.)
2. The VCMP1IC register can be used when the IRQ1SEL bit in the CMPA register is set to 1 (maskable interrupt).

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.9.5 Rewriting Interrupt Control Register**.

11.2.2 Interrupt Control Register (FMRDYIC, TRCIC, SSUIC/IICIC)

Address 0041h (FMRDYIC), 0047h (TRCIC), 004Fh (SSUIC/IICIC (1))

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	X	X	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b5	—			
b6	—			
b7	—			

Note:
1. Selectable by the IICSEL bit in the SSUIICSR register.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated. Refer to **11.9.5 Rewriting Interrupt Control Register**.

11.2.3 INTi Interrupt Control Register (INTiIC) (i = 0, 1, 3)

Address 0059h (INT1IC), 005Ah (INT3IC), 005Dh (INT0IC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	POL	IR	ILVL2	ILVL1	ILVL0
After Reset	X	X	0	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled) 0 0 1: Level 1 0 1 0: Level 2 0 1 1: Level 3 1 0 0: Level 4 1 0 1: Level 5 1 1 0: Level 6 1 1 1: Level 7	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W (1)
b4	POL	Polarity switch bit (3)	0: Falling edge selected 1: Rising edge selected (2)	R/W
b5	—	Reserved bit	Set to 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b7	—			

Notes:
1. Only 0 can be written to the IR bit. (Do not write 1 to this bit.)
2. If the INTiPL bit in the INTEN register is set to 1 (both edges), set the POL bit to 0 (falling edge selected).
3. The IR bit may be set to 1 (interrupt requested) when the POL bit is rewritten.
   Refer to **11.9.4 Changing Interrupt Sources**.

Rewrite the interrupt control register when an interrupt request corresponding to the register is not generated.
Refer to **11.9.5 Rewriting Interrupt Control Register**.

11.3 Interrupt Control

The following describes enabling and disabling maskable interrupts and setting the acknowledgement priority. This description does not apply to non-maskable interrupts.
Use the I flag in the FLG register, IPL, and bits ILVL2 to ILVL0 in the corresponding interrupt control register to enable or disable a maskable interrupt. Whether an interrupt is requested or not is indicated by the IR bit in the corresponding interrupt control register.

11.3.1 I Flag

The I flag enables or disables maskable interrupts. Setting the I flag to 1 (enabled) enables maskable interrupts. Setting the I flag to 0 (disabled) disables all maskable interrupts.

11.3.2 IR Bit

The IR bit is set to 1 (interrupt requested) when an interrupt request is generated. After the interrupt request is acknowledged and the CPU branches to the corresponding interrupt vector, the IR bit is set to 0 (no interrupt requested).
The IR bit can be set to 0 by a program. Do not write 1 to this bit.
However, the IR bit operations of the timer RC interrupt, the synchronous serial communication unit interrupt the I^2C bus interface interrupt, and the flash memory interrupt are different. Refer to **11.7 Timer RC Interrupt, Synchronous Serial Communication Unit Interrupt, I^2C bus Interface Interrupt, and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)**.

11.3.3 Bits ILVL2 to ILVL0, IPL

Interrupt priority levels can be set using bits ILVL2 to ILVL0.
Table 11.4 lists the Settings of Interrupt Priority Levels and Table 11.5 lists the Interrupt Priority Levels Enabled by IPL.
The following are the conditions when an interrupt is acknowledged:

- I flag = 1
- IR bit = 1
- Interrupt priority level > IPL

The I flag, IR bit, bits ILVL2 to ILVL0, and IPL are independent of each other. They do not affect one another.

Table 11.4 Settings of Interrupt Priority Levels

Bits ILVL2 to ILVL0	Interrupt Priority Level	Priority
000b	Level 0 (interrupt disabled)	—
001b	Level 1	Low
010b	Level 2	
011b	Level 3	
100b	Level 4	
101b	Level 5	
110b	Level 6	
111b	Level 7	High

Table 11.5 Interrupt Priority Levels Enabled by IPL

IPL	Enabled Interrupt Priority Level
000b	Interrupt level 1 and above
001b	Interrupt level 2 and above
010b	Interrupt level 3 and above
011b	Interrupt level 4 and above
100b	Interrupt level 5 and above
101b	Interrupt level 6 and above
110b	Interrupt level 7 and above
111b	All maskable interrupts are disabled

11.3.4 Interrupt Sequence

The following describes an interrupt sequence which is performed from when an interrupt request is acknowledged until the interrupt routine is executed.
When an interrupt request is generated while an instruction is being executed, the CPU determines its interrupt priority level after the instruction is completed. The CPU starts the interrupt sequence from the following cycle. However, for the SMOVB, SMOVF, SSTR, or RMPA instruction, if an interrupt request is generated while the instruction is being executed, the CPU suspends the instruction to start the interrupt sequence. The interrupt sequence is performed as indicated below.
Figure 11.3 shows the Time Required for Executing Interrupt Sequence.

(1) The CPU obtains interrupt information (interrupt number and interrupt request level) by reading address 00000h. The IR bit for the corresponding interrupt is set to 0 (no interrupt requested). (2)
(2) The FLG register is saved to a temporary register (1) in the CPU immediately before entering the interrupt sequence.
(3) The I, D and U flags in the FLG register are set as follows:
The I flag is set to 0 (interrupts disabled).
The D flag is set to 0 (single-step interrupt disabled).
The U flag is set to 0 (ISP selected).
However, the U flag does not change state if an INT instruction for software interrupt number 32 to 63 is executed.
(4) The CPU internal temporary register (1) is saved on the stack.
(5) The PC is saved on the stack.
(6) The interrupt priority level of the acknowledged interrupt is set in the IPL.
(7) The starting address of the interrupt routine set in the interrupt vector is stored in the PC.

After the interrupt sequence is completed, instructions are executed from the starting address of the interrupt routine.

Notes:
1. These registers cannot be accessed by the user.
2. Refer to **11.7 Timer RC Interrupt, Synchronous Serial Communication Unit Interrupt, I²C bus Interface Interrupt, and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)** for the IR bit operations of the timer RC Interrupt, Synchronous Serial Communication unit Interrupt, and the I²C bus Interface Interrupt.

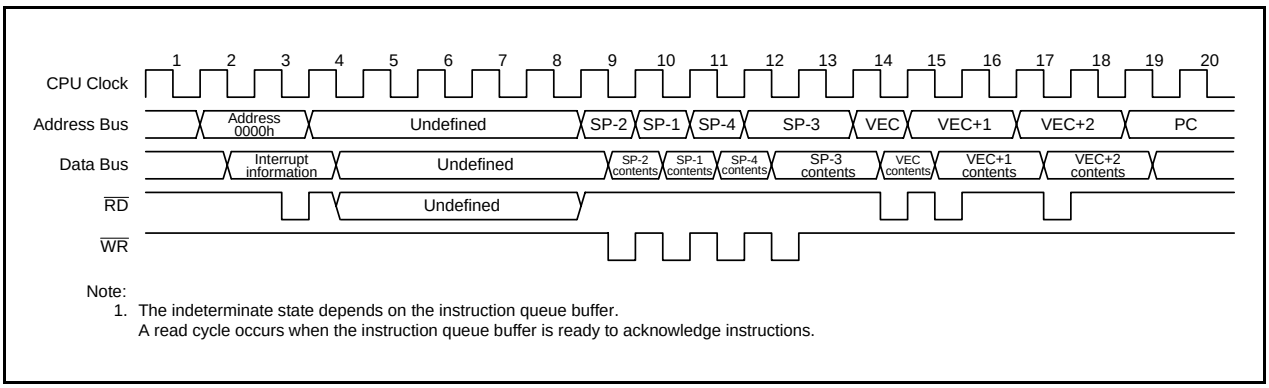
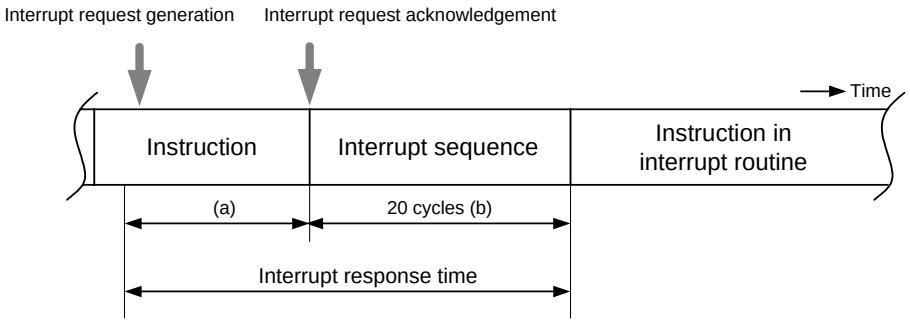


Figure 11.3 Time Required for Executing Interrupt Sequence

11.3.5 Interrupt Response Time

Figure 11.4 shows the Interrupt Response Time. The interrupt response time is the period from when an interrupt request is generated until the first instruction in the interrupt routine is executed. The interrupt response time includes the period from when an interrupt request is generated until the currently executing instruction is completed (refer to (a) in Figure 11.4) and the period required for executing the interrupt sequence (20 cycles, refer to (b) in Figure 11.4).



(a) The period from when an interrupt request is generated until the currently executing instruction is completed. The length of time varies depending on the instruction being executed. The DIVX instruction requires the longest time, 30 cycles (no wait states if the divisor is a register).
(b) 21 cycles for address match and single-step interrupts.

Figure 11.4 Interrupt Response Time

11.3.6 IPL Change when Interrupt Request is Acknowledged

When a maskable interrupt request is acknowledged, the interrupt priority level of the acknowledged interrupt is set in the IPL.
When a software interrupt or special interrupt request is acknowledged, the level listed in Table 11.6 is set in the IPL.
Table 11.6 lists the IPL Value When Software or Special Interrupt is Acknowledged.

Table 11.6 IPL Value When Software or Special Interrupt is Acknowledged

Interrupt Source without Interrupt Priority Level	Value Set in IPL
Watchdog timer, oscillation stop detection, voltage monitor 1 (1), address break	7
Software, address match, single-step	Not changed

Note:
1. Voltage monitor 1 interrupt is selected when the IRQ1SEL bit in the CMPA register is set to 0 (non-maskable interrupt).

11.3.7 Saving Registers

In the interrupt sequence, the FLG register and PC are saved on the stack.
After an extended 16 bits, 4 high-order bits in the PC and 4 high-order (IPL) and 8 low-order bits in the FLG register, are saved on the stack, the 16 low-order bits in the PC are saved.
Figure 11.5 shows the Stack State Before and After Acknowledgement of Interrupt Request.
The other necessary registers should be saved by a program at the beginning of the interrupt routine. The PUSHM instruction can save several registers in the register bank being currently used (1) with a single instruction.

Note:
1. Selectable from registers R0, R1, R2, R3, A0, A1, SB, and FB.

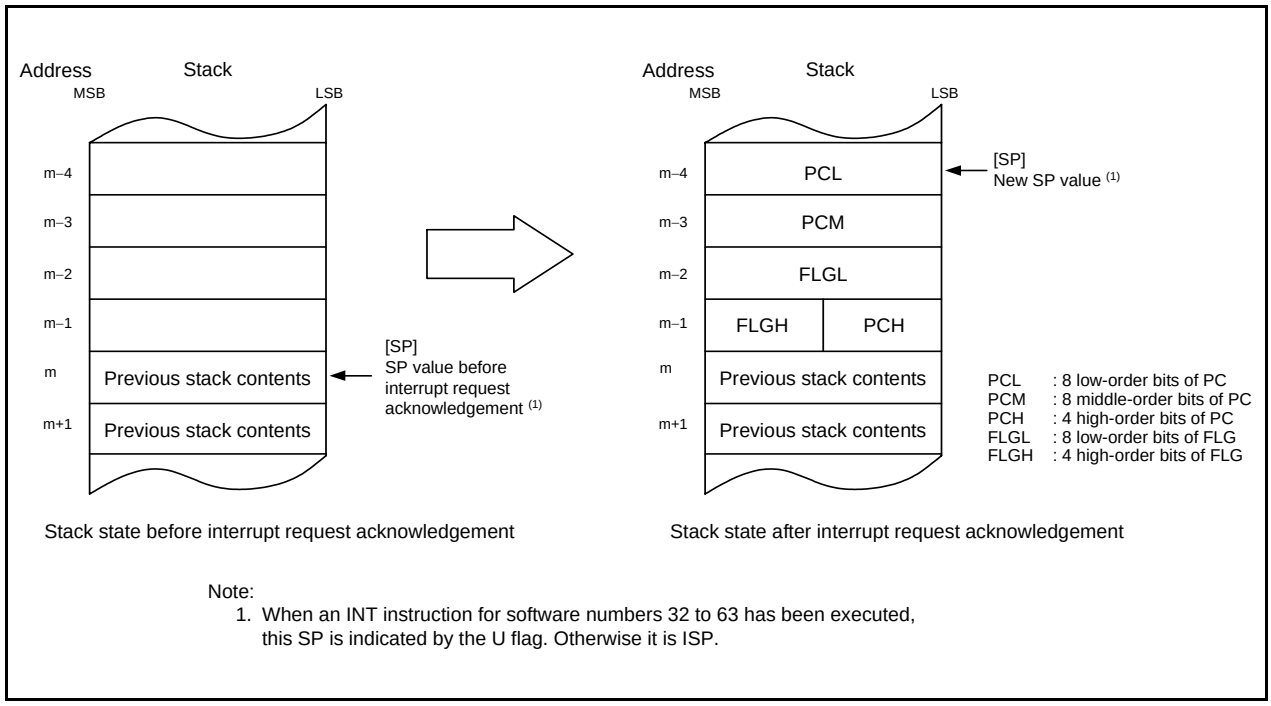
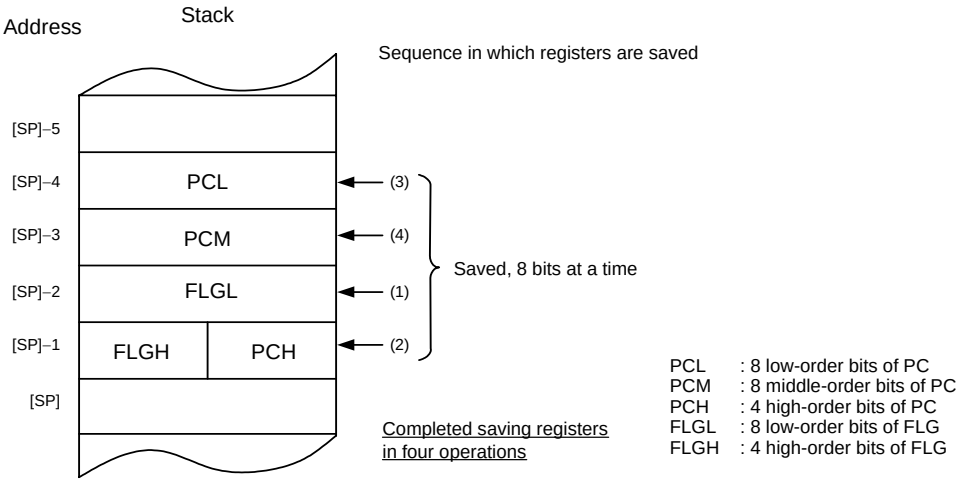


Figure 11.5 Stack State Before and After Acknowledgement of Interrupt Request

The register saving operation, which is performed as part of the interrupt sequence, saved in 8 bits at a time in four steps.
Figure 11.6 shows the Register Saving Operation.



Note:
1. [SP] indicates the SP initial value when an interrupt request is acknowledged.
After registers are saved, the SP content is [SP] minus 4.
When an INT instruction for software numbers 32 to 63 has been executed,
this SP is indicated by the U flag. Otherwise it is ISP.

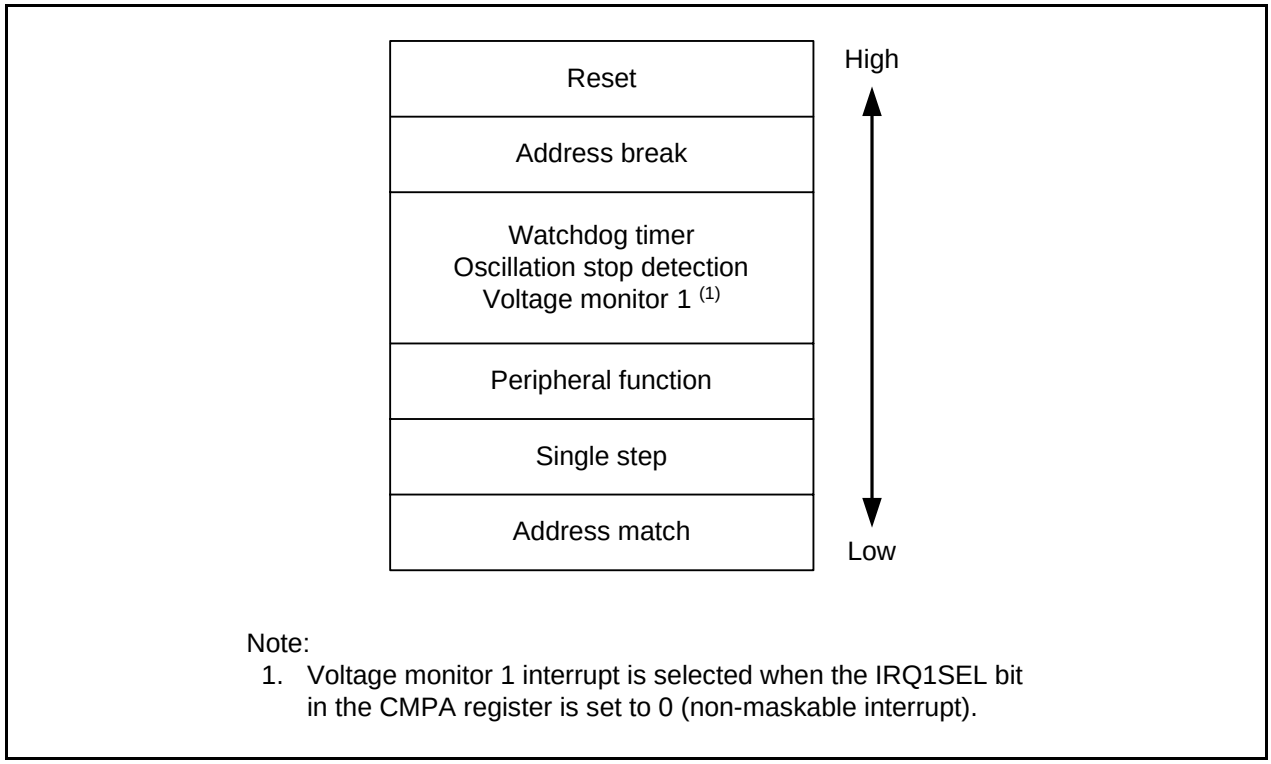
Figure 11.6 Register Saving Operation

11.3.8 Returning from Interrupt Routine

When the REIT instruction is executed at the end of an interrupt routine, the FLG register and PC, which have been saved on the stack, are automatically restored. The program, that was running before the interrupt request was acknowledged, starts running again.
Registers saved by a program in an interrupt routine should be saved using the POPM instruction or a similar instruction before executing the REIT instruction.

11.3.9 Interrupt Priority

If two or more interrupt requests are generated while a single instruction is being executed, the interrupt with the higher priority is acknowledged.
Set bits ILVL2 to ILVL0 to select any priority level for maskable interrupts (peripheral function). However, if two or more maskable interrupts have the same priority level, their interrupt priority is resolved by hardware, with the higher priority interrupts acknowledged.
The priority of watchdog timer and other special interrupts is set by hardware.
Figure 11.7 shows the Hardware Interrupt Priority.
Software interrupts are not affected by the interrupt priority. If an instruction is executed, the CPU executes the interrupt routine.

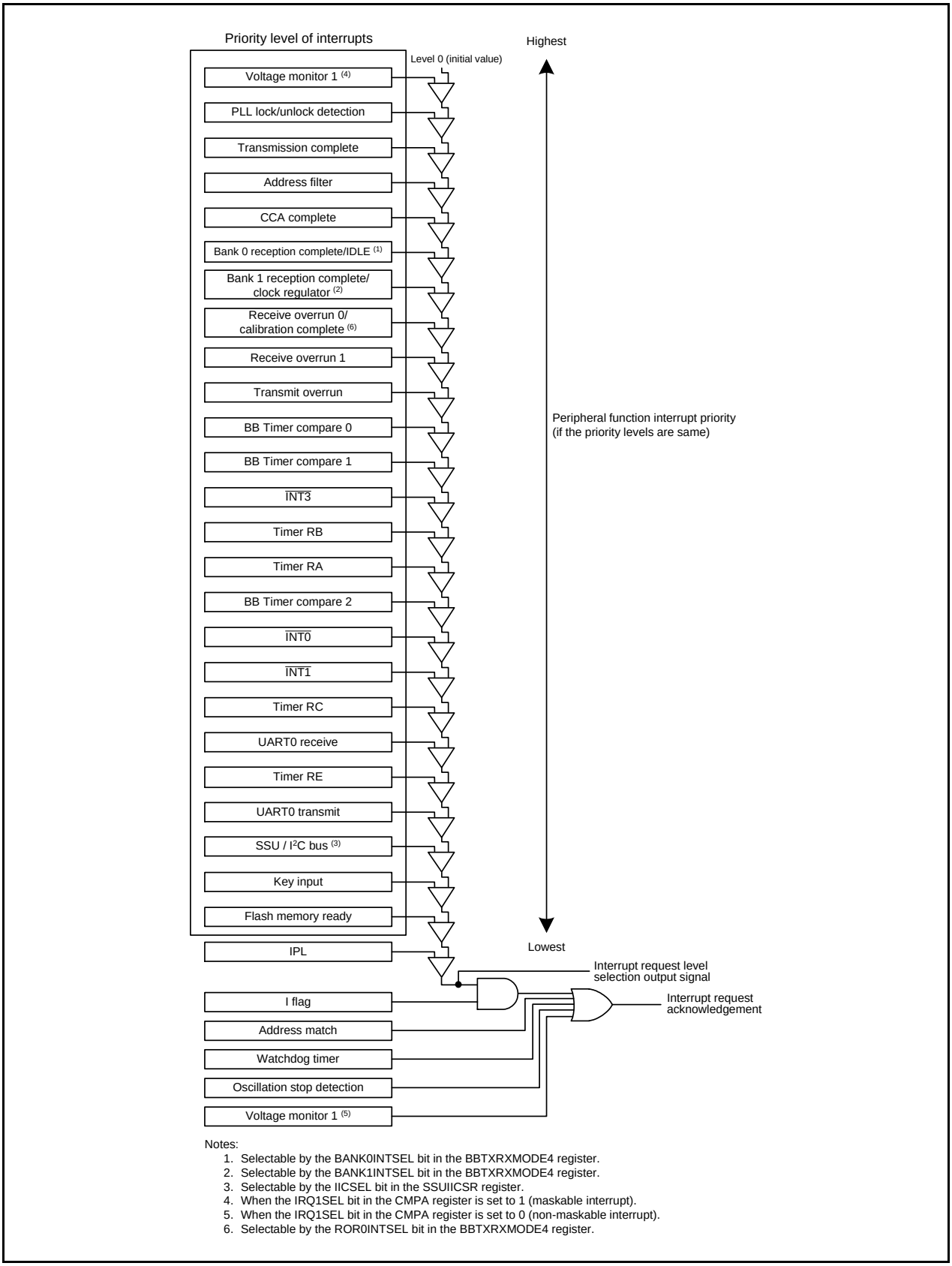


Note:
1. Voltage monitor 1 interrupt is selected when the IRQ1SEL bit in the CMPA register is set to 0 (non-maskable interrupt).

Figure 11.7 Hardware Interrupt Priority

11.3.10 Interrupt Priority Level Selection Circuit

The interrupt priority level selection circuit is used to select the highest priority interrupt.
Figure 11.8 shows the Interrupt Priority Level Selection Circuit.



Notes:
1. Selectable by the BANK0INTSEL bit in the BBTXRXMODE4 register.
2. Selectable by the BANK1INTSEL bit in the BBTXRXMODE4 register.
3. Selectable by the IICSEL bit in the SSUIICSR register.
4. When the IRQ1SEL bit in the CMPA register is set to 1 (maskable interrupt).
5. When the IRQ1SEL bit in the CMPA register is set to 0 (non-maskable interrupt).
6. Selectable by the ROR0INTSEL bit in the BBTXRXMODE4 register.

Figure 11.8 Interrupt Priority Level Selection Circuit

11.4 $\overline{\text{INT}}$ Interrupt

11.4.1 $\overline{\text{INTi}}$ Interrupt (i = 0, 1, 3)

The $\overline{\text{INTi}}$ interrupt is generated by an $\overline{\text{INTi}}$ input. To use the $\overline{\text{INTi}}$ interrupt, set the INTiEN bit in the INTEN register is to 1 (enabled). The edge polarity is selected using the INTiPL bit in the INTEN register and the POL bit in the INTiIC register. The input pin used as the $\overline{\text{INT1}}$ input can be selected.
Also, inputs can be passed through a digital filter with three different sampling clocks.
The $\overline{\text{INT0}}$ pin is shared with the pulse output forced cutoff input of timer RC, and the external trigger input of timer RB.
Table 11.7 lists the Pin Configuration of $\overline{\text{INT}}$ Interrupt.

Table 11.7 Pin Configuration of $\overline{\text{INT}}$ Interrupt

Pin Name	Assigned Pin	I/O	Function
$\overline{\text{INT0}}$	P4_5	Input	$\overline{\text{INT0}}$ interrupt input, timer RB external trigger input, and timer RC pulse output forced cutoff input
$\overline{\text{INT1}}$	P1_5 or P1_7	Input	$\overline{\text{INT1}}$ interrupt input
$\overline{\text{INT3}}$	P3_3	Input	$\overline{\text{INT3}}$ interrupt input

11.4.2 INT Interrupt Input Pin Select Register (INTSR)

Address 018Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INT1SEL2	INT1SEL1	INT1SEL0	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	INT1SEL0	$\overline{\text{INT1}}$ pin select bit	b3 b2 b1 0 0 0: P1_7 assigned 0 0 1: P1_5 assigned Other than above: Do not set.	R/W
b2	INT1SEL1			R/W
b3	INT1SEL2			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

The INTSR register selects which pin is assigned to the $\overline{\text{INT1}}$ input. To use $\overline{\text{INT1}}$, set this register.
Set the INTSR register before setting the $\overline{\text{INT1}}$ associated registers. Also, do not change the setting values in this register during $\overline{\text{INT1}}$ operation.

11.4.3 External Input Enable Register 0 (INTEN)

Address 01FAh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3PL	INT3EN	—	—	INT1PL	INT1EN	INT0PL	INT0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0EN	$\overline{\text{INT0}}$ input enable bit	0: Disabled 1: Enabled	R/W
b1	INT0PL	$\overline{\text{INT0}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b2	INT1EN	$\overline{\text{INT1}}$ input enable bit	0: Disabled 1: Enabled	R/W
b3	INT1PL	$\overline{\text{INT1}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	INT3EN	$\overline{\text{INT3}}$ input enable bit	0: Disabled 1: Enabled	R/W
b7	INT3PL	$\overline{\text{INT3}}$ input polarity select bit (1, 2)	0: One edge 1: Both edges	R/W

Notes:
1. To set the INTiPL bit (i = 0, 1, 3) to 1 (both edges), set the POL bit in the INTiIC register to 0 (falling edge selected).
2. The IR bit in the INTiIC register may be set to 1 (interrupt requested) if the INTEN register is rewritten. Refer to **11.9.4 Changing Interrupt Sources**.

11.4.4 INT Input Filter Select Register 0 (INTF)

Address 01FCh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	INT3F1	INT3F0	—	—	INT1F1	INT1F0	INT0F1	INT0F0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	INT0F0	$\overline{\text{INT0}}$ input filter select bit	b1 b0 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b1	INT0F1			R/W
b2	INT1F0	$\overline{\text{INT1}}$ input filter select bit	b3 b2 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b3	INT1F1			R/W
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	INT3F0	$\overline{\text{INT3}}$ input filter select bit	b7 b6 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b7	INT3F1			R/W

11.4.5 $\overline{\text{INTi}}$ Input Filter (i = 0, 1, 3)

The $\overline{\text{INTi}}$ input contains a digital filter. The sampling clock is selected using bits INTiF1 and INTiF0 in registers INTF. The $\overline{\text{INTi}}$ level is sampled every sampling clock cycle and if the sampled input level matches three times, the IR bit in the INTiIC register is set to 1 (interrupt requested).
Figure 11.9 shows the $\overline{\text{INTi}}$ Input Filter Configuration. Figure 11.10 shows an Operating Example of $\overline{\text{INTi}}$ Input Filter.

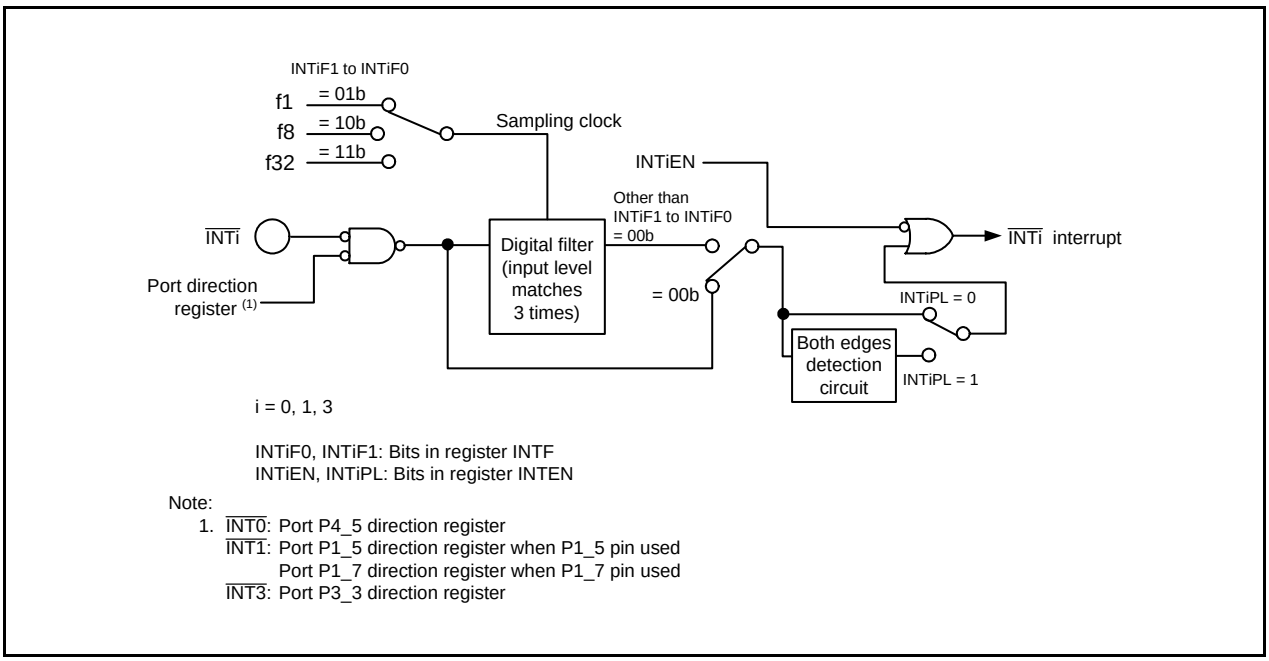


Figure 11.9 $\overline{\text{INTi}}$ Input Filter Configuration

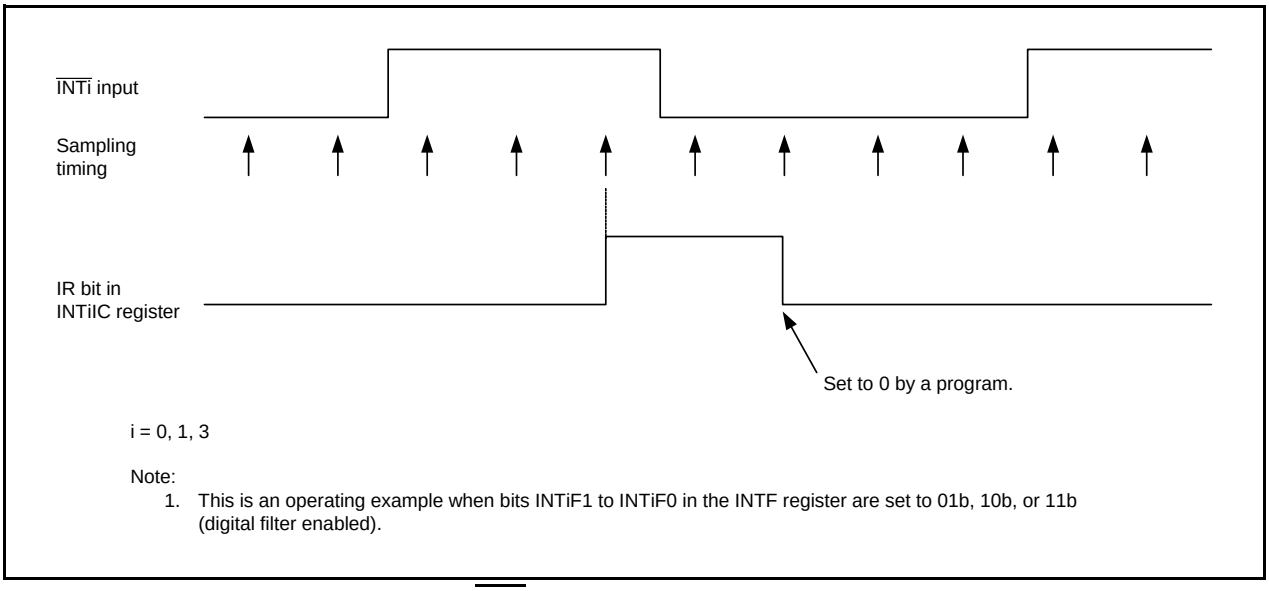


Figure 11.10 Operating Example of $\overline{\text{INTi}}$ Input Filter

11.5 Key Input Interrupt

A key input interrupt request is generated by one of the input edges of pins $\overline{KI0}$ to $\overline{KI7}$. The key input interrupt can be used as a key-on wake-up function to exit wait or stop mode.

The KIiEN bit (i = 0 to 3) in the KIEN register and the KIiEN bit (i = 4 to 7) in the KIEN1 register are used to select whether or not the pins are used as the $\overline{KIi}$ input.

Also, the KIiPL bit (i = 0 to 3) in the KIEN register and the KIiP bit (i = 4 to 7) in the KIEN1 register are used to select the input polarity.

When inputting "L" to the $\overline{KIi}$ pin, which sets the KIiPL bit to 0 (falling edge), the input to the other pins $\overline{KI0}$ to $\overline{KI7}$ is not detected as interrupts. When inputting "H" to the $\overline{KIi}$ pin, which sets the KIiPL bit to 1 (rising edge), the input to the other pins $\overline{KI0}$ to $\overline{KI7}$ is not also detected as interrupts.

Figure 11.11 shows a Block Diagram of Key Input Interrupt. Table 11.8 lists the Pin Configuration of Key Input Interrupt.

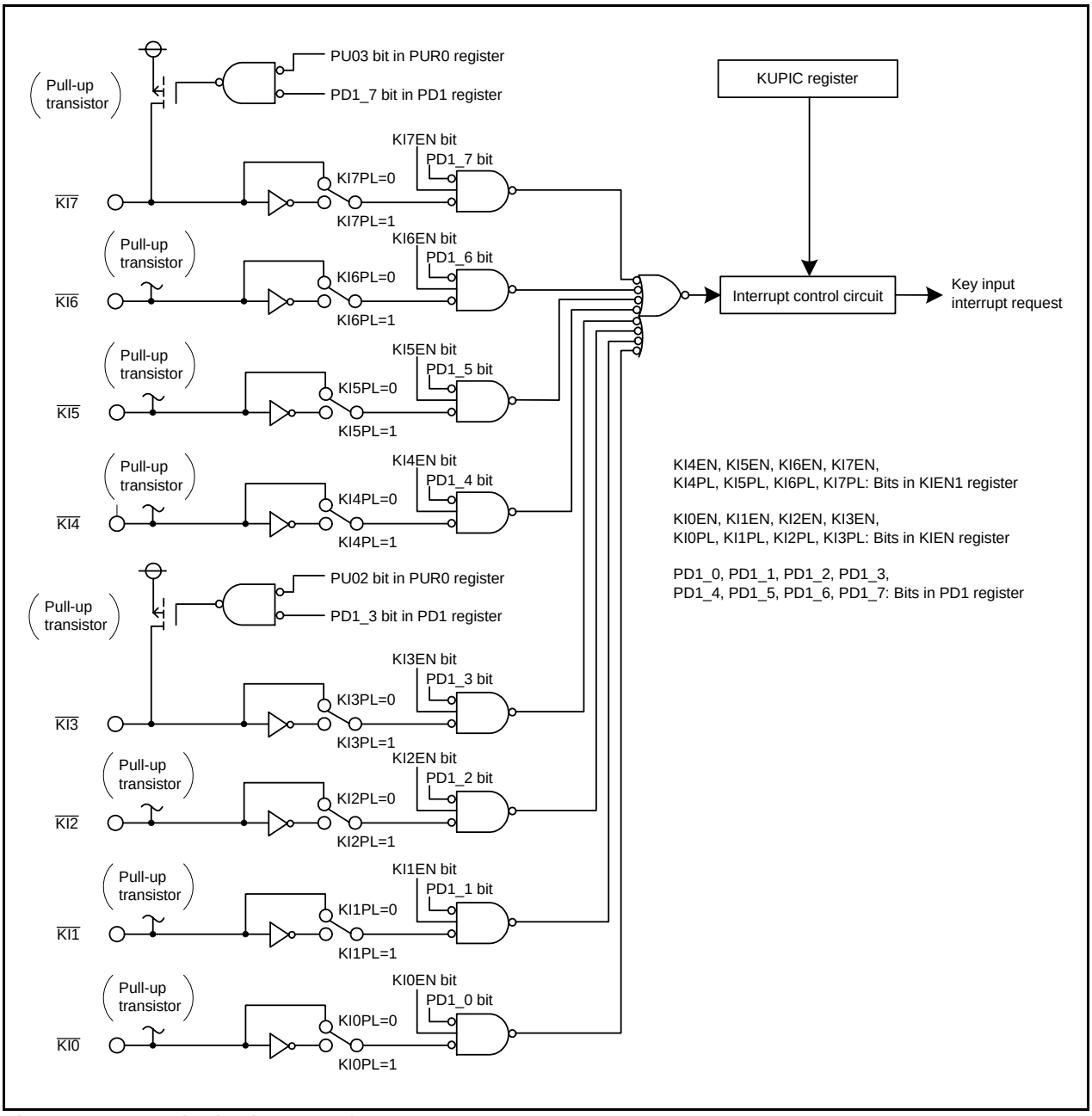


Figure 11.11 Block Diagram of Key Input Interrupt

Table 11.8 Pin Configuration of Key Input Interrupt

Pin Name	I/O	Function
$\overline{KI0}$	Input	$\overline{KI0}$ interrupt input
$\overline{KI1}$	Input	$\overline{KI1}$ interrupt input
$\overline{KI2}$	Input	$\overline{KI2}$ interrupt input
$\overline{KI3}$	Input	$\overline{KI3}$ interrupt input
$\overline{KI4}$	Input	$\overline{KI4}$ interrupt input
$\overline{KI5}$	Input	$\overline{KI5}$ interrupt input
$\overline{KI6}$	Input	$\overline{KI6}$ interrupt input
$\overline{KI7}$	Input	$\overline{KI7}$ interrupt input

11.5.1 Key Input Enable Register 0 (KIEN)

Address 01FFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI3PL	KI3EN	KI2PL	KI2EN	KI1PL	KI1EN	KI0PL	KI0EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI0EN	KI0 input enable bit	0: Disabled 1: Enabled	R/W
b1	KI0PL	KI0 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b2	KI1EN	KI1 input enable bit	0: Disabled 1: Enabled	R/W
b3	KI1PL	KI1 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	KI2EN	KI2 input enable bit	0: Disabled 1: Enabled	R/W
b5	KI2PL	KI2 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b6	KI3EN	KI3 input enable bit	0: Disabled 1: Enabled	R/W
b7	KI3PL	KI3 input polarity select bit	0: Falling edge 1: Rising edge	R/W

The IR bit in the KUPIC register may be set to 1 (interrupt requested) when the KIEN register is rewritten. Refer to **11.9.4 Changing Interrupt Sources**.

11.5.2 Key Input Enable Register 1 (KIEN1)

Address 01FEh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	KI7PL	KI7EN	KI6PL	KI6EN	KI5PL	KI5EN	KI4PL	KI4EN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	KI4EN	KI4 input enable bit	0: Disabled 1: Enabled	R/W
b1	KI4PL	KI4 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b2	KI5EN	KI5 input enable bit	0: Disabled 1: Enabled	R/W
b3	KI5PL	KI5 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b4	KI6EN	KI6 input enable bit	0: Disabled 1: Enabled	R/W
b5	KI6PL	KI6 input polarity select bit	0: Falling edge 1: Rising edge	R/W
b6	KI7EN	KI7 input enable bit	0: Disabled 1: Enabled	R/W
b7	KI7PL	KI7 input polarity select bit	0: Falling edge 1: Rising edge	R/W

The IR bit in the KUPIC register may be set to 1 (interrupt requested) when the KIEN1 register is rewritten. Refer to **11.9.4 Changing Interrupt Sources**.

11.6 Address Match Interrupt

An address match interrupt request is generated immediately before execution of the instruction at the address indicated by the RMADi register (i = 0 or 1). This interrupt is used as a break function by the debugger. When the on-chip debugger is used, do not set an address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1, and fixed vector tables) in the user system.

Set the starting address of any instruction in the RMADi register (i = 0 or 1). The AIERi0 bit in the AIERi register can be used to select enable or disable the interrupt. The address match interrupt is not affected by the I flag and IPL.

The PC value (refer to **11.3.7 Saving Registers**) which is saved on the stack when an address match interrupt request is acknowledged varies depending on the instruction at the address indicated by the RMADi register. (The appropriate return address is not saved on the stack.) When returning from the address match interrupt, follow one of the following means:

- Rewrite the contents of the stack and use the REIT instruction to return.
- Use an instruction such as POP to restore the stack to its previous state before the interrupt request was acknowledged. Then use a jump instruction to return.

Table 11.9 lists the PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged. Table 11.10 lists the Correspondence Between Address Match Interrupt Sources and Associated Registers.

Table 11.9 PC Value Saved on Stack When Address Match Interrupt Request is Acknowledged

Address Indicated by RMADi Register (i = 0 or 1)	PC Value Saved (1)
• Instruction with 2-byte operation code (2) • Instruction with 1-byte operation code (2) ADD.B:S #IMM8,dest SUB.B:S #IMM8,dest AND.B:S #IMM8,dest OR.B:S #IMM8,dest MOV.B:S #IMM8,dest STZ #IMM8,dest STNZ #IMM8,dest STZX #IMM81,#IMM82,dest CMP.B:S #IMM8,dest PUSHM src POPM dest JMPS #IMM8 JSRS #IMM8 MOV.B:S #IMM,dest (however, dest = A0 or A1)	Address indicated by RMADi register + 2
Instructions other than above	Address indicated by RMADi register + 1

Notes:
1. Refer to **11.3.7 Saving Registers**.
2. Operation code: Refer to the **R8C/Tiny Series Software Manual** (REJ09B0001). **Chapter 4. Instruction Code/Number of Cycles** contains diagrams showing operation code below each syntax. Operation code is shown in the bold frame in the diagrams.

Table 11.10 Correspondence Between Address Match Interrupt Sources and Associated Registers

Address Match Interrupt Source	Address Match Interrupt Enable Bit	Address Match Interrupt Register
Address match interrupt 0	AIER00	RMAD0
Address match interrupt 1	AIER10	RMAD1

11.6.1 Address Match Interrupt Enable Register i (AIERi) (i = 0 or 1)

Address 01C3h (AIER0), 01C7h (AIER1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	AIER00	AIER0 register
After Reset	0	0	0	0	0	0	0	0	

Symbol	—	—	—	—	—	—	—	AIER10	AIER1 register
After Reset	0	0	0	0	0	0	0	0	

Bit	Symbol	Bit Name	Function	R/W
b0	AIERi0	Address match interrupt i enable bit	0: Disabled 1: Enabled	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

11.6.2 Address Match Interrupt Register i (RMADi) (i = 0 or 1)

Address 01C2h to 01C0h (RMAD0), 01C6h to 01C4h (RMAD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b23	b22	b21	b20	b19	b18	b17	b16
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	X	X	X	X

Bit	Symbol	Function	Setting Range	R/W
b19 to b0	—	Address setting register for address match interrupt	00000h to FFFFFh	R/W
b20	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b21	—			
b22	—			
b23	—			

11.7 Timer RC Interrupt, Synchronous Serial Communication Unit Interrupt, I²C bus Interface Interrupt, and Flash Memory Interrupt (Interrupts with Multiple Interrupt Request Sources)

The timer RC interrupt, synchronous serial communication unit interrupt, I²C bus interface interrupt, and flash memory interrupt each have multiple interrupt request sources. An interrupt request is generated by the logical OR of several interrupt request sources and is reflected in the IR bit in the corresponding interrupt control register. Therefore, each of these peripheral functions has its own interrupt request source status register (status register) and interrupt request source enable register (enable register) to control the generation of interrupt requests (change of the IR bit in the interrupt control register). Table 11.11 lists the Registers Associated with Timer RC Interrupt, Synchronous Serial Communication Unit Interrupt, I²C bus Interface Interrupt, and Flash Memory Interrupt.

Table 11.11 Registers Associated with Timer RC Interrupt, Synchronous Serial Communication Unit Interrupt, I²C bus Interface Interrupt, and Flash Memory Interrupt

Peripheral Function Name	Status Register of Interrupt Request Source	Enable Register of Interrupt Request Source	Interrupt Control Register
Timer RC	TRCSR	TRCIER	TRCIC
Synchronous serial communication unit	SSSR	SSER	SSUIC
I²C bus interface	ICSR	ICIER	IICIC
Flash memory	RDYSTI	RDYSTIE	FMRDYIC
	BSYAEI	BSYAEIE	
		CMDERIE	

As with other maskable interrupts, the timer RC interrupt, synchronous serial communication unit interrupt, I²C bus interface interrupt, and flash memory interrupt are controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, since each interrupt source is generated by a combination of multiple interrupt request sources, the following differences from other maskable interrupts apply:

- When bits in the enable register are set to 1 and the corresponding bits in the status register are set to 1 (interrupt enabled), the IR bit in the interrupt control register is set to 1 (interrupt requested).
- When either bits in the status register or the corresponding bits in the enable register, or both are set to 0, the IR bit is set to 0 (no interrupt requested).
  That is, even if the interrupt is not acknowledged after the IR bit is set to 1, the interrupt request will not be retained.
  Also, the IR bit is not set to 0 even if 0 is written to this bit.
- Individual bits in the status register are not automatically set to 0 even if the interrupt is acknowledged.
  The IR bit is also not automatically set to 0 when the interrupt is acknowledged.
  Set individual bits in the status register to 0 in the interrupt routine. Refer to the status register figure for how to set individual bits in the status register to 0.
- When multiple bits in the enable register are set to 1 and other request sources are generated after the IR bit is set to 1, the IR bit remains 1.
- When multiple bits in the enable register are set to 1, use the status register to determine which request source causes an interrupt.

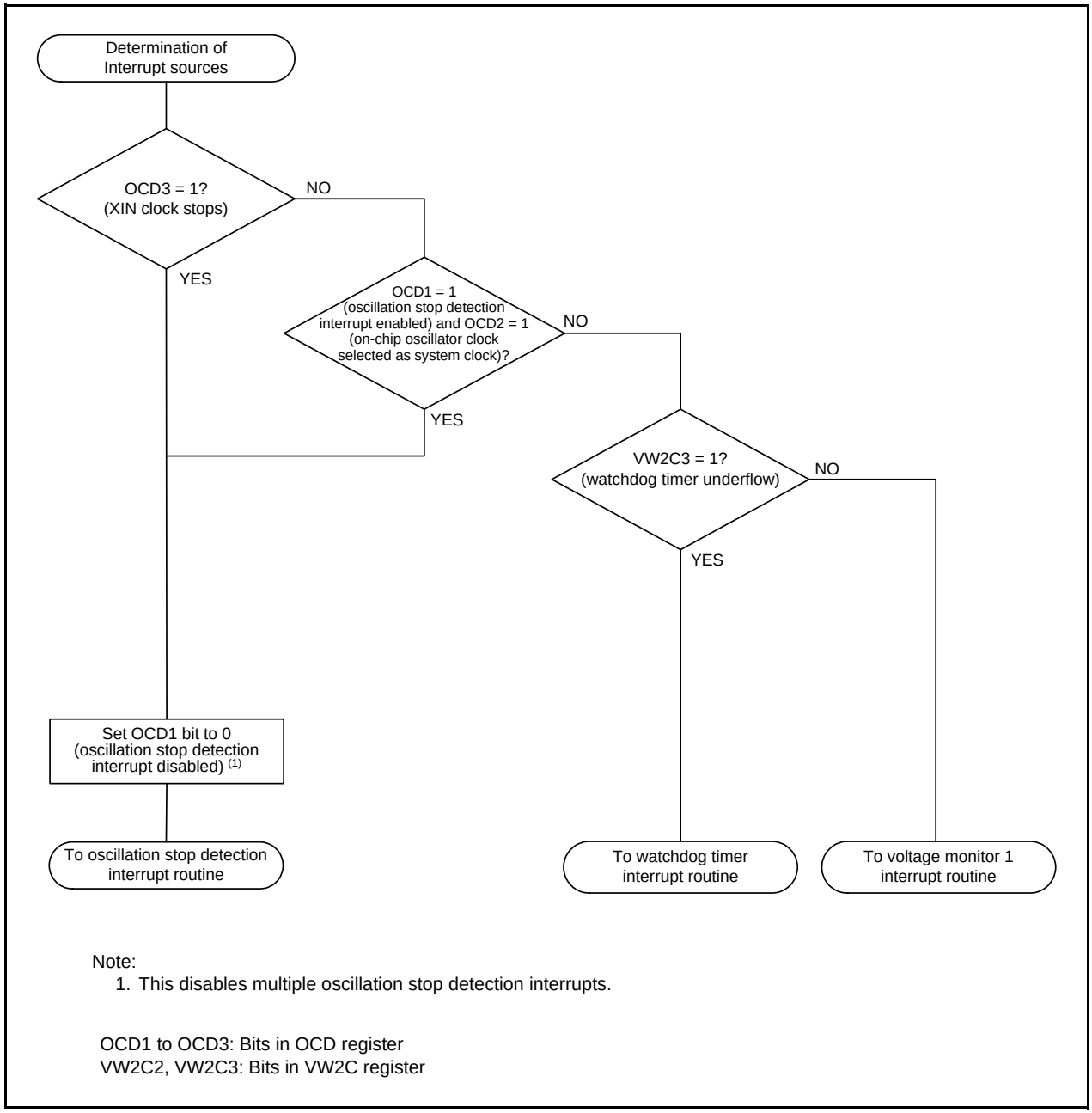
Refer to chapters of the individual peripheral functions (**19. Timer RC**, **23. Synchronous Serial Communication Unit (SSU)**, **24. I²C bus Interface**, and **26. Flash Memory**) for the status register and enable register.
For the interrupt control register, refer to **11.3 Interrupt Control**.

11.8 How to Determine Interrupt Sources

Table 11.12 lists Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1, and Figure 11.12 shows Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1.

Table 11.12 Determination of Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1

Generated Interrupt Source	Bit Indicating Interrupt Source
Oscillation stop detection ((a) or (b))	(a) OCD3 bit in OCD register = 1
	(b) OCD1 to OCD0 bits in OCD register = 11b and OCD2 bit = 1
Watchdog timer	VW2C3 bit in VW2C register = 1
Voltage monitor 1	VW1C2 bit in VW1C register = 1



Note:
1. This disables multiple oscillation stop detection interrupts.

OCD1 to OCD3: Bits in OCD register
VW2C2, VW2C3: Bits in VW2C register

Figure 11.12 Example of Determining Interrupt Sources for Oscillation Stop Detection, Watchdog Timer, Voltage Monitor 1

11.9 Notes on Interrupts

11.9.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

11.9.2 SP Setting

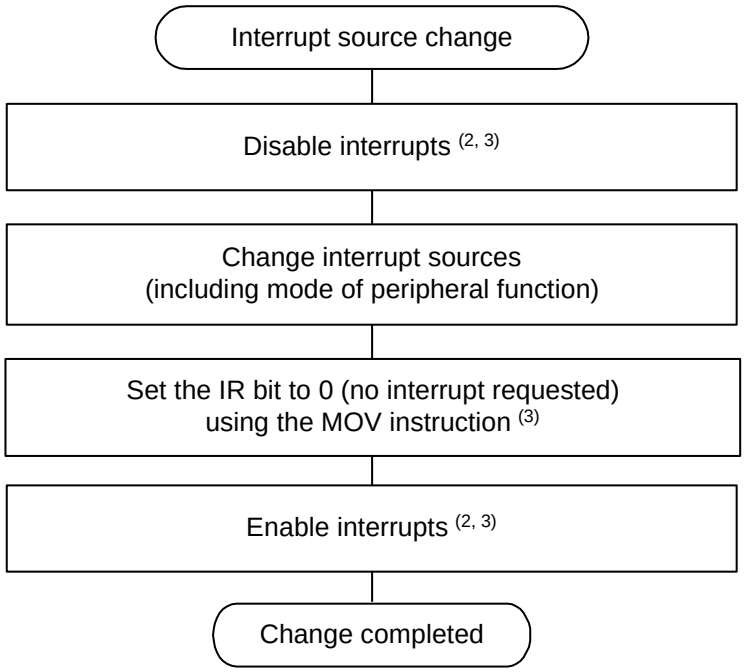
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

11.9.3 External Interrupt and Key Input Interrupt

Either the “L” level width or “H” level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$, regardless of the CPU clock.
For details, refer to **Table 28.17** (VCC = 3 V), **Table 28.21** (VCC = 2.15 V) **External Interrupt $\overline{\text{INTi}}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 7)**.

11.9.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 11.13 shows a Procedure Example for Changing Interrupt Sources.



IR bit: The interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to the input with the digital filter used, wait for three or more cycles of the sampling clock of the digital filter before setting the IR bit to 0 (no interrupt requested). Refer to **11.9.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 11.13 Procedure Example for Changing Interrupt Sources

11.9.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.
Changing any bit other than the IR bit
If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register: AND, OR, BCLR, and BSET.

Changing the IR bit
Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested). Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below. Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    MOV.W   MEM, R0         ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    POPC    FLG             ; Enable interrupts
```

12. ID Code Areas

The ID code areas are used to implement a function that prevents the flash memory from being rewritten in standard serial I/O mode. This function prevents the flash memory from being read, rewritten, or erased.

12.1 Overview

The ID code areas are assigned to 0FFDFh, 0FFE3h, 0FFEBh, 0FFEFh, 0FFF3h, 0FFF7h, and 0FFFBh of the respective vector highest-order addresses of the fixed vector table. Figure 12.1 shows the ID Code Areas.

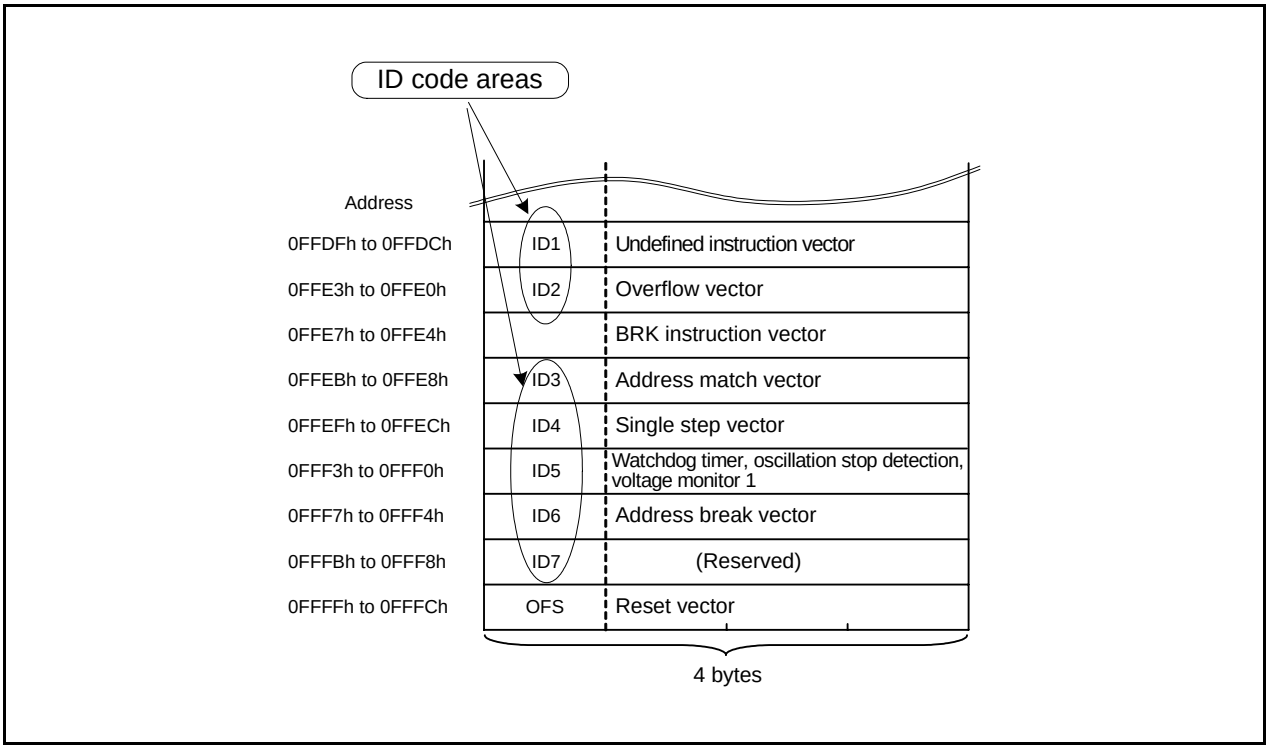


Figure 12.1 ID Code Areas

12.2 Functions

The ID code areas are used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes stored in the ID code areas and the ID codes sent from the serial programmer or the on-chip debugging emulator are checked to see if they match. If the ID codes match, the commands sent from the serial programmer or the on-chip debugging emulator are acknowledged. If the ID codes do not match, the commands are not acknowledged. To use the serial programmer or the on-chip debugging emulator, first write predetermined ID codes to the ID code areas.
If 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes are not checked and all commands are accepted.

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.

The character sequence of the ASCII codes “ALeRASE” is the reserved word used for the forced erase function. The character sequence of the ASCII codes “Protect” is the reserved word used for the standard serial I/O mode disabled function. Table 12.1 shows the ID Code Reserved Word. The reserved word is a set of reserved characters when all the addresses and data in the ID code storage addresses sequentially match Table 12.1. When the forced erase function or standard serial I/O mode disabled function is not used, use another character sequence of the ASCII codes.

Table 12.1 ID Code Reserved Word

ID Code Storage Address		ID Code Reserved Word (ASCII) (1)	
		ALeRASE	Protect
0FFDFh	ID1	41h (upper-case “A”)	50h (upper-case “P”)
0FFE3h	ID2	4Ch (upper-case “L”)	72h (lower-case “r”)
0FFEBh	ID3	65h (lower-case “e”)	6Fh (lower-case “o”)
0FFEFh	ID4	52h (upper-case “R”)	74h (lower-case “t”)
0FFF3h	ID5	41h (upper-case “A”)	65h (lower-case “e”)
0FFF7h	ID6	53h (upper-case “S”)	63h (lower-case “c”)
0FFFBh	ID7	45h (upper-case “E”)	74h (lower-case “t”)

Note:
1. Reserve word: A set of characters when all the addresses and data in the ID code storage addresses sequentially match Table 12.1.

12.3 Forced Erase Function

This function is used in standard serial I/O mode. When the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE” in ASCII code, the content of the user ROM area will be erased at once. However, if the contents of the ID code addresses are set to other than “ALeRASE” (other than **Table 12.1 ID Code Reserved Word**) when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), forced erasure is not executed and the ID codes are checked with the ID code check function. Table 12.2 lists the Conditions and Operations of Forced Erase Function.
Also, when the contents of the ID code addresses are set to “ALeRASE” in ASCII code, if the ID codes sent from the serial programmer or the on-chip debugging emulator are “ALeRASE”, the content of the user ROM area will be erased. If the ID codes sent from the serial programmer are other than “ALeRASE”, the ID codes do not match and no command is acknowledged, thus the user ROM area remains protected.

Table 12.2 Conditions and Operations of Forced Erase Function

Condition			Operation
ID code from serial programmer or the on-chip debugging emulator	ID code in ID code storage address	Bits ROMCP1 and ROMCR in OFS register	
ALeRASE	ALeRASE	—	All erasure of user ROM area (forced erase function)
	Other than ALeRASE (1)	Other than 01b (ROM code protect disabled)	
		01b (ROM code protect enabled)	ID code check (ID code check function)
Other than ALeRASE	ALeRASE	—	ID code check (ID code check function. No ID code match.)
	Other than ALeRASE (1)	—	ID code check (ID code check function)

Note:
1. For “Protect”, refer to **12.4 Standard Serial I/O Mode Disabled Function**.

12.4 Standard Serial I/O Mode Disabled Function

This function is used in standard serial I/O mode. When the I/D codes in the ID code storage addresses are set to the reserved character sequence of the ASCII codes “Protect” (refer to **Table 12.1 ID Code Reserved Word**), communication with the serial programmer or the on-chip debugging emulator is not performed. This does not allow the flash memory to be read, rewritten, or erased using the serial programmer or the on-chip debugging emulator.
Also, if the ID codes are also set to the reserved character sequence of the ASCII codes “Protect” when the ROMCR bit in the OFS register is set to 1 and the ROMCP1 bit is set to 0 (ROM code protect enabled), ROM code protection cannot be disabled using the serial programmer or the on-chip debugging emulator. This prevents the flash memory from being read, rewritten, or erased using the serial programmer, the on-chip debugging emulator, or parallel programmer.

12.5 Notes on ID Code Areas

12.5.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)   ; UND
.lword dummy | (55000000h)   ; INTO
.lword dummy                 ; BREAK
.lword dummy | (55000000h)   ; ADDRESS MATCH
.lword dummy | (55000000h)   ; SET SINGLE STEP
.lword dummy | (55000000h)   ; WDT
.lword dummy | (55000000h)   ; ADDRESS BREAK
.lword dummy | (55000000h)   ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

13. Option Function Select Area

13.1 Overview

The option function select area is used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation. The reset vector highest-order-address, 0FFFFh and 0FFDBh, are assigned as the option function select area. Figure 13.1 shows the Option Function Select Area.

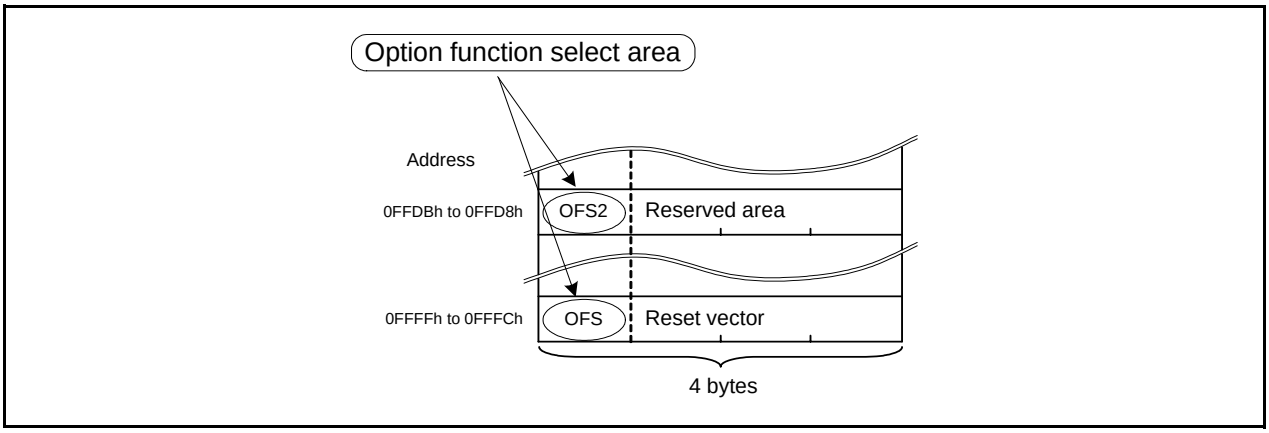


Figure 13.1 Option Function Select Area

13.2 Registers

Registers OFS and OFS2 are used to select the MCU state after a reset, the function to prevent rewriting in parallel I/O mode, or the watchdog timer operation.

13.2.1 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: Do not set. 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   Initial value of OFS register is FFh. The value of OFS register changes as programmed by user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

13.2.2 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Settng Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:
1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   At shipment, the OFS2 register is set to FFh. It is set to the written value after written by the user.

   For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

13.3 Notes on Option Function Select Area

13.3.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)     ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

14. Watchdog Timer

The watchdog timer is a function that detects when a program is out of control. Use of the watchdog timer is recommended to improve the reliability of the system.

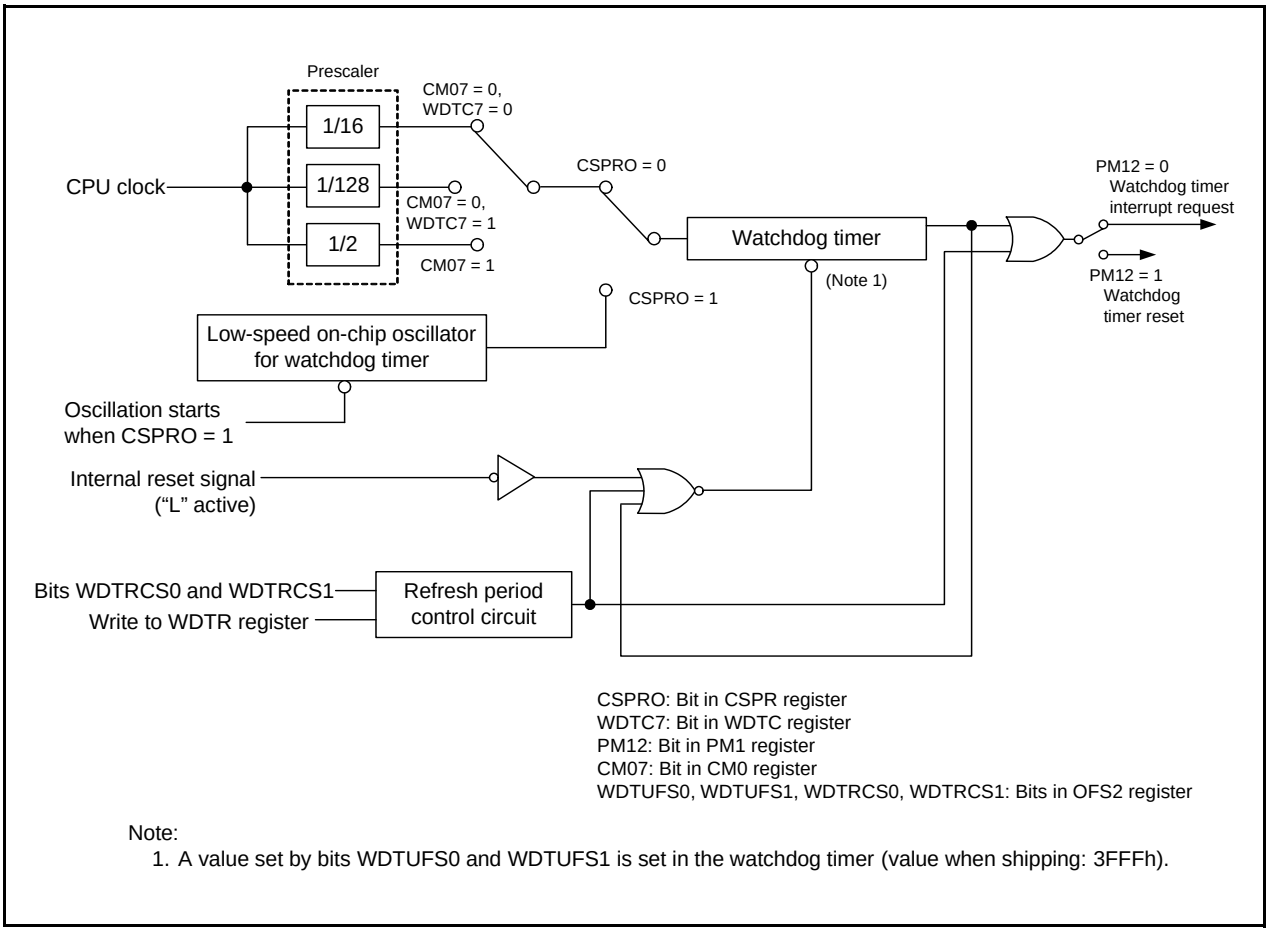
14.1 Overview

The watchdog timer contains a 14-bit counter and allows selection of count source protection mode enable or disable.
Table 14.1 lists the Watchdog Timer Specifications.
Refer to **5.5 Watchdog Timer Reset** for details of the watchdog timer reset.
Figure 14.1 shows a Watchdog Timer Block Diagram.

Table 14.1 Watchdog Timer Specifications

Item	Count Source Protection Mode Disabled	Count Source Protection Mode Enabled
Count source	CPU clock	Low-speed on-chip oscillator clock for the watchdog timer
Count operation	Decrement	
Count start condition	Either of the following can be selected: • After a reset, count starts automatically • Count starts by writing to the WDTS register	
Count stop condition	Stop mode, wait mode	None
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register (with acknowledgement period setting) (1) • Underflow	
Operations at underflow	Watchdog timer interrupt or watchdog timer reset	Watchdog timer reset
Selectable functions	• Division ratio of the prescaler Selected by the WDTC7 bit in the WDTC register or the CM07 bit in the CM0 register. • Count source protection mode Whether count source protection mode is enabled or disabled after a reset can be selected by the CSPROINI bit in the OFS register (flash memory). If count source protection mode is disabled after a reset, it can be enabled or disabled by the CSPRO bit in the CSPR register (program). • Start or stop of the watchdog timer after a reset Selected by the WDTON bit in the OFS register (flash memory). • Initial value of the watchdog timer Selectable by bits WDTUFS0 and WDTUFS1 in the OFS2 register. • Refresh acknowledgement period for the watchdog timer Selectable by bits WDTRCS0 and WDTRCS1 in the OFS2 register.	

Note:
1. Write the WDTR register during the count operation of the watchdog timer.



Note:
1. A value set by bits WDTUFS0 and WDTUFS1 is set in the watchdog timer (value when shipping: 3FFFh).

Figure 14.1 Watchdog Timer Block Diagram

14.2 Registers

14.2.1 Processor Mode Register 1 (PM1)

Address 0005h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	PM12	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	PM12	WDT interrupt/reset switch bit	0: Watchdog timer interrupt 1: Watchdog timer reset (1)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—	Reserved bit	Set to 0.	R/W

Note:
1. The PM12 bit is set to 1 when 1 is written by a program (and remains unchanged even if 0 is written to it). This bit is automatically set to 1 when the CSPRO bit in the CSPR register is set to 1 (count source protection mode enabled).

Set the PRC1 bit in the PRCR register to 1 (write enabled) before rewriting the PM1 register.

14.2.2 Watchdog Timer Reset Register (WDTR)

Address 000Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	Writing 00h and then FFh to this register initializes the watchdog timer. The initial value of the watchdog timer is specified by bits WDTUFS0 and WDTUF1 in the OFS2 register. (1)	W

Note:
1. Write the WDTR register during the count operation of the watchdog timer.

14.2.3 Watchdog Timer Start Register (WDTS)

Address 000Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	R/W
b7 to b0	A write instruction to this register starts the watchdog timer.	W

14.2.4 Watchdog Timer Control Register (WDTC)

Address 000Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	WDTC7	—	—	—	—	—	—	—
After Reset	0	0	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	The following bits of the watchdog timer can be read. When bits WDTUFS1 to WDTUFS0 in the OFS2 register are 00b (03FFh): b5 to b0 01b (0FFFh): b7 to b2 10b (1FFFh): b8 to b3 11b (3FFFh): b9 to b4		R
b1	—			R
b2	—			R
b3	—			R
b4	—			R
b5	—			R
b6	—	Reserved bit	When read, the content is 0.	R
b7	WDTC7	Prescaler select bit	0: Divided-by-16 1: Divided-by-128	R/W

14.2.5 Count Source Protection Mode Register (CSPR)

Address 001Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPRO	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is set to 1.

After Reset	1	0	0	0	0	0	0	0

The above applies when the CSPROINI bit in the OFS register is set to 0.

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	CSPRO	Count source protection mode select bit (1)	0: Count source protection mode disabled 1: Count source protection mode enabled	R/W

Note:
1. To set the CSPRO bit to 1, write 0 and then 1 to it. This bit cannot be set to 0 by a program. Disable interrupts and DTC activation between writing 0 and writing 1.

14.2.6 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: Do not set. 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   Initial value of OFS register is FFh. The value of OFS register changes as programmed by user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

14.2.7 Option Function Select Register 2 (OFS2)

Address 0FFDBh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	WDTRCS1	WDTRCS0	WDTUFS1	WDTUFS0
After Reset	User Settng Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTUFS0	Watchdog timer underflow period set bit	b1 b0 0 0: 03FFh 0 1: 0FFFh 1 0: 1FFFh 1 1: 3FFFh	R/W
b1	WDTUFS1			R/W
b2	WDTRCS0	Watchdog timer refresh acknowledgement period set bit	b3 b2 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100%	R/W
b3	WDTRCS1			R/W
b4	—	Reserved bits	Set to 1.	R/W
b5	—			
b6	—			
b7	—			

Note:

1. The OFS2 register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS2 register. If the block including the OFS2 register is erased, the OFS2 register is set to FFh.
   At shipment, the OFS2 register is set to FFh. It is set to the written value after written by the user.

   For a setting example of the OFS2 register, refer to **13.3.1 Setting Example of Option Function Select Area**.

Bits WDTRCS0 and WDTRCS1 (Watchdog Timer Refresh Acknowledgement Period Set Bit)

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, the refresh acknowledgement period for the watchdog timer can be selected.
For details, refer to **14.3.1.1 Refresh Acknowledgment Period**.

14.3 Functional Description

14.3.1 Common Items for Multiple Modes

14.3.1.1 Refresh Acknowledgment Period

The period for acknowledging refreshment operation to the watchdog timer (write to the WDTR register) can be selected by bits WDTRCS0 and WDTRCS1 in the OFS2 register. Figure 14.2 shows the Refresh Acknowledgement Period for Watchdog Timer.

Assuming that the period from when the watchdog timer starts counting until it underflows is 100%, a refresh operation executed during the refresh acknowledgement period is acknowledged. Any refresh operation executed during the period other than the above is processed as an incorrect write, and a watchdog timer interrupt or watchdog timer reset (selectable by the PM12 bit in the PM1 register) is generated.

Do not execute any refresh operation while the count operation of the watchdog timer is stopped.

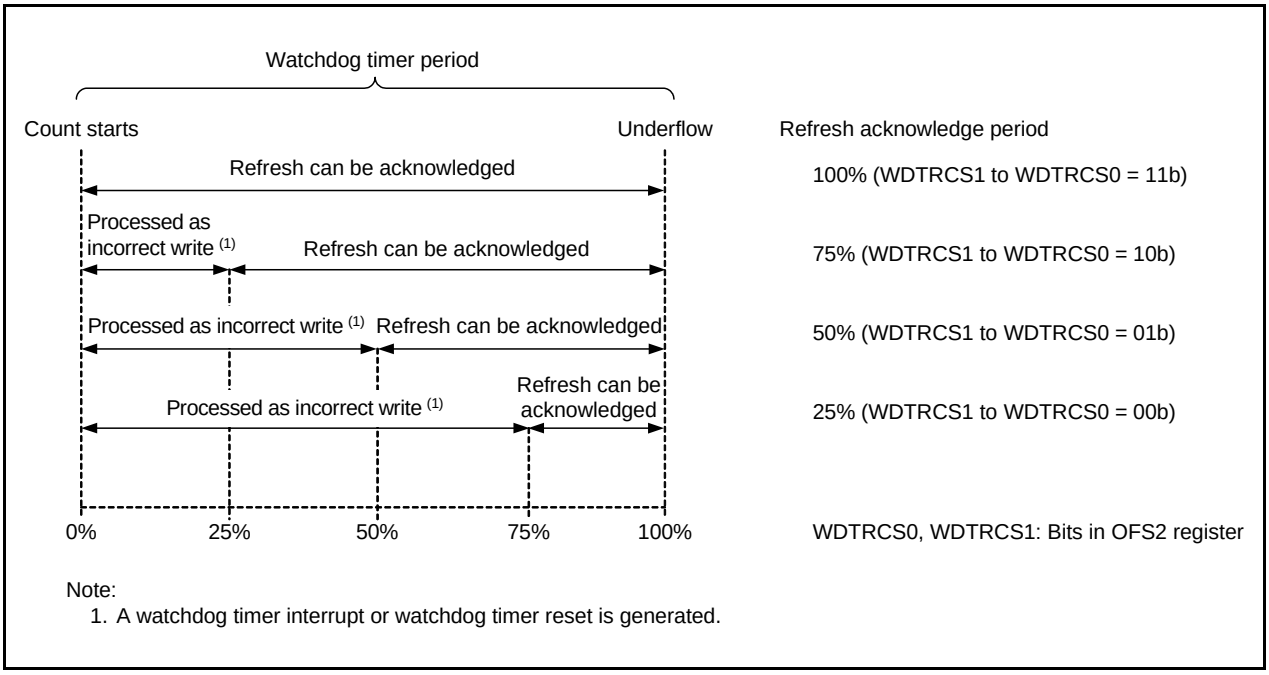


Figure 14.2 Refresh Acknowledgement Period for Watchdog Timer

14.3.2 Count Source Protection Mode Disabled

The count source for the watchdog timer is the CPU clock when count source protection mode is disabled. Table 14.2 lists the Watchdog Timer Specifications (Count Source Protection Mode Disabled).

Table 14.2 Watchdog Timer Specifications (Count Source Protection Mode Disabled)

Item	Specification
Count source	CPU clock
Count operation	Decrement
Period	$\frac{\text{Division ratio of prescaler (n)} \times \text{count value of watchdog timer (m)}}{\text{CPU clock}}$ (1) n: 16 or 128 (selected by the WDTC7 bit in the WDTC register), or 2 when selecting the low-speed clock (CM07 bit in CM0 register = 1) m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 16.38 ms when: - The CPU clock frequency is set to 16 MHz. - The prescaler is divided by 16. - Bits WDTUFS1 to WDTUFS0 are set to 11b (3FFFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register. (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (2) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset) The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset) The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	Stop mode, wait mode (Count resumes from the retained value after exiting.)
Operations at underflow	• When the PM12 bit in the PM1 register is set to 0 Watchdog timer interrupt • When the PM12 bit in the PM1 register is set to 1 Watchdog timer reset (refer to **5.5 Watchdog Timer Reset**)

Notes:
1. The watchdog timer is initialized when 00h and then FFh is written to the WDTR register. The prescaler is initialized after a reset. This may cause some errors due to the prescaler during the watchdog timer period.
2. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

14.3.3 Count Source Protection Mode Enabled

The count source for the watchdog timer is the low-speed on-chip oscillator clock for the watchdog timer when count source protection mode is enabled. If the CPU clock stops when a program is out of control, the clock can still be supplied to the watchdog timer.
Table 14.3 lists the Watchdog Timer Specifications (Count Source Protection Mode Enabled).

Table 14.3 Watchdog Timer Specifications (Count Source Protection Mode Enabled)

Item	Specification
Count source	Low-speed on-chip oscillator clock
Count operation	Decrement
Period	$\frac{\text{Count value of watchdog timer (m)}}{\text{Low-speed on-chip oscillator clock for the watchdog timer}}$ m: Value set by bits WDTUFS0 and WDTUFS1 in the OFS2 register Example: The period is approximately 8.2 ms when: - The on-chip oscillator clock for the watchdog timer is set to 125 kHz. - Bits WDTUFS1 to WDTUFS0 are set to 00b (03FFh).
Watchdog timer initialization conditions	• Reset • Write 00h and then FFh to the WDTR register (3) • Underflow
Count start conditions	The operation of the watchdog timer after a reset is selected by the WDTON bit (1) in the OFS register (address 0FFFFh). • When the WDTON bit is set to 1 (watchdog timer is stopped after reset) The watchdog timer and prescaler are stopped after a reset and start counting when the WDTS register is written to. • When the WDTON bit is set to 0 (watchdog timer starts automatically after reset) The watchdog timer and prescaler start counting automatically after a reset.
Count stop condition	None (Count does not stop even in wait mode and stop mode once it starts)
Operation at underflow	Watchdog timer reset (refer to **5.5 Watchdog Timer Reset**)
Registers, bits	• When the CSPPRO bit in the CSPR register is set to 1 (count source protection mode enabled) (2), the following are set automatically: - The low-speed on-chip oscillator for the watchdog timer is on. - The PM12 bit in the PM1 register is set to 1 (watchdog timer reset when the watchdog timer underflows).

Notes:
1. The WDTON bit cannot be changed by a program. To set this bit, write 0 to bit 0 of address 0FFFFh with a flash programmer.
2. Even if 0 is written to the CSPROINI bit in the OFS register, the CSPRO bit is set to 1. The CSPROINI bit cannot be changed by a program. To set this bit, write 0 to bit 7 of address 0FFFFh with a flash programmer.
3. Write the WDTR register during the count operation of the watchdog timer.

15. DTC

The DTC (data transfer controller) is a function that transfers data between the SFR and on-chip memory without using the CPU. This chip incorporates one DTC channel. The DTC is activated by a peripheral function interrupt to perform data transfers. The DTC and CPU use the same bus, and the DTC takes priority over the CPU in using the bus.
To control DTC data transfers, control data comprised of a transfer source address, a transfer destination address, and operating modes are allocated in the DTC control data area. Each time the DTC is activated, the DTC reads control data to perform data transfers.

15.1 Overview

Table 15.1 shows the DTC Specifications.

Table 15.1 DTC Specifications

Item		Specification
Activation sources		17 sources
Allocatable control data		24 sets
Address space which can be transferred		64 Kbytes (00000h to 0FFFFh)
Maximum number of transfer times	Normal mode	256 times
	Repeat mode	255 times
Maximum size of block to be transferred	Normal mode	256 bytes
	Repeat mode	255 bytes
Unit of transfers		Byte
Transfer mode	Normal mode	Transfers end on completion of the transfer causing the DTCCTj register value to change from 1 to 0.
	Repeat mode	On completion of the transfer causing the DTCCTj register value to change from 1 to 0, the repeat area address is initialized and the DTRLDj register value is reloaded to the DTCCTj register to continue transfers.
Address control	Normal mode	Fixed or incremented
	Repeat mode	Addresses of the area not selected as the repeat area are fixed or incremented.
Priority of activation sources		Refer to **Table 15.5 DTC Activation Sources and DTC Vector Addresses**.
Interrupt request	Normal mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed, the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the data transfer.
	Repeat mode	When the data transfer causing the DTCCTj register value to change from 1 to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), the activation source interrupt request is generated for the CPU, and interrupt handling is performed on completion of the transfer.
Transfer start		When bits DTCENi0 to DTCENi7 in the DTCENi registers are 1 (activation enabled), data transfer is started each time the corresponding DTC activation sources are generated.
Transfer stop	Normal mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed.
	Repeat mode	• When bits DTCENi0 to DTCENi7 are set to 0 (activation disabled). • When the data transfer causing the DTCCTj register value to change from 1 to 0 is completed while the RPTINT bit is 1 (interrupt generation enabled).

i = 0 to 3, 5, 6, j = 0 to 23

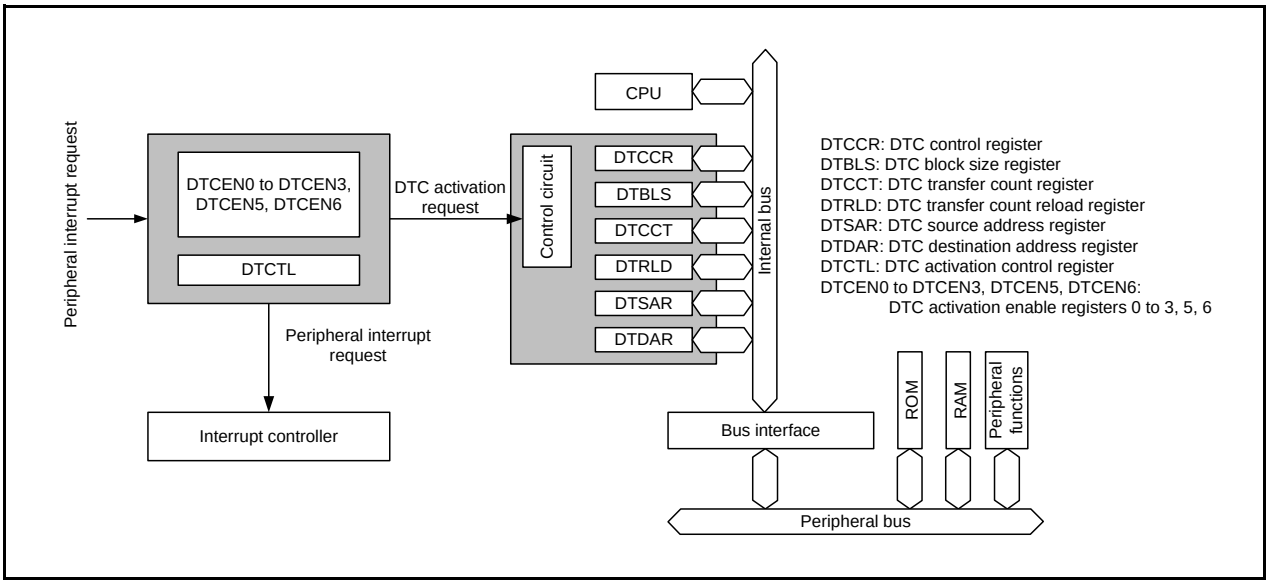


Figure 15.1 DTC Block Diagram

15.2 Registers

When the DTC is activated, control data (DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj, j = 0 to 23) allocated in the control data area is read, and then transferred to the control registers (DTCCR, DTBLS, DTCCT, DTRLD, DTSAR, and DTDAR) in the DTC. On completion of the DTC data transfer, the contents of the DTC control registers are written back to the control data area.

Each DTCCR, DTBLS, DTCCT, DTRLD, DTSAR, and DTDAR register cannot be directly read or written to. DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj are allocated as control data at addresses from 2C40h to 2CFFh in the DTC control data area, and can be directly accessed.
Also, registers DTCTL and DTCENi (i = 0 to 3, 5, 6) can be directly accessed.

15.2.1 DTC Control Register j (DTCCRj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RPTINT	CHNE	DAMOD	SAMOD	RPTSEL	MODE
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	MODE	Transfer mode select bit	0: Normal mode 1: Repeat mode	R/W
b1	RPTSEL	Repeat area select bit (1)	0: Transfer destination is the repeat area 1: Transfer source is the repeat area	R/W
b2	SAMOD	Source address control bit (2)	0: Fixed 1: Incremented	R/W
b3	DAMOD	Destination address control bit (2)	0: Fixed 1: Incremented	R/W
b4	CHNE	Chain transfer enable bit (3)	0: Chain transfers disabled 1: Chain transfers enabled	R/W
b5	RPTINT	Repeat mode interrupt enable bit (1)	0: Interrupt generation disabled 1: Interrupt generation enabled	R/W
b6	—	Reserved bits	Set to 0.	R/W
b7	—			

Notes:
1. This bit is valid when the MODE bit is 1 (repeat mode).
2. Settings of bits SAMOD and DAMOD are invalid for the repeat area.
3. Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).

15.2.2 DTC Block Size Register j (DTBLSj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the size of the data block to be transferred by one activation.	00h to FFh (1)	R/W

Note:
1. When the DTBLS register is set to 00h, the block size is 256 bytes.

15.2.3 DTC Transfer Count Register j (DTCCTj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	These bits specify the number of times of DTC data transfers.	00h to FFh (1)	R/W

Note:
1. When the DTCCT register is set to 00h, the number of transfer times is 256. Each time the DTC is activated, the DTCCT register is decremented by 1.

15.2.4 DTC Transfer Count Reload Register j (DTRLDj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	This register value is reloaded to the DTCCT register in repeat mode.	00h to FFh (1)	R/W

Note:
1. Set the initial value for the DTCCT register.

15.2.5 DTC Source Address Register j (DTSARj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer source address for data transfer.	0000h to FFFFh	R/W

15.2.6 DTC Destination Address Register j (DTDARj) (j = 0 to 23)

Address Refer to **Table 15.4 Control Data Allocation Addresses**.

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b15 to b0	These bits specify a transfer destination address for data transfer.	0000h to FFFFh	R/W

15.2.7 DTC Activation Enable Register i (DTCENi) (i = 0 to 3, 5, 6)

Address 0088h (DTCEN0), 0089h (DTCEN1), 008Ah (DTCEN2), 008Bh (DTCEN3), 008Dh (DTCEN5), 008Eh (DTCEN6)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DTCENi7	DTCENi6	DTCENi5	DTCENi4	DTCENi3	DTCENi2	DTCENi1	DTCENi0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DTCENi0	DTC activation enable bit (1)	If an interrupt source is assigned: 0: Activation disabled 1: Activation enabled If no interrupt source is assigned: Set to 0 (reserved bit).	R/W
b1	DTCENi1			R/W
b2	DTCENi2			R/W
b3	DTCENi3			R/W
b4	DTCENi4			R/W
b5	DTCENi5			R/W
b6	DTCENi6			R/W
b7	DTCENi7			R/W

i = 0 to 3, 5, 6

Note:

1. For the operation of these bits, refer to **15.3.7 Interrupt Sources**.

The DTCENi registers enable/disable DTC activation by interrupt sources. Table 15.2 shows the Correspondences between Bits DTCENi0 to DTCENi7 (i = 0 to 3, 5, 6) and Interrupt Sources (1).

Table 15.2 Correspondences between Bits DTCENi0 to DTCENi7 (i = 0 to 3, 5, 6) and Interrupt Sources (1)

Register	DTCENi7 Bit	DTCENi6 Bit	DTCENi5 Bit	DTCENi4 Bit	DTCENi3 Bit	DTCENi2 Bit	DTCENi1 Bit	DTCENi0 Bit
DTCEN0	$\overline{\text{INT0}}$	$\overline{\text{INT1}}$	—	$\overline{\text{INT3}}$	—	—	—	—
DTCEN1	Key input	—	UART0 reception	UART0 transmission	—	—	—	—
DTCEN2	SSU/I²C bus receive data full	SSU/I²C bus transmit data empty	—	Voltage Monitor 1	—	—	Timer RC input-capture/ compare-match A	Timer RC input-capture/ compare-match B
DTCEN3	Timer RC input-capture/ compare-match C	Timer RC input-capture/ compare-match D	—	—	—	—	—	—
DTCEN5	—	—	Timer RE	—	—	—	—	—
DTCEN6	—	Timer RA	—	Timer RB	Flash ready status	—	—	—

Note:

1. The bits with no interrupt source assigned are reserved. Set the reserved bits to 0.

15.2.8 DTC Activation Control Register (DTCTL)

Address 0080h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	NMIF	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	NMIF	Non-maskable interrupt generation bit (1)	0: Non-maskable interrupts not generated 1: Non-maskable interrupts generated	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:

1. This bit is set to 0 when the read result is 1 and 0 is written to the same bit. This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. This bit remains unchanged if 1 is written to it.

The DTCTL register controls DTC activation when a non-maskable interrupt (an interrupt by the watchdog timer, oscillation stop detection, voltage monitor 1) is generated.

NMIF Bit (Non-Maskable Interrupt Generation Bit)

The NMIF bit is set to 1 when a watchdog timer interrupt, an oscillation stop detection interrupt, or a voltage monitor 1 interrupt is generated.
When the NMIF bit is 1, the DTC is not activated even if the interrupt which enables DTC activation is generated. If the NMIF bit is changed to 1 during DTC transfer, the transfer is continued until it is completed.

When an interrupt source is the watchdog timer, wait for the following cycles before writing 0 to the NMIF bit:
If the WDTC7 bit in the WDTC register is set to 0 (divide-by-16 using the prescaler), wait for 16 cycles of the CPU clock after the interrupt source is generated.
If the WDTC7 bit is set to 1 (divide-by-128 using the prescaler), wait for 128 cycles of the CPU clock after the interrupt source is generated.
When an interrupt source is oscillation stop detection, set to the OCD1 bit in the OCD register to 0 (oscillation stop detection interrupt disabled) before writing 0 to the NMIF bit.

15.3 Function Description

15.3.1 Overview

When the DTC is activated, control data is read from the DTC control data area to perform data transfers and control data after data transfer is written back to the DTC control data area. Twenty-four sets of control data can be stored in the DTC control data area, which allows 24 types of data transfers to be performed.
There are two transfer modes: normal mode and repeat mode. When the CHNE bit in the DTCCRj (j = 0 to 23) register is set to 1 (chain transfers enabled), multiple control data is read and data transfers are continuously performed by one activation source (chain transfers).
A transfer source address is specified by the 16-bit register DTSARj, and a transfer destination address is specified by the 16-bit register DTDARj. The values in the registers DTSARj and DTDARj are separately fixed or incremented according to the control data on completion of the data transfer.

15.3.2 Activation Sources

The DTC is activated by an interrupt source. Figure 15.2 is a Block Diagram Showing Control of DTC Activation Sources.
The interrupt sources to activate the DTC are selected with the DTCENi (i = 0 to 3, 5, 6) registers.
The DTC sets 0 (activation disabled) to the corresponding bit among bits DTCENi0 to DTCENi7 in the DTCENi register during operation when the setting of data transfer (the first transfer in chain transfers) is either of the following:

- Transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- Transfer causing the DTCCTj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

If the data transfer setting is not either of the above and the activation source is an interrupt source for timer RC, or the flash memory, the DTC sets 0 to the interrupt source flag corresponding to the activation source during operation.
Table 15.3 shows the DTC Activation Sources and Interrupt Source Flags for Setting to 0 during DTC Operation.
If multiple activation sources are simultaneously generated, the DTC activation will be performed according to the DTC activation source priority.
If multiple activation sources are simultaneously generated on completion of DTC operation, the next transfer will be performed according to the priority.
DTC activation is not affected by the I flag or interrupt control register, unlike with interrupt request operation. Therefore, even if interrupt requests cannot be acknowledged because interrupts are disabled, DTC activation requests can be acknowledged. The IR bit in the interrupt control register does not change even when an interrupt source to enable DTC activation is generated.

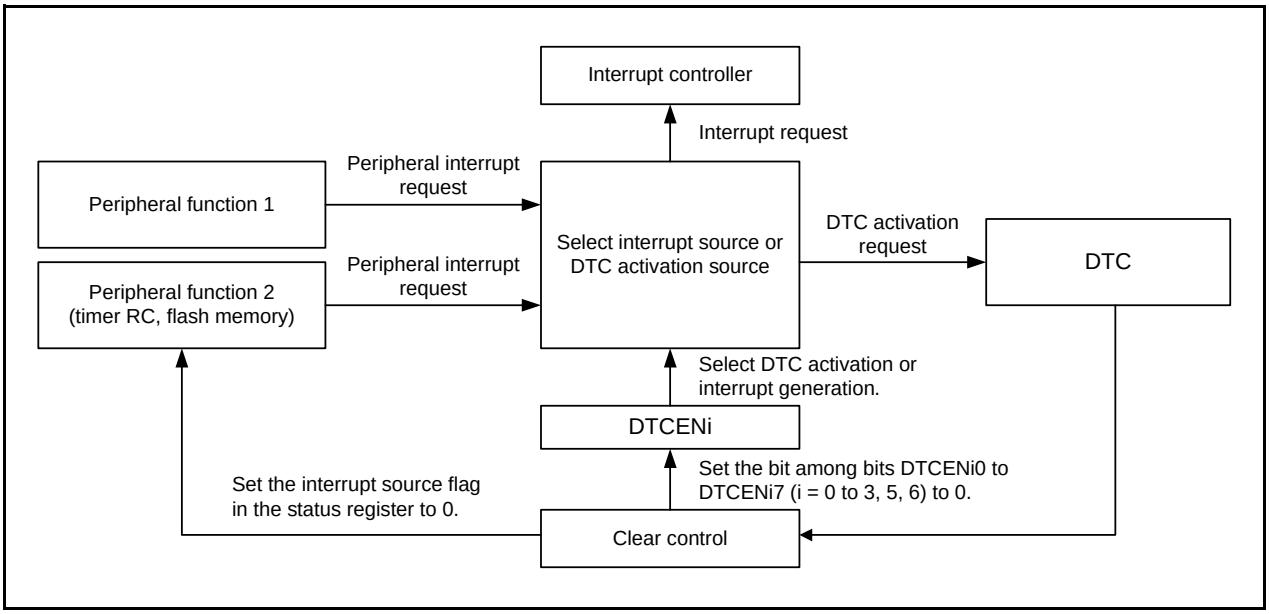


Figure 15.2 Block Diagram Showing Control of DTC Activation Sources

Table 15.3 DTC Activation Sources and Interrupt Source Flags for Setting to 0 during DTC Operation

DTC activation source generation	Interrupt Source Flag for Setting to 0
Timer RC input-capture/compare-match A	IMFA bit in TRCSR register
Timer RC input-capture/compare-match B	IMFB bit in TRCSR register
Timer RC input-capture/compare-match C	IMFC bit in TRCSR register
Timer RC input-capture/compare-match D	IMFD bit in TRCSR register
Flash ready status	RDYSTI bit in FST register

15.3.3 Control Data Allocation and DTC Vector Table

Control data is allocated in the order: Registers DTCCRj, DTBLSj, DTCCTj, DTRLDj, DTSARj, and DTDARj (j = 0 to 23). Table 15.4 shows the Control Data Allocation Addresses.

Table 15.4 Control Data Allocation Addresses

Register Symbol	Control Data No.	Address	DTCCRj Register	DTBLSj Register	DTCCTj Register	DTRLDj Register	DTSARj Register (Lower 8 Bits)	DTSARj Register (Higher 8 Bits)	DTDARj Register (Lower 8 Bits)	DTDARj Register (Higher 8 Bits)
DTCD0	Control Data 0	2C40h to 2C47h	2C40h	2C41h	2C42h	2C43h	2C44h	2C45h	2C46h	2C47h
DTCD1	Control Data 1	2C48h to 2C4Fh	2C48h	2C49h	2C4Ah	2C4Bh	2C4Ch	2C4Dh	2C4Eh	2C4Fh
DTCD2	Control Data 2	2C50h to 2C57h	2C50h	2C51h	2C52h	2C53h	2C54h	2C55h	2C56h	2C57h
DTCD3	Control Data 3	2C58h to 2C5Fh	2C58h	2C59h	2C5Ah	2C5Bh	2C5Ch	2C5Dh	2C5Eh	2C5Fh
DTCD4	Control Data 4	2C60h to 2C67h	2C60h	2C61h	2C62h	2C63h	2C64h	2C65h	2C66h	2C67h
DTCD5	Control Data 5	2C68h to 2C6Fh	2C68h	2C69h	2C6Ah	2C6Bh	2C6Ch	2C6Dh	2C6Eh	2C6Fh
DTCD6	Control Data 6	2C70h to 2C77h	2C70h	2C71h	2C72h	2C73h	2C74h	2C75h	2C76h	2C77h
DTCD7	Control Data 7	2C78h to 2C7Fh	2C78h	2C79h	2C7Ah	2C7Bh	2C7Ch	2C7Dh	2C7Eh	2C7Fh
DTCD8	Control Data 8	2C80h to 2C87h	2C80h	2C81h	2C82h	2C83h	2C84h	2C85h	2C86h	2C87h
DTCD9	Control Data 9	2C88h to 2C8Fh	2C88h	2C89h	2C8Ah	2C8Bh	2C8Ch	2C8Dh	2C8Eh	2C8Fh
DTCD10	Control Data 10	2C90h to 2C97h	2C90h	2C91h	2C92h	2C93h	2C94h	2C95h	2C96h	2C97h
DTCD11	Control Data 11	2C98h to 2C9Fh	2C98h	2C99h	2C9Ah	2C9Bh	2C9Ch	2C9Dh	2C9Eh	2C9Fh
DTCD12	Control Data 12	2CA0h to 2CA7h	2CA0h	2CA1h	2CA2h	2CA3h	2CA4h	2CA5h	2CA6h	2CA7h
DTCD13	Control Data 13	2CA8h to 2CAFh	2CA8h	2CA9h	2CAAh	2CABh	2CACh	2CADh	2CAEh	2CAFh
DTCD14	Control Data 14	2CB0h to 2CB7h	2CB0h	2CB1h	2CB2h	2CB3h	2CB4h	2CB5h	2CB6h	2CB7h
DTCD15	Control Data 15	2CB8h to 2CBFh	2CB8h	2CB9h	2CBAh	2CBBh	2CBCh	2CBDh	2CBEh	2CBFh
DTCD16	Control Data 16	2CC0h to 2CC7h	2CC0h	2CC1h	2CC2h	2CC3h	2CC4h	2CC5h	2CC6h	2CC7h
DTCD17	Control Data 17	2CC8h to 2CCFh	2CC8h	2CC9h	2CCAh	2CCBh	2CCCh	2CCDh	2CCEh	2CCFh
DTCD18	Control Data 18	2CD0h to 2CD7h	2CD0h	2CD1h	2CD2h	2CD3h	2CD4h	2CD5h	2CD6h	2CD7h
DTCD19	Control Data 19	2CD8h to 2CDFh	2CD8h	2CD9h	2CDAh	2CDBh	2CDCh	2CDDh	2CDEh	2CDFh
DTCD20	Control Data 20	2CE0h to 2CE7h	2CE0h	2CE1h	2CE2h	2CE3h	2CE4h	2CE5h	2CE6h	2CE7h
DTCD21	Control Data 21	2CE8h to 2CEFh	2CE8h	2CE9h	2CEAh	2CEBh	2CECh	2CEDh	2CEEh	2CEFh
DTCD22	Control Data 22	2CF0h to 2CF7h	2CF0h	2CF1h	2CF2h	2CF3h	2CF4h	2CF5h	2CF6h	2CF7h
DTCD23	Control Data 23	2CF8h to 2CFFh	2CF8h	2CF9h	2CFAh	2CFBh	2CFCh	2CFDh	2CFEh	2CFFh

j = 0 to 23

When the DTC is activated, one control data is selected according to the data read from the vector table which has been assigned to each activation source, and the selected control data is read from the DTC control data area.
Table 15.5 shows the DTC Activation Sources and DTC Vector Addresses. A one-byte vector table area is assigned to each activation source and one value from 00000000b to 00010111b (control data numbers in Table 15.4) is stored in each area to select one of the 24 control data sets.
Figures 15.3 to 15.7 show the DTC Internal Operation Flowchart.

Table 15.5 DTC Activation Sources and DTC Vector Addresses

Interrupt Request Source	Interrupt Name	Source No.	DTC Vector Address	Priority
External input	$\overline{\text{INT0}}$	0	2C00h	High
	$\overline{\text{INT1}}$	1	2C01h	↑
	$\overline{\text{INT3}}$	3	2C03h	
Key input	Key input	8	2C08h	
UART0	UART0 reception	10	2C0Ah	
	UART0 transmission	11	2C0Bh	
SSU/I^{2}C bus	Receive data full	16	2C10h	
	Transmit data empty	17	2C11h	
Voltage detection circuit	Voltage monitor 1	19	2C13h	
Timer RC	Input-capture/compare-match A	22	2C16h	
	Input-capture/compare-match B	23	2C17h	
	Input-capture/compare-match C	24	2C18h	
	Input-capture/compare-match D	25	2C19h	
Timer RE	Timer RE	42	2C2Ah	
Timer RA	Timer RA	49	2C31h	
Timer RB	Timer RB	51	2C33h	↓
Flash memory	Flash ready status	52	2C34h	Low

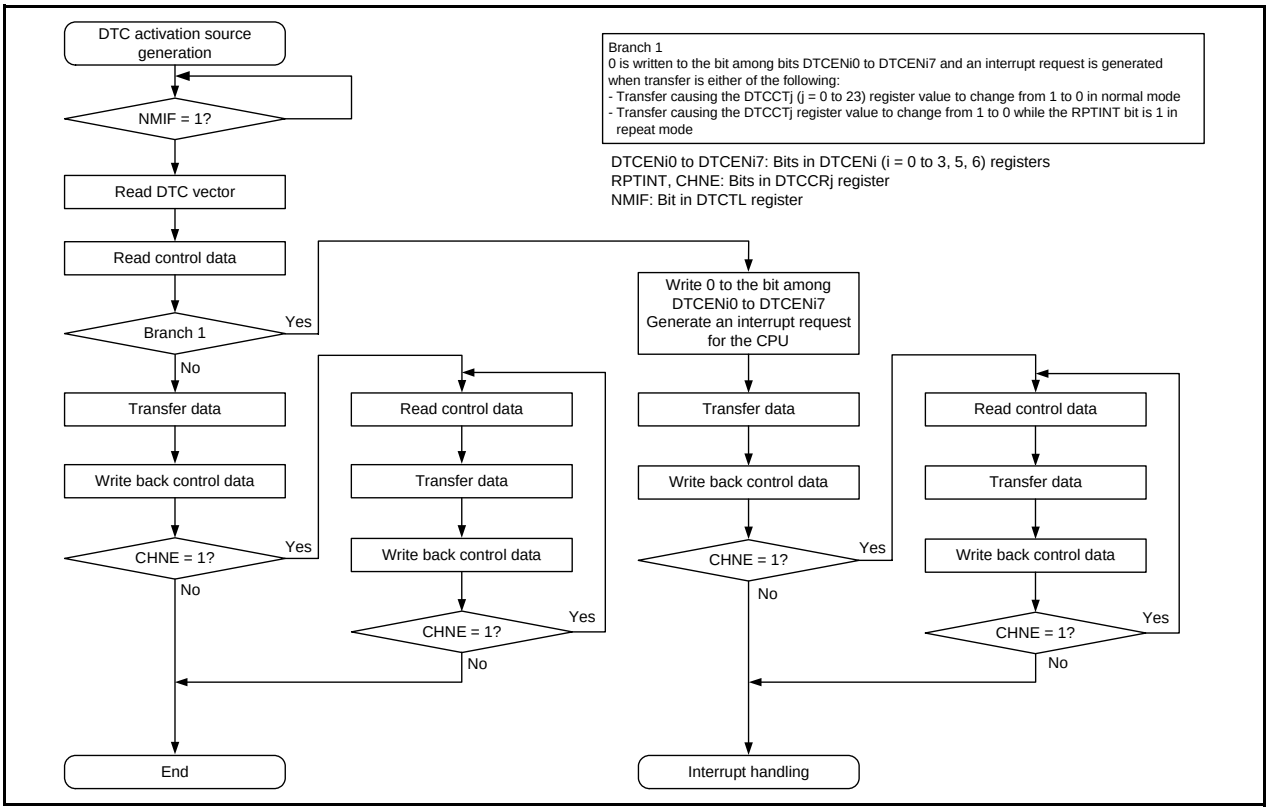


Figure 15.3 DTC Internal Operation Flowchart When DTC Activation Source is not SSU/I²C bus, Timer RC, or Flash Memory Interrupt Source

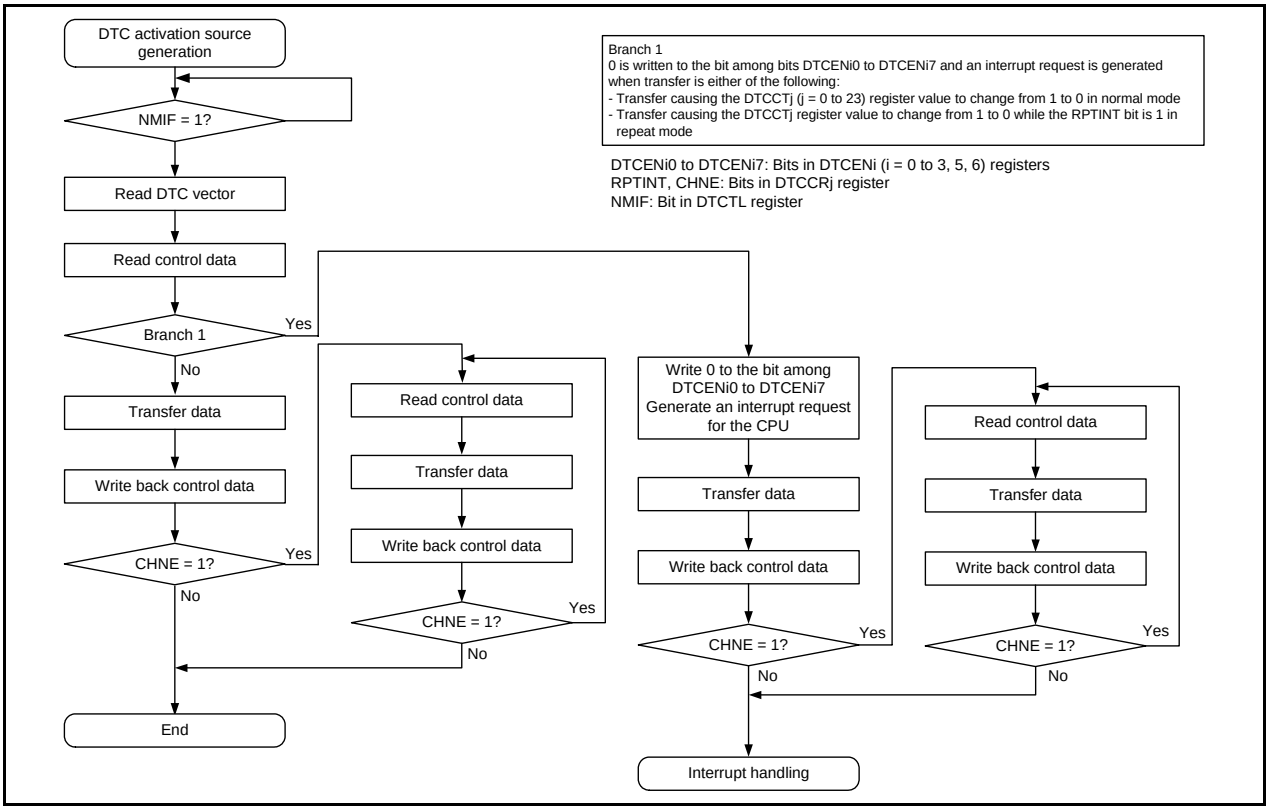
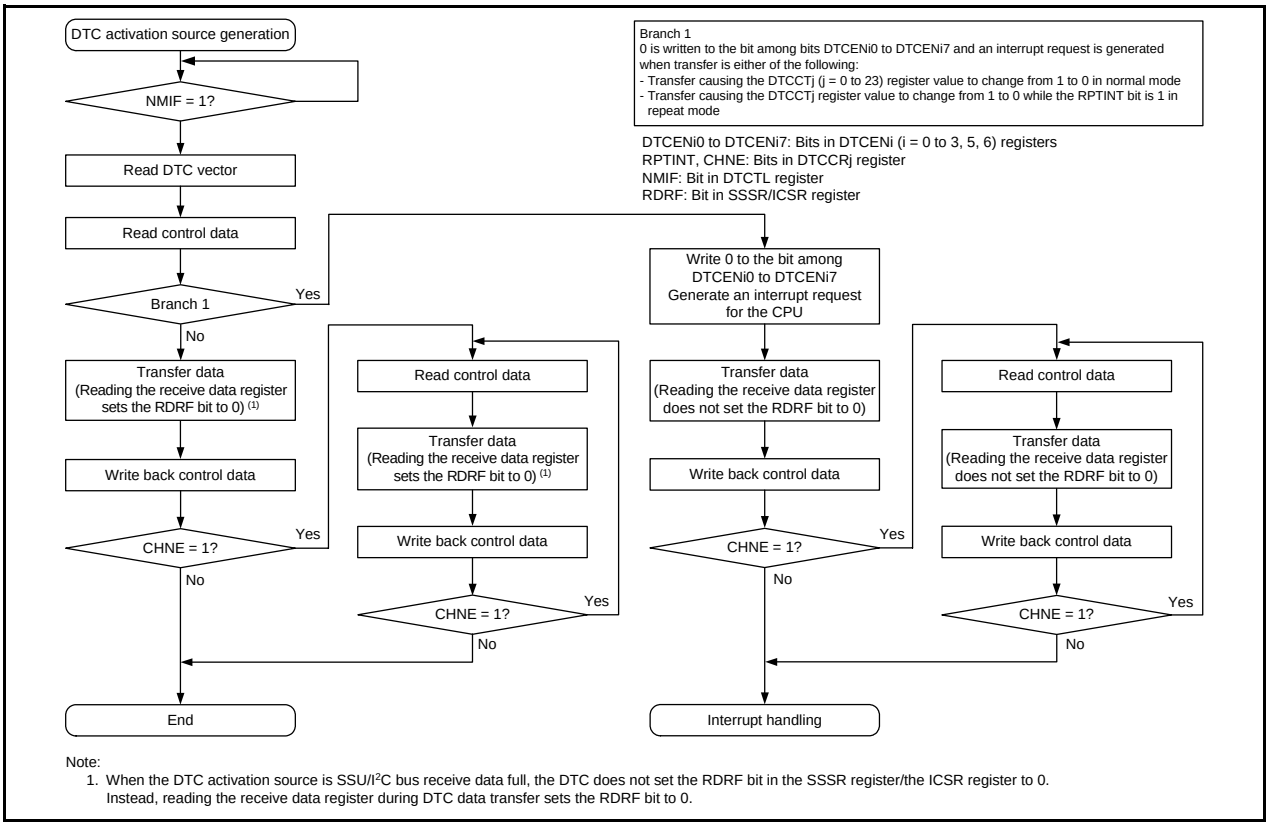
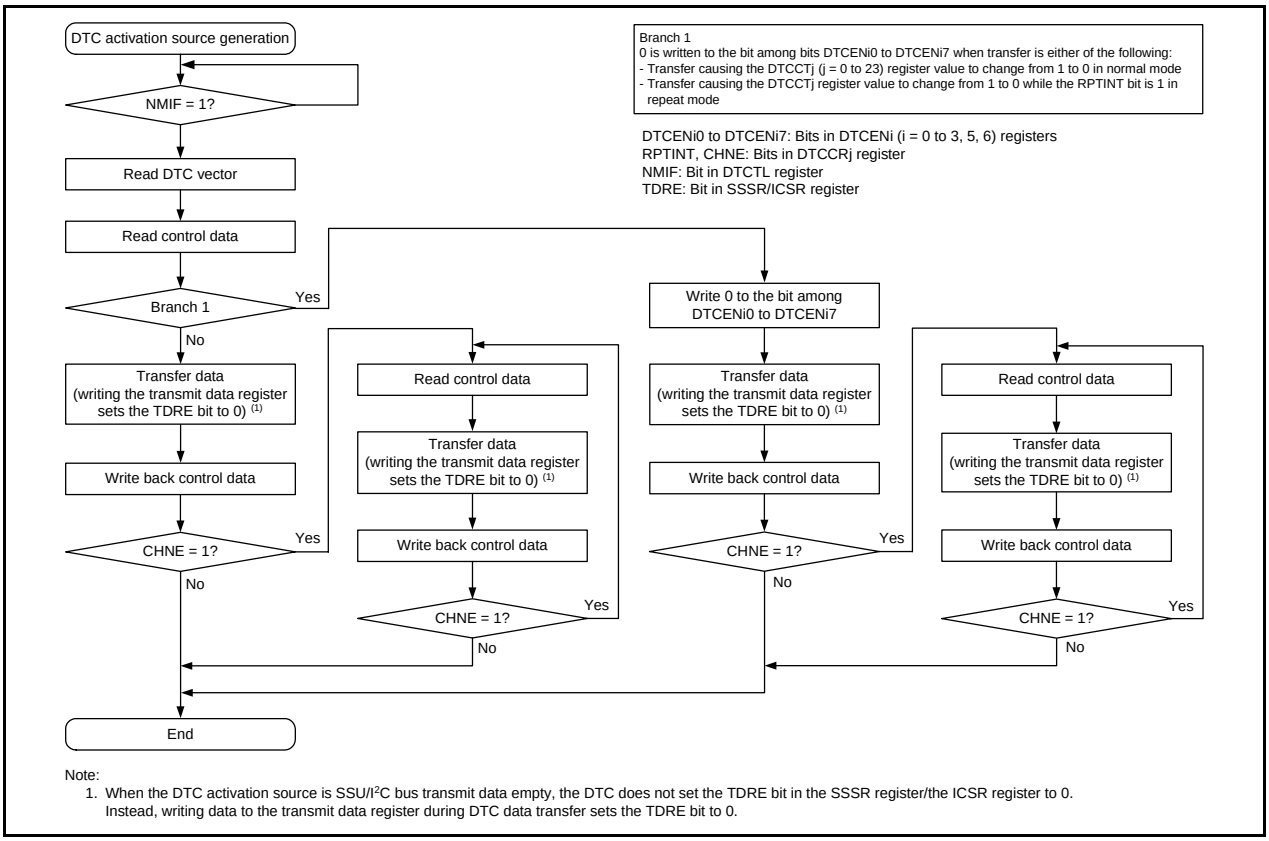


Figure 15.4 DTC Internal Operation Flowchart When DTC Activation Source is Timer RC Interrupt Source



Note:
1. When the DTC activation source is SSU/I²C bus receive data full, the DTC does not set the RDRF bit in the SSSR register/the ICSR register to 0. Instead, reading the receive data register during DTC data transfer sets the RDRF bit to 0.

Figure 15.5 DTC Internal Operation Flowchart When DTC Activation Source is SSU/I²C bus Receive Data Full



Note:
1. When the DTC activation source is SSU/I²C bus transmit data empty, the DTC does not set the TDRE bit in the SSSR register/the ICSR register to 0. Instead, writing data to the transmit data register during DTC data transfer sets the TDRE bit to 0.

Figure 15.6 DTC Internal Operation Flowchart When DTC Activation Source is SSU/I²C bus Transmit Data Empty

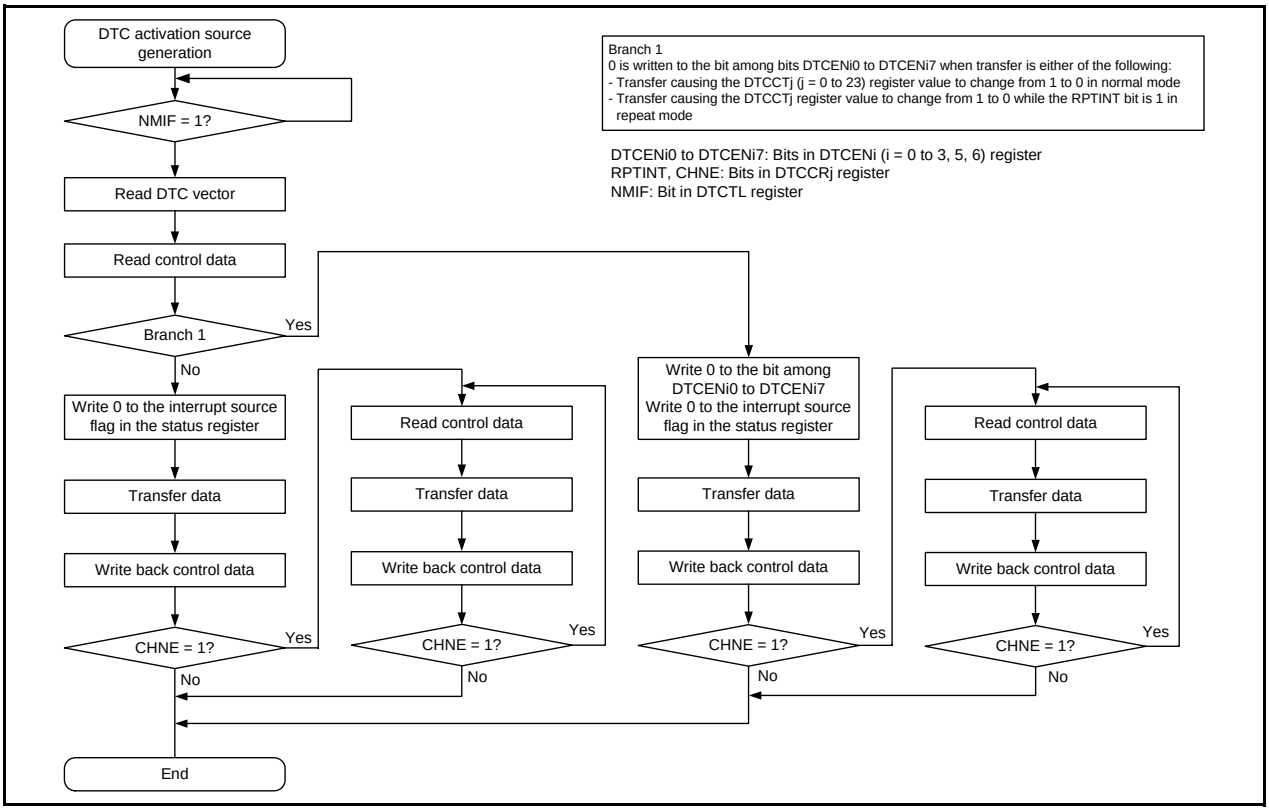


Figure 15.7 DTC Internal Operation Flowchart When DTC Activation Source is Flash ready status

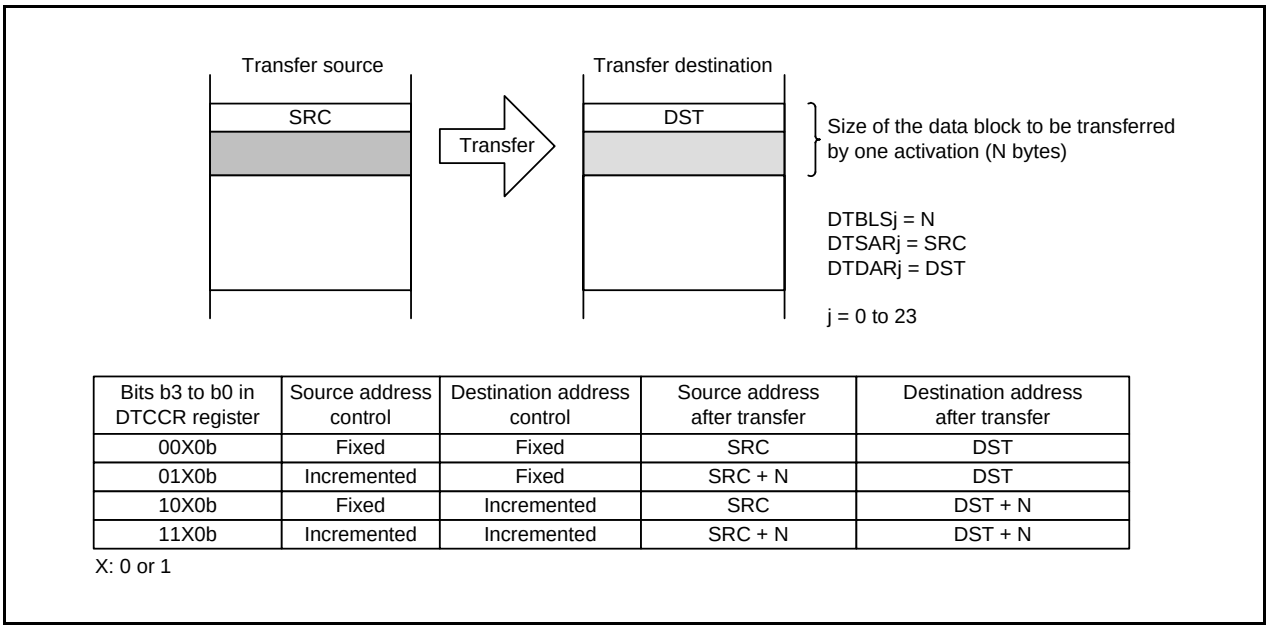
15.3.4 Normal Mode

One to 256 bytes of data are transferred by one activation. The number of transfer times can be 1 to 256. When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed, an interrupt request for the CPU is generated during DTC operation.
Table 15.6 shows Register Functions in Normal Mode.
Figure 15.8 shows Data Transfers in Normal Mode.

Table 15.6 Register Functions in Normal Mode

Register	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of times of data transfers
DTC transfer count reload register j	DTRLDj	Not used
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

j =0 to 23



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
00X0b	Fixed	Fixed	SRC	DST
01X0b	Incremented	Fixed	SRC + N	DST
10X0b	Fixed	Incremented	SRC	DST + N
11X0b	Incremented	Incremented	SRC + N	DST + N

X: 0 or 1

Figure 15.8 Data Transfers in Normal Mode

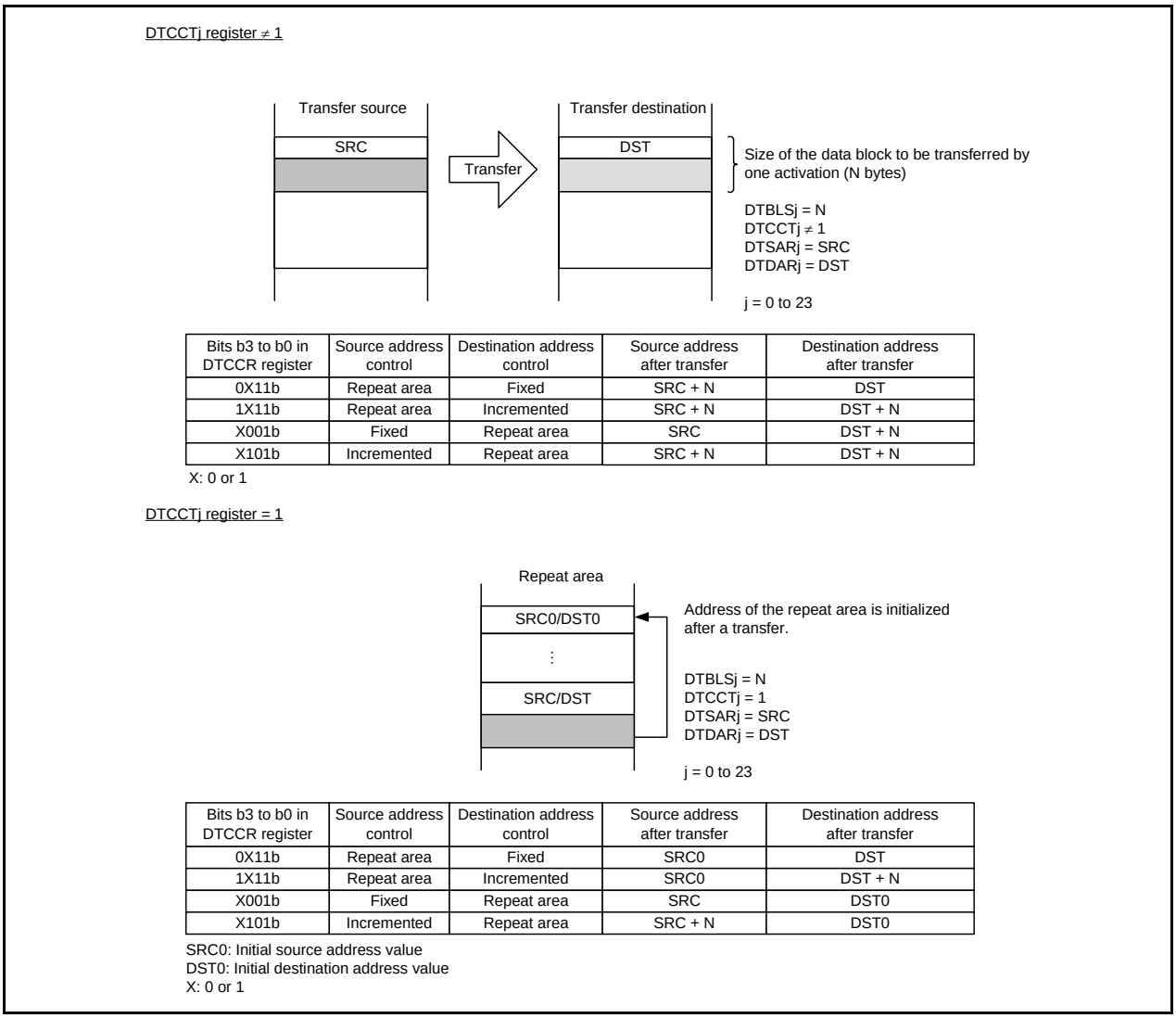
15.3.5 Repeat Mode

One to 255 bytes of data are transferred by one activation. Either of the transfer source or destination should be specified as the repeat area. The number of transfer times can be 1 to 255. On completion of the specified number of transfer times, the DTCCTj (i =0 to 23) register and the address specified for the repeat area are initialized to continue transfers. When the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled), an interrupt request for the CPU is generated during DTC operation.
The lower 8 bits of the initial value for the repeat area address must be 00h. The size of data to be transferred must be set to 255 bytes or less before the specified number of transfer times is completed.
Table 15.7 shows Register Functions in Repeat Mode. Figure 15.9 shows Data Transfers in Repeat Mode.

Table 15.7 Register Functions in Repeat Mode

Register	Symbol	Function
DTC block size register j	DTBLSj	Size of the data block to be transferred by one activation
DTC transfer count register j	DTCCTj	Number of times of data transfers
DTC transfer count reload register j	DTRLDj	This register value is reloaded to the DTCCT register (Data transfer count is initialized)
DTC source address register j	DTSARj	Data transfer source address
DTC destination address register j	DTDARj	Data transfer destination address

j =0 to 23



Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
0X11b	Repeat area	Fixed	SRC + N	DST
1X11b	Repeat area	Incremented	SRC + N	DST + N
X001b	Fixed	Repeat area	SRC	DST + N
X101b	Incremented	Repeat area	SRC + N	DST + N

X: 0 or 1

Bits b3 to b0 in DTCCR register	Source address control	Destination address control	Source address after transfer	Destination address after transfer
0X11b	Repeat area	Fixed	SRC0	DST
1X11b	Repeat area	Incremented	SRC0	DST + N
X001b	Fixed	Repeat area	SRC	DST0
X101b	Incremented	Repeat area	SRC + N	DST0

SRC0: Initial source address value
DST0: Initial destination address value
X: 0 or 1

Figure 15.9 Data Transfers in Repeat Mode

15.3.6 Chain Transfers

When the CHNE bit in the DTCCRj (j = 0 to 22) register is 1 (chain transfers enabled), multiple data transfers can be continuously performed by one activation source. Figure 15.10 shows a Flow of Chain Transfers.
When the DTC is activated, one control data is selected according to the data read from the DTC vector address corresponding to the activation source, and the selected control data is read from the DTC control data area. When the CHNE bit for the control data is 1 (chain transfers enabled), the next control data immediately following the current control data is read and transferred after the current transfer is completed. This operation is repeated until the data transfer with the control data for which the CHNE bit is 0 (chain transfers disabled) is completed.
When performing chain transfers using several control data, the number of transfers set to the first control data is enabled and the number of transfers proceeded after the first control data is disabled.
Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled).

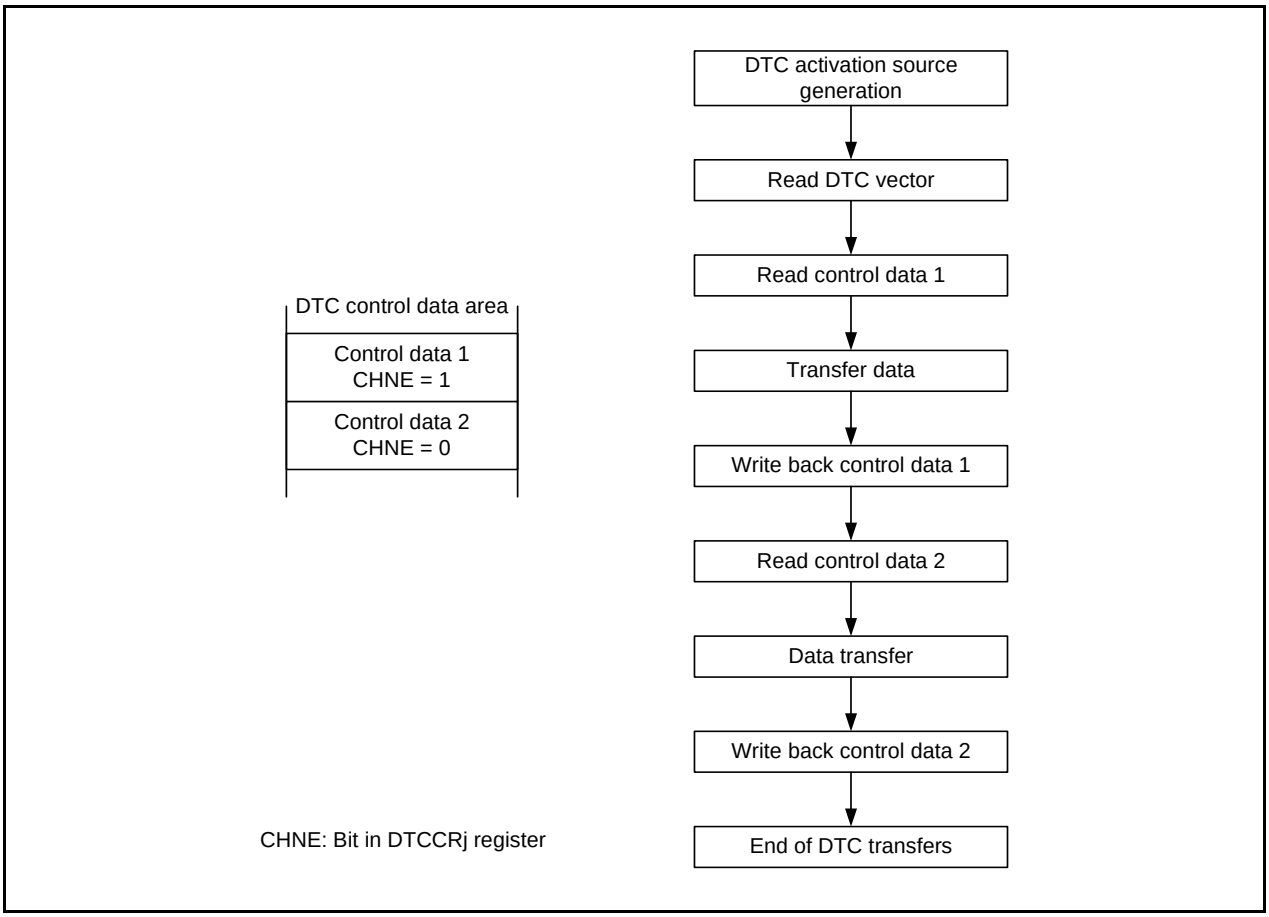


Figure 15.10 Flow of Chain Transfers

15.3.7 Interrupt Sources

When the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 is performed in normal mode, and when the data transfer causing the DTCCTj register value to change to 0 is performed while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode, the interrupt request corresponding to the activation source is generated for the CPU during DTC operation. However, no interrupt request is generated for the CPU when the activation source is SSU/I^{2}C bus transmit data empty or flash ready status.
Interrupt requests for the CPU are affected by the I flag or interrupt control register. In chain transfers, whether the interrupt request is generated or not is determined both by the number of transfer count specified for the first data transfer of the multiple ones and the RPTINT bit. When an interrupt request is generated for the CPU, the bit among bits DTCENi0 to DTCENi7 in the DTCENi (i = 0 to 3, 5, 6) registers corresponding to the activation source are set to 0 (activation disabled).

15.3.8 Operation Timings

The DTC requires five clock cycles to read control data allocated in the DTC control data area. The number of clock cycles required to write back control data differs depending on the control data settings.
Figure 15.11 shows an Example of DTC Operation Timings and Figure 15.12 shows an Example of DTC Operation Timings in Chain Transfers.
Table 15.8 shows the Specifications of Control Data Write-Back Operation.

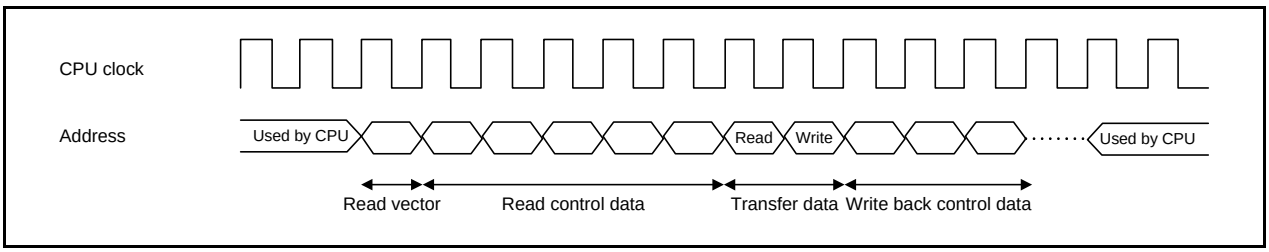


Figure 15.11 Example of DTC Operation Timings

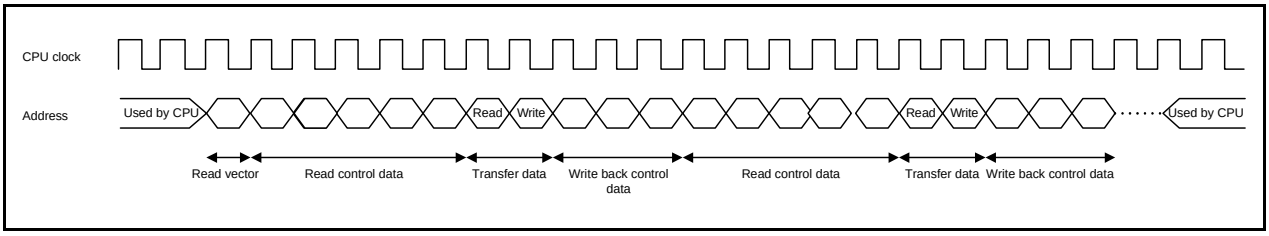


Figure 15.12 Example of DTC Operation Timings in Chain Transfers

Table 15.8 Specifications of Control Data Write-Back Operation

Bits b3 to b0 in DTCCR Register	Operating Mode	Address Control		Control Data to be Written Back				Number of Clock Cycles
		Source	Destination	DTCCTj Register	DTRLDj Register	DTSARj Register	DTDARj Register	
00X0b	Normal mode	Fixed	Fixed	Written back	Written back	Not written back	Not written back	1
01X0b		Incremented	Fixed	Written back	Written back	Written back	Not written back	2
10X0b		Fixed	Incremented	Written back	Written back	Not written back	Written back	2
11X0b		Incremented	Incremented	Written back	Written back	Written back	Written back	3
0X11b	Repeat mode	Repeat area	Fixed	Written back	Written back	Written back	Not written back	2
1X11b			Incremented	Written back	Written back	Written back	Written back	3
X001b		Fixed	Repeat area	Written back	Written back	Not written back	Written back	2
X101b		Incremented		Written back	Written back	Written back	Written back	3

j = 0 to 23
X: 0 or 1

15.3.9 Number of DTC Execution Cycles

Table 15.9 shows the Operations Following DTC Activation and Required Number of Cycles for each operation.
Table 15.10 shows the Number of Clock Cycles Required for Data Transfers.

Table 15.9 Operations Following DTC Activation and Required Number of Cycles

Vector Read	Control Data		Data Read	Data Write	Internal Operation
	Read	Write-back			
1	5	(Note 2)	(Note 1)	(Note 1)	1

Notes:
1. For the number of clock cycles required for data read/write, refer to **Table 15.10 Number of Clock Cycles Required for Data Transfers**.
2. For the number of clock cycles required for control data write-back, see **Table 15.8 Specifications of Control Data Write-Back Operation**.

Data is transferred as described below, when the DTBLSj (j = 0 to 23) register = N,
(1) When N = 2n (even), two-byte transfers are performed n times.
(2) When N = 2n + 1 (odd), two-byte transfers are performed n times followed by one time of one-byte transfer.

Table 15.10 Number of Clock Cycles Required for Data Transfers

Operation	Unit of Transfers	Internal RAM (During DTC Transfers)		Internal ROM (Program ROM)	Internal ROM (Data flash)	SFR (Word Access)		SFR (Byte Access)	SFR (DTC control data area)	
		Even Address	Odd Address			Even Address	Odd Address		Even Address	Odd Address
Data read	1-byte SK1	1		1	2	2		2	1	
	2-byte SK2	1	2	2	4	2	4	4	1	2
Data write	1-byte SL1	1		—	—	2		2	1	
	2-byte SL2	1	2	—	—	2	4	4	1	2

From Tables 15.9 and 15.10, the total number of required execution cycles can be obtained by the following formula:

Number of required execution cycles = 1 + Σ[formula A] + 2
Σ: Sum of the cycles for the number of transfer times performed by one activation source ([the number of transfer times for which CHNE is set to 1] + 1)

(1) For N = 2n (even)
Formula A = J + n • SK2 + n • SL2
(2) For N = 2n+1 (odd)
Formula A = J + n • SK2 + 1 • SK1 + n • SL2 + 1 • SL1
J: Number of cycles required to read control data (5 cycles) + number of cycles required to write back control data

To read data from or write data to the register that should be accessed in 16-bit units, set an even value of 2 or greater to the DTBLSj (j = 0 to 23) register.
The DTC performs accesses in 16-bit units.

15.3.10 DTC Activation Source Acknowledgement and Interrupt Source Flags

15.3.10.1 Interrupt Sources Except for Flash Memory, Timer RC, and Synchronous Serial Communication Unit (SSU)/I²C bus

When the DTC activation source is an interrupt source except for the flash memory, timer RC, or the synchronous serial communication unit/I²C bus, the same DTC activation source cannot be acknowledged for 8 to 12 cycles of the CPU clock after the interrupt source is generated. If an interrupt source is generated when a software command is executed, the same DTC activation source cannot be acknowledged for 9 to 16 cycles of the CPU clock. If a DTC activation source is generated during DTC operation and acknowledged, the same DTC activation source cannot be acknowledged for 8 to 12 cycles of the CPU clock on completion of the DTC transfer immediately before the DTC is activated by the source. When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the same DTC activation source cannot be acknowledged for 16 cycles of the CPU clock.

15.3.10.2 Flash Memory

When the DTC activation source is flash ready status, even if a flash ready status interrupt request is generated, it is not acknowledged as the DTC activation source after the RDYSTI bit in the FST register is set to 1 (flash ready status interrupt request) and before the DTC sets the RDYSTI bit to 0 (no flash ready status interrupt request). If a flash ready status interrupt request is generated after the DTC sets the RDYSTI bit to 0, the DTC acknowledges it as the activation source. 8 to 12 cycles of the CPU clock are required after the RDYSTI bit is set to 1 and before the DTC sets the interrupt request flag to 0. If a flash ready status interrupt is generated when a software command is executed, 9 to 16 cycles of the CPU clock are required before the DTC sets the interrupt source flag to 0. If a flash ready status interrupt request is generated during DTC operation and acknowledged as the DTC activation source, the RDYSTI bit is set to 0 after 8 to 12 cycles of the CPU clock on completion of the DTC transfer immediately before the DTC is activated by the source. When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the RDYSTI bit is set to 0 after 16 cycles of the CPU clock.

15.3.10.3 Timer RC

When the DTC activation source is an interrupt source for timer RC, even if an input capture/compare match in individual timers occurs, it is not acknowledged as the DTC activation source after the interrupt source flag is set to 1 and before the DTC sets the flag to 0. If an input capture/compare match occurs after the DTC sets the interrupt source flag to 0, the DTC acknowledges it as the activation source. 8 to 12 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock are required after the interrupt source flag is set to 1 and before the DTC sets the flag to 0. If the interrupt request flag is set to 1 when a software command is executed, 9 to 16 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock are required before the DTC sets the interrupt source flag to 0. If individual DTC activation sources are generated for timer RC during DTC operation and acknowledged, the interrupt source flag is set to 0 after 8 to 12 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock on completion of the DTC transfer immediately before the DTC is activated by the source. When a software command is executed on completion of the DTC transfer immediately before the DTC is activated, the interrupt source flag is set to 0 after 16 cycles of the CPU clock plus 0.5 to 1.5 cycles of the timer operating clock.

15.3.10.4 SSU/I²C bus Receive Data Full

When the DTC activation source is SSU/I²C bus receive data full, read the SSRDR register/the ICDRR register using a data transfer. The RDRF bit in the SSSR register/the ICSR register is set to 0 (no data in SSRDR/ICDRR register) by reading the SSRDR register/ the ICDRR register. If an interrupt source for receive data full is subsequently generated, the DTC acknowledges it as the activation source.

15.3.10.5 SSU/I²C bus Transmit Data Empty

When the DTC activation source is SSU/I²C bus transmit data empty, write to the SSTDR register/the ICDRT register using a data transfer. The TDRE bit in the SSSR register/the ICSR register is set to 0 (data is not transferred from registers SSTDR/ICDRT to SSTRSR/ICDRS) by writing to the SSTDR register/the ICDRT register. If an interrupt source for transmit data empty is subsequently generated, the DTC acknowledges it as the activation source.

15.4 Notes on DTC

15.4.1 DTC activation source

- Do not generate any DTC activation sources before entering wait mode or during wait mode.
- Do not generate any DTC activation sources before entering stop mode or during stop mode.

15.4.2 DTCENi (i = 0 to 3, 5, 6) Registers

- Modify bits DTCENi0 to DTCENi7 only while an interrupt request corresponding to the bit is not generated.
- When the interrupt source flag in the status register for the peripheral function is 1, do not modify the corresponding activation source bit among bits DTCENi0 to DTCENi7.
- Do not access the DTCENi registers using DTC transfers.
- The bits with no interrupt sources assigned are reserved. Set these bits to 0.

15.4.3 Peripheral Modules

- Do not set the status register bit for the peripheral function to 0 using a DTC transfer.
- When the DTC activation source is SSU/I^{2}C bus receive data full, read the SSRDR register/the ICDRR register using a DTC transfer.
  The RDRF bit in the SSSR register/the ICSR register is set to 0 (no data in SSRDR/ICDRR register) by reading the SSRDR register/the ICDRR register.
  However, the RDRF bit is not set to 0 by reading the SSRDR register/the ICDRR register when the DTC data transfer setting is either of the following:
  - Transfer causing the DTCCTj (j = 0 to 23) register value to change from 1 to 0 in normal mode
  - Transfer causing the DTCCRj register value to change from 1 to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode
- When the DTC activation source is SSU/I^{2}C bus transmit data empty, write to the SSTDR register/the ICDRT register using a DTC transfer. The TDRE bit in the SSSR register/the ICSR register is set to 0 (data is not transferred from registers SSTDR/ICDRT to SSTRSR/ICDRS) by writing to the SSTDR register/the ICDRT register.

15.4.4 Interrupt Requests

No interrupt is generated for the CPU during DTC operation in any of the following cases:
- When the DTC activation source is SSU/I^{2}C transmit data empty or flash ready status
- When performing the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- When performing the data transfer causing the DTCCRj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

15.4.5 DTC Chain Transfers

When performing chain transfers using several control data, the number of transfers set to the first control data is enabled and the number of transfers proceeded after the first control data is disabled.
Examples:
- When DTCCT0 = 5 and DTCCT1 = 10, chain transfers are performed as DTCCT0 = DTCCT1 = 5.
- When DTCCT0 = 10 and DTCCT1 = 5, chain transfers are performed as DTCCT0 = DTCCT1 = 10.
- When DTCCT0 = 10, DTCCT1 = 5, and DTCCT2 = 2, chain transfers are performed as DTCCT0 = DTCCT1 = DTCCT2 = 10.

16. General Overview of Timers

The MCU has two 8-bit timers with 8-bit prescalers, one 16-bit timer, and a timer with a 4-bit counter and an 8-bit counter. The two 8-bit timers with 8-bit prescalers are timer RA and timer RB. These timers contain a reload register to store the default value of the counter. The 16-bit timer is timer RC which has input capture and output compare functions. The timer with the 4-bit and 8-bit counters is timer RE. All the timers operate independently.
Table 16.1 lists Functional Comparison of Timers.

Table 16.1 Functional Comparison of Timers

Item		Timer RA	Timer RB	Timer RC	Timer RE
Configuration		8-bit timer with 8-bit prescaler (with reload register)	8-bit timer with 8-bit prescaler (with reload register)	16-bit timer (with input capture and output compare)	4-bit counter 8-bit counter
Count		Decrement	Decrement	Increment	Increment
Count sources		• f1 • f2 • f8 • fOCO • fC32 • fC	• f1 • f2 • f8 • Timer RA underflow	• f1 • f2 • f4 • f8 • f32 • TRCCLK	• f4 • f8 • f32 • fC4
Function	Count of the internal count source	Timer mode	Timer mode	Timer mode (output compare function)	—
	Count of the external count source	Event counter mode	—	Timer mode (output compare function)	—
	External pulse width/ period measurement	Pulse width measurement mode, pulse period measurement mode	—	Timer mode (input capture function; 4 pins)	—
	PWM output	Pulse output mode (1), Event counter mode (1)	Programmable waveform generation mode	Timer mode (output compare function; 4 pins), PWM mode (3 pins), PWM2 mode (1 pin)	Output compare mode
	One-shot waveform output	—	Programmable one-shot generation mode, Programmable wait one-shot generation mode	PWM mode (3 pins)	—
	Three-phase waveforms output	—	—	—	—
	Timer	Timer mode (only fC32 count)	—	—	Real-time clock mode
Input pin		TRAIO	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$, TRCCLK, TRCTRG, TRCIOA, TRCIOB, TRCIOC, TRCIOD	—
Output pin		TRAO, TRAIO	TRBO	TRCIOA, TRCIOB, TRCIOC, TRCIOD	TREO
Related interrupt		Timer RA interrupt	Timer RB interrupt, $\overline{\text{INT0}}$ interrupt	Compare match/ input capture A to D interrupt, Overflow interrupt, $\overline{\text{INT0}}$ interrupt	Timer RE interrupt
Timer stop		Provided	Provided	Provided	Provided

Note:
1. Rectangular waves are output in these modes. Since the waves are inverted at each overflow, the “H” and “L” level widths of the pulses are the same.

17. Timer RA

Timer RA is an 8-bit timer with an 8-bit prescaler.

17.1 Overview

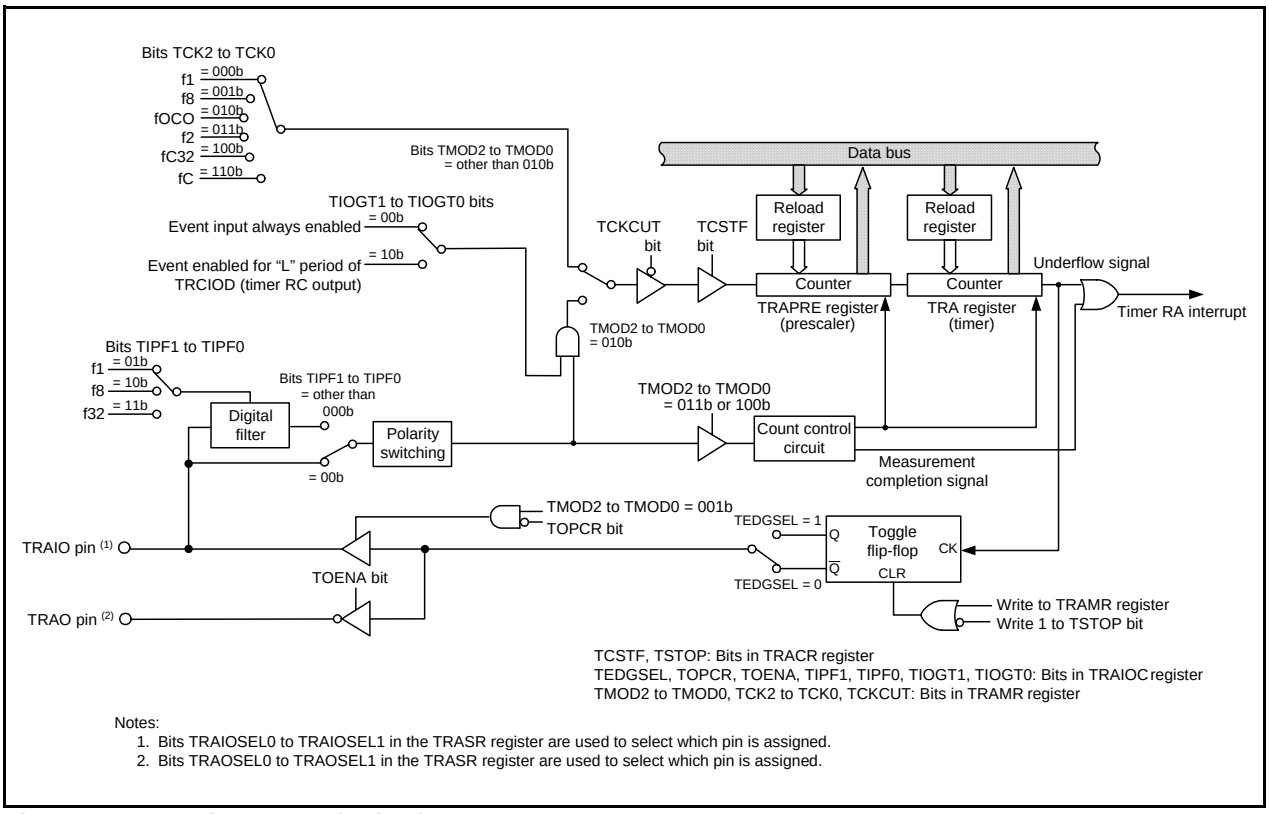
The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing registers TRAPRE and TRA (refer to **Tables 17.2 to 17.6 the Specifications of Each Mode**).

The count source for timer RA is the operating clock that regulates the timing of timer operations such as counting and reloading.

Figure 17.1 shows a Timer RA Block Diagram. Table 17.1 lists Pin Configuration of Timer RA.

Timer RA contains the following five operating modes:

- Timer mode — The timer counts the internal count source.
- Pulse output mode — The timer counts the internal count source and outputs pulses which invert the polarity by underflow of the timer.
- Event counter mode — The timer counts external pulses.
- Pulse width measurement mode — The timer measures the pulse width of an external pulse.
- Pulse period measurement mode — The timer measures the pulse period of an external pulse.



Notes:
1. Bits TRAIOSEL0 to TRAIOSEL1 in the TRASR register are used to select which pin is assigned.
2. Bits TRAOSEL0 to TRAOSEL1 in the TRASR register are used to select which pin is assigned.

Figure 17.1 Timer RA Block Diagram

Table 17.1 Pin Configuration of Timer RA

Pin Name	Assigned Pin	I/O	Function
TRAIO	P1_5, or P1_7	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details
TRAO	P3_0, or P3_7	Output	

17.2 Registers

17.2.1 Timer RA Control Register (TRACR)

Address 0100h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RA count status flag (1)	0: Count stops 1: During count	R
b2	TSTOP	Timer RA count forcible stop bit (2)	When this bit is set to 1, the count is forcibly stopped. When read, its content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TEDGF	Active edge judgment flag (3, 4)	0: Active edge not received 1: Active edge received (end of measurement period)	R/W
b5	TUNDF	Timer RA underflow flag (3)	0: No underflow 1: Underflow	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. Refer to **17.8 Notes on Timer RA** for precautions regarding bits TSTART and TCSTF.
2. When the TSTOP bit is set to 1, bits TSTART and TCSTF and registers TRAPRE and TRA are set to the values after a reset.
3. Bits TEDGF and TUNDF can be set to 0 by writing 0 to these bits by a program. However, their value remains unchanged when 1 is written.
4. The TEDGF bit is not used in timer mode, pulse output mode, or event count mode.

In pulse width measurement mode and pulse period measurement mode, use the MOV instruction to set the TRACR register. If it is necessary to avoid changing the values of bits TEDGF and TUNDF, write 1 to them.

17.2.2 Timer RA I/O Control Register (TRAIOC)

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Function varies according to the operating mode.	R/W
b1	TOPCR	TRAIO output control bit		
b2	TOENA	TRAO output enable bit		
b3	—	Reserved bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit	Function varies according to the operating mode.	R/W
b5	TIPF1			
b6	TIOGT0	TRAIO event input control bit		
b7	TIOGT1			

17.2.3 Timer RA Mode Register (TRAMR)

Address 0102h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	TCK2	TCK1	TCK0	—	TMOD2	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode 1 0 1: Do not set. 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TCK0	Timer RA count source select bit	b6 b5 b4 0 0 0: f1 0 0 1: f8 0 1 0: fOCO 0 1 1: f2 1 0 0: fC32 1 0 1: Do not set. 1 1 0: fC 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Provides count source 1: Cuts off count source	R/W

When both the TSTART and TCSTF bits in the TRACR register are set to 0 (count stops), rewrite this register.

17.2.4 Timer RA Prescaler Register (TRAPRE)

Address 0103h

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source	00h to FFh	R/W
	Pulse output mode		00h to FFh	R/W
	Event counter mode	Counts an external count source	00h to FFh	R/W
	Pulse width measurement mode	Measure pulse width of input pulses from external (counts internal count source)	00h to FFh	R/W
	Pulse period measurement mode	Measure pulse period of input pulses from external (counts internal count source)	00h to FFh	R/W

Note:
1. When the TSTOP bit in the TRACR register is set to 1, the TRAPRE register is set to FFh.

17.2.5 Timer RA Register (TRA)

Address 0104h

Bit	b7	b6	b5	b4	b3	b2	b1	b0	
Symbol	—	—	—	—	—	—	—	—	
After Reset	1	1	1	1	1	1	1	1	(Note 1)

Bit	Mode	Function	Setting Range	R/W
b7 to b0	All modes	Counts on underflow of TRAPRE register	00h to FFh (2)	R/W

Notes:
1. When the TSTOP bit in the TRACR register is set to 1, the TRA register is set to FFh.
2. Do not set 00h to the TRA register in pulse width measurement mode and pulse period measurement mode.

17.2.6 Timer RA Pin Select Register (TRASR)

Address 0180h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	TRAOSEL1	TRAOSEL0	—	TRAIOSEL1	TRAIOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRAIOSEL0	TRAIO pin select bit	b1 b0 0 0: TRAIO pin not used 0 1: P1_7 assigned 1 0: P1_5 assigned 1 1: Do not set.	R/W
b1	TRAIOSEL1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	TRAOSEL0	TRAO pin select bit	b4 b3 0 0: P3_7 assigned 0 1: P3_0 assigned 1 0: Do not set. 1 1: Do not set.	R/W
b4	TRAOSEL1			R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The TRASR register selects which pin is assigned to the timer RA I/O. To use the I/O pin for timer RA, set this register.
Set the TRASR register before setting the timer RA associated registers. Also, do not change the setting value in this register during timer RA operation.

17.3 Timer Mode

In this mode, the timer counts an internally generated count source (refer to **Table 17.2 Timer Mode Specifications**).

Table 17.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32, fC
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
TRAIO pin function	Programmable I/O port
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).

17.3.1 Timer RA I/O Control Register (TRAIOC) in Timer Mode

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in timer mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

17.3.2 Timer Write Control during Count Operation

Timer RA has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. When writing to the prescaler or timer, values are written to both the reload register and counter.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, if the prescaler or timer is written to when count operation is in progress, the counter value is not updated immediately after the WRITE instruction is executed. Figure 17.2 shows an Operating Example of Timer RA when Counter Value is Rewritten during Count Operation.

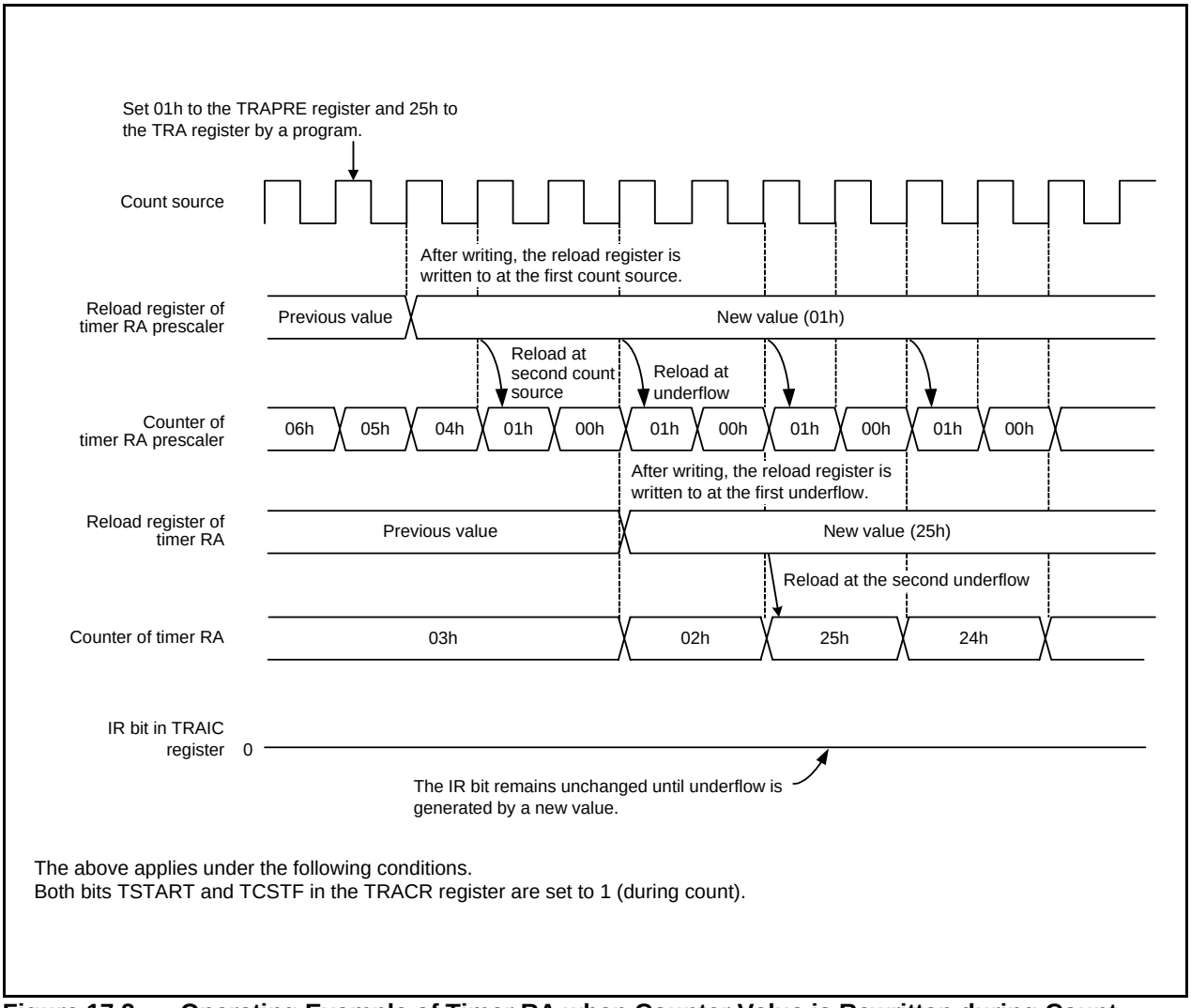


Figure 17.2 Operating Example of Timer RA when Counter Value is Rewritten during Count Operation

17.4 Pulse Output Mode

In pulse output mode, the internally generated count source is counted, and a pulse with inverted polarity is output from the TRAIO pin each time the timer underflows (refer to **Table 17.3 Pulse Output Mode Specifications**).

Table 17.3 Pulse Output Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32, fC
Count operations	• Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
TRAIO pin function	Pulse output, programmable output port
TRAO pin function	Programmable I/O port or inverted output of TRAIO
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRAIO signal polarity switch function The level when the pulse output starts is selected by the TEDGSEL bit in the TRAIOC register. (1) • TRAO output function Pulses inverted from the TRAIO output polarity can be output from the TRAO pin (selectable by the TOENA bit in the TRAIOC register). • Pulse output stop function Output from the TRAIO pin is stopped by the TOPCR bit in the TRAIOC register. • TRAIO pin select function P1_5, or P1_7 is selected by bits TRAIOSEL0 to TRAIOSEL1 in the TRASR register. • TRAO pin select function P3_0, or P3_7 is selected by bits TRAOSEL0 and TRAOSEL1 in the TRASR register.

Note:
1. The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.

17.4.1 Timer RA I/O Control Register (TRAIOC) in Pulse Output Mode

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: TRAIO output starts at “H” 1: TRAIO output starts at “L”	R/W
b1	TOPCR	TRAIO output control bit	0: TRAIO output 1: TRAIO output disabled	R/W
b2	TOENA	TRAO output enable bit	0: TRAO output disabled 1: TRAO output (inverted TRAIO output from the port)	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in pulse output mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

17.5 Event Counter Mode

In event counter mode, external signal inputs to the TRAIO pin are counted (refer to **Table 17.4 Event Counter Mode Specifications**).

Table 17.4 Event Counter Mode Specifications

Item	Specification
Count source	External signal which is input to TRAIO pin (active edge selectable by a program)
Count operations	• Decrement • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Divide ratio	1/(n+1)(m+1) n: setting value of TRAPRE register, m: setting value of TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	When timer RA underflows [timer RA interrupt].
TRAIO pin function	Count source input
TRAO pin function	Programmable I/O port or pulse output (1)
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• TRAIO input polarity switch function The active edge of the count source is selected by the TEDGSEL bit in the TRAIOC register. • Count source input pin select function P1_5, or P1_7 is selected by bits TRAIOSEL0 to TRAIOSEL1 in the TRASR register. • Pulse output function Pulses of inverted polarity can be output from the TRAO pin each time the timer underflows (selectable by the TOENA bit in the TRAIOC register). (1) • TRAO pin select function P3_0, or P3_7 is selected by bits TRAOSEL0 and TRAOSEL1 in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAIOC register. • Event input control function The enabled period for the event input to the TRAIO pin is selected by bits TIOGT0 and TIOGT1 in the TRAIOC register.

Note:
1. The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.

17.5.1 Timer RA I/O Control Register (TRAIOC) in Event Counter Mode

Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: Starts counting at rising edge of the TRAIO input and TRAO starts output at “L” 1: Starts counting at falling edge of the TRAIO input and TRAO starts output at “H”	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in event counter mode.	R/W
b2	TOENA	TRAO output enable bit	0: TRAO output disabled 1: TRAO output	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	b7 b6 0 0: Event input always enabled 0 1: Do not set. 1 0: Event input enabled for “L” period of TRCIOD (timer RC output) 1 1: Do not set.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

17.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the TRAIO pin is measured (refer to **Table 17.5 Pulse Width Measurement Mode Specifications**).
Figure 17.3 shows an Operating Example of Pulse Width Measurement Mode.

Table 17.5 Pulse Width Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32, fC
Count operations	• Decrement • Continuously counts the selected signal only when measurement pulse is “H” level, or conversely only “L” level. • When the timer underflows, the contents of the reload register are reloaded and the count is continued.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]
TRAIO pin function	Measured pulse input
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement level setting The “H” level or “L” level period is selected by the TEDGSEL bit in the TRAIOC register. • Measured pulse input pin select function P1_5, or P1_7 is selected by bits TRAIOSEL0 to TRAIOSEL1 in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAIOC register.

17.6.1 Timer RA I/O Control Register (TRAIOC) in Pulse Width Measurement Mode

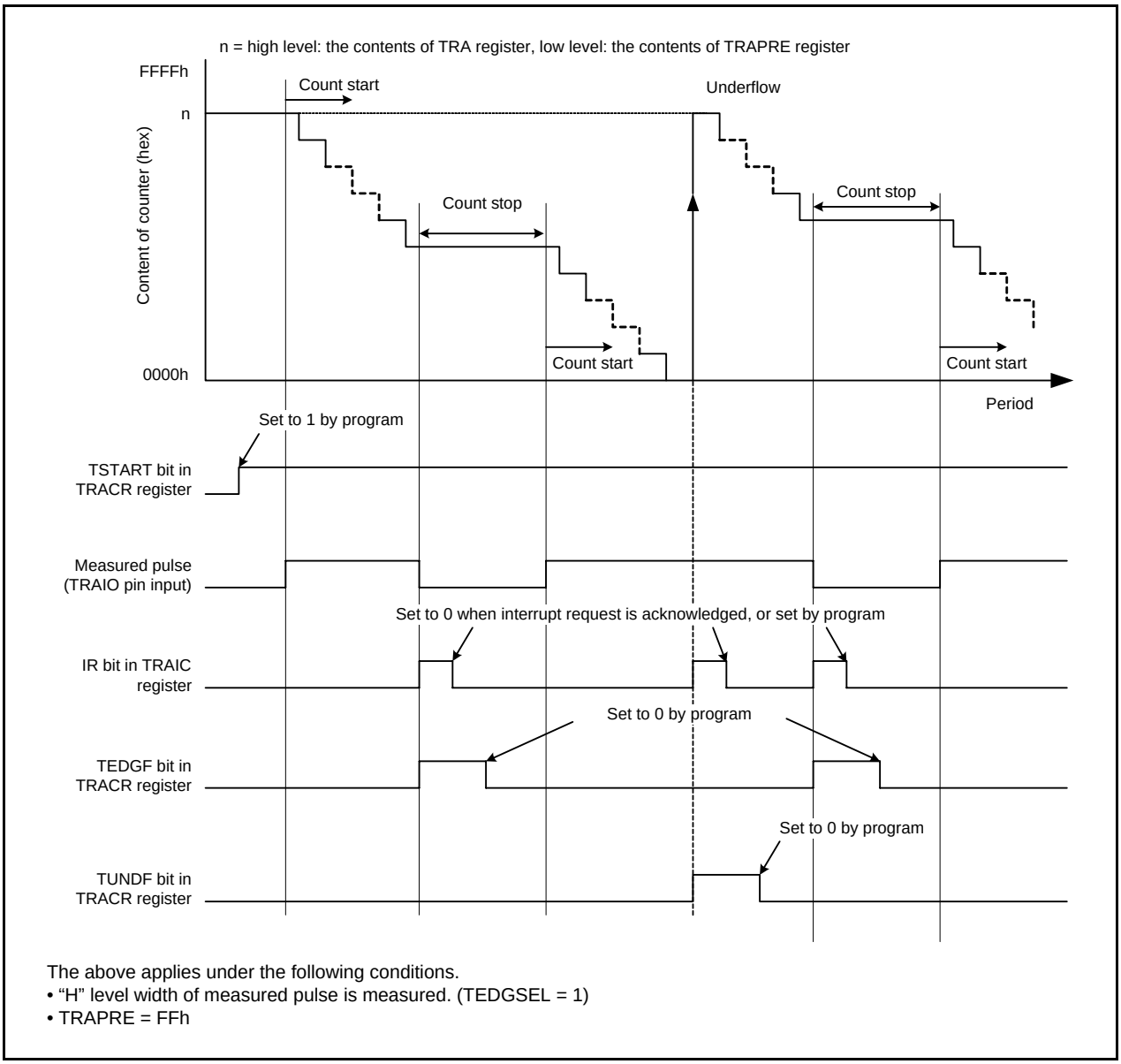
Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: TRAIO input starts at “L” 1: TRAIO input starts at “H”	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in pulse width measurement mode.	R/W
b2	TOENA	TRAO output enable bit		R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	Set to 0 in pulse width measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

17.6.2 Operating Example



The above applies under the following conditions.
- "H" level width of measured pulse is measured. (TEDGSEL = 1)
- TRAPRE = FFh

Figure 17.3 Operating Example of Pulse Width Measurement Mode

17.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the TRAIO pin is measured (refer to **Table 17.6 Pulse Period Measurement Mode Specifications**).
Figure 17.4 shows an Operating Example of Pulse Period Measurement Mode.

Table 17.6 Pulse Period Measurement Mode Specifications

Item	Specification
Count sources	f1, f2, f8, fOCO, fC32, fC
Count operations	• Decrement • After the active edge of the measured pulse is input, the contents of the read-out buffer are retained at the first underflow of timer RA prescaler. Then timer RA reloads the contents in the reload register at the second underflow of timer RA prescaler and continues counting.
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	• 0 (count stops) is written to TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	• When timer RA underflows or reloads [timer RA interrupt]. • Rising or falling of the TRAIO input (end of measurement period) [timer RA interrupt]
TRAIO pin function	Measured pulse input (1)
TRAO pin function	Programmable I/O port
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	• When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to **17.3.2 Timer Write Control during Count Operation**).
Selectable functions	• Measurement period selection The measurement period of the input pulse is selected by the TEDGSEL in the TRAIOC register. • Measured pulse input pin select function P1_5, or P1_7 is selected by bits TRAIOSEL0 to TRAIOSEL1 in the TRASR register. • Digital filter function Whether enabling or disabling the digital filter and the sampling frequency is selected by bits TIPF0 and TIPF1 in the TRAIOC register.

Note:
1. Input a pulse with a period longer than twice the timer RA prescaler period. Input a pulse with a longer “H” and “L” width than the timer RA prescaler period. If a pulse with a shorter period is input to the TRAIO pin, the input may be ignored.

17.7.1 Timer RA I/O Control Register (TRAIOC) in Pulse Period Measurement Mode

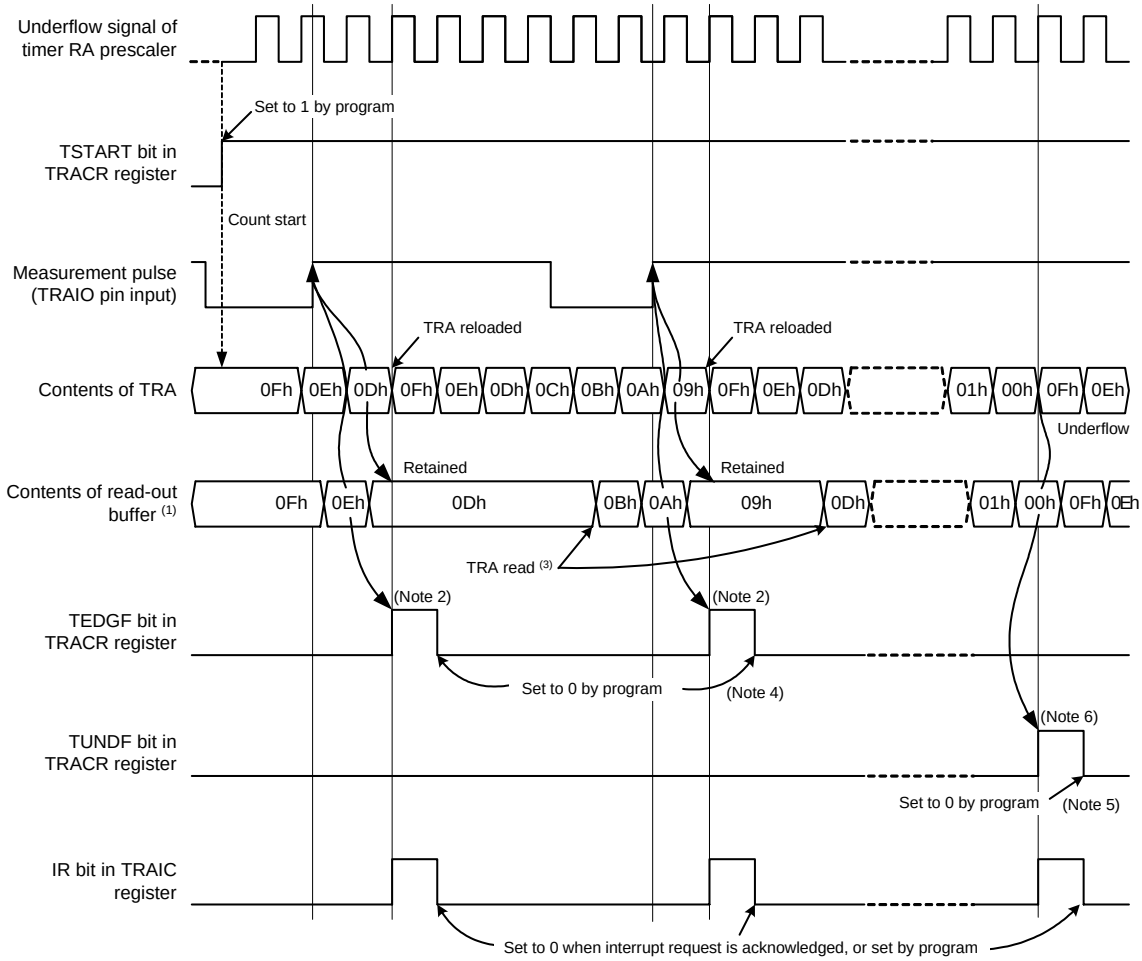
Address 0101h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIOGT1	TIOGT0	TIPF1	TIPF0	—	TOENA	TOPCR	TEDGSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	0: Measures measurement pulse from one rising edge to next rising edge 1: Measures measurement pulse from one falling edge to next falling edge	R/W
b1	TOPCR	TRAIO output control bit	Set to 0 in pulse period measurement mode.	R/W
b2	TOENA	TRAO output enable bit		R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	TIPF0	TRAIO input filter select bit (1)	b5 b4 0 0: No filter 0 1: Filter with f1 sampling 1 0: Filter with f8 sampling 1 1: Filter with f32 sampling	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit	Set to 0 in pulse period measurement mode.	R/W
b7	TIOGT1			R/W

Note:
1. When the same value from the TRAIO pin is sampled three times continuously, the input is determined.

17.7.2 Operating Example



Conditions: The period from one rising edge to the next rising edge of the measured pulse is measured (TEDGSEL = 0) with the default value of the TRA register as 0Fh.

Notes:
1. The contents of the read-out buffer can be read by reading the TRA register in pulse period measurement mode.
2. After an active edge of the measured pulse is input, the TEDGF bit in the TRACR register is set to 1 (active edge received) when the timer RA prescaler underflows for the second time.
3. The TRA register should be read before the next active edge is input after the TEDGF bit is set to 1 (active edge received). The contents in the read-out buffer are retained until the TRA register is read. If the TRA register is not read before the next active edge is input, the measured result of the previous period is retained.
4. To set to 0 by a program, use a MOV instruction to write 0 to the TEDGF bit in the TRACR register. At the same time, write 1 to the TUNDF bit in the TRACR register.
5. To set to 0 by a program, use a MOV instruction to write 0 to the TUNDF bit. At the same time, write 1 to the TEDGF bit.
6. Bits TUNDF and TEDGF are both set to 1 if timer RA underflows and reloads on an active edge simultaneously.

Figure 17.4 Operating Example of Pulse Period Measurement Mode

17.8 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse width measurement mode and pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).

  The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.
- Do not set 00h to the TRA register in pulse width measurement mode and pulse period measurement mode.

18. Timer RB

Timer RB is an 8-bit timer with an 8-bit prescaler.

18.1 Overview

The prescaler and timer each consist of a reload register and counter (refer to **Tables 18.2 to 18.5 the Specifications of Each Mode**). Timer RB has timer RB primary and timer RB secondary as reload registers.
The count source for timer RB is the operating clock that regulates the timing of timer operations such as counting and reloading.
Figure 18.1 shows a Timer RB Block Diagram. Table 18.1 lists Pin Configuration of Timer RB.

Timer RB has four operation modes listed as follows:

- Timer mode — The timer counts an internal count source (peripheral function clock or timer RA underflows).
- Programmable waveform generation mode — The timer outputs pulses of a given width successively.
- Programmable one-shot generation mode — The timer outputs a one-shot pulse.
- Programmable wait one-shot generation mode — The timer outputs a delayed one-shot pulse.

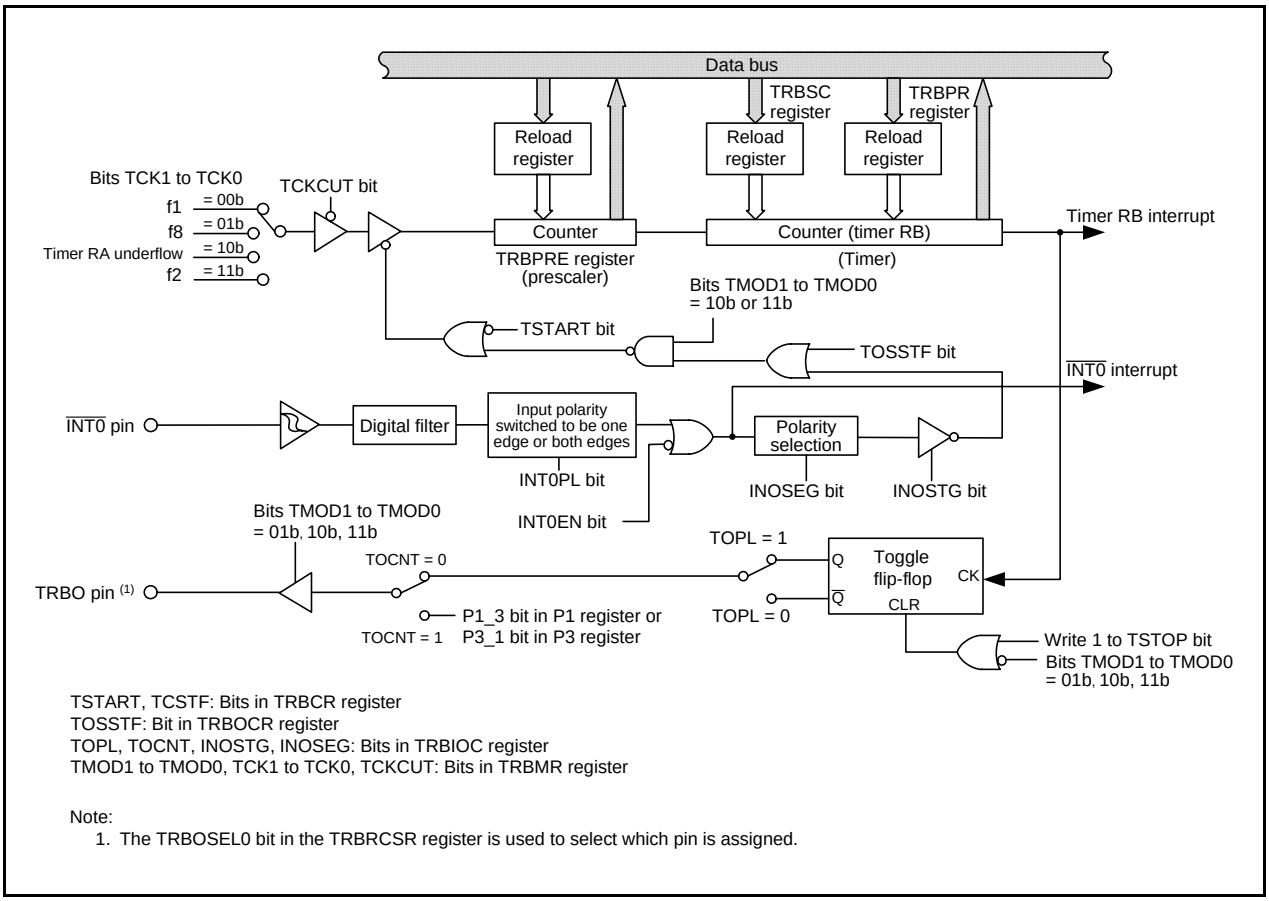


Figure 18.1 Timer RB Block Diagram

Table 18.1 Pin Configuration of Timer RB

Pin Name	Assigned Pin	I/O	Function
TRBO	P1_3 or P3_1	Output	Pulse output (programmable waveform generation mode, programmable one-shot generation mode, programmable wait one-shot generation mode)

18.2 Registers

18.2.1 Timer RB Control Register (TRBCR)

Address 0108h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TSTOP	TCSTF	TSTART
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RB count start bit (1)	0: Count stops 1: Count starts	R/W
b1	TCSTF	Timer RB count status flag (1)	0: Count stops 1: During count (3)	R
b2	TSTOP	Timer RB count forcible stop bit (1, 2)	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Notes:
1. Refer to **18.7 Notes on Timer RB** for precautions regarding bits TSTART, TCSTF and TSTOP.
2. When the TSTOP bit is set to 1, registers TRBPRE, TRBSC, TRBPR, and bits TSTART and TCSTF, and the TOSSTF bit in the TRBOCR register are set to values after a reset.
3. Indicates that count operation is in progress in timer mode or programmable waveform mode. In programmable one-shot generation mode or programmable wait one-shot generation mode, indicates that a one-shot pulse trigger can be acceptable.

18.2.2 Timer RB One-Shot Control Register (TRBOCR)

Address 0109h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	TOSSTF	TOSSP	TOSST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOSST	Timer RB one-shot start bit	When this bit is set to 1, one-shot trigger generated. When read, its content is 0.	R/W
b1	TOSSP	Timer RB one-shot stop bit	When this bit is set to 1, counting of one-shot pulses (including programmable wait one-shot pulses) stops. When read, the content is 0.	R/W
b2	TOSSTF	Timer RB one-shot status flag (1)	0: One-shot stopped 1: One-shot operating (Including wait period)	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. When 1 is set to the TSTOP bit in the TRBCR register, the TOSSTF bit is set to 0.

This register is enabled when bits TMOD1 to TMOD0 in the TRBMR register is set to 10b (programmable one-shot generation mode) or 11b (programmable wait one-shot generation mode).

18.2.3 Timer RB I/O Control Register (TRBIOC)

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	Function varies according to the operating mode.	R/W
b1	TOCNT	Timer RB output switch bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.2.4 Timer RB Mode Register (TRBMR)

Address 010Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCKCUT	—	TCK1	TCK0	TWRC	—	TMOD1	TMOD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RB operating mode select bit (1)	b1 b0 0 0: Timer mode 0 1: Programmable waveform generation mode 1 0: Programmable one-shot generation mode 1 1: Programmable wait one-shot generation mode	R/W
b1	TMOD1			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	TWRC	Timer RB write control bit (2)	0: Write to reload register and counter 1: Write to reload register only	R/W
b4	TCK0	Timer RB count source select bit (1)	b5 b4 0 0: f1 0 1: f8 1 0: Timer RA underflow (3) 1 1: f2	R/W
b5	TCK1			R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	TCKCUT	Timer RB count source cutoff bit (1)	0: Provides count source 1: Cuts off count source	R/W

Notes:
1. Change bits TMOD1 and TMOD0; TCK1 and TCK0; and TCKCUT when both the TSTART and TCSTF bits in the TRBCR register are set to 0 (count stops).
2. The TWRC bit can be set to either 0 or 1 in timer mode. In programmable waveform generation mode, programmable one-shot generation mode, or programmable wait one-shot generation mode, the TWRC bit must be set to 1 (write to reload register only).
3. To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

18.2.5 Timer RB Prescaler Register (TRBPRE)

Address 010Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source or timer RA underflows	00h to FFh	R/W
	Programmable waveform generation mode		00h to FFh	R/W
	Programmable one-shot generation mode		00h to FFh	R/W
	Programmable wait one-shot generation mode		00h to FFh	R/W

When the TSTOP bit in the TRBCR register is set to 1, the TRBPRE register is set to FFh.

18.2.6 Timer RB Secondary Register (TRBSC)

Address 010Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Disabled	00h to FFh	—
	Programmable waveform generation mode	Counts timer RB prescaler underflows (1)	00h to FFh	W (2)
	Programmable one-shot generation mode	Disabled	00h to FFh	—
	Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	W (2)

Notes:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.
2. The count value can be read out by reading the TRBPR register even when the secondary period is being counted.

When the TSTOP bit in the TRBCR register is set to 1, the TRBSC register is set to FFh.
To write to the TRBSC register, perform the following steps.
(1) Write the value to the TRBSC register.
(2) Write the value to the TRBPR register. (If the value does not change, write the same value second time.)

18.2.7 Timer RB Primary Register (TRBPR)

Address 010Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts timer RB prescaler underflows	00h to FFh	R/W
	Programmable waveform generation mode	Counts timer RB prescaler underflows (1)	00h to FFh	R/W
	Programmable one-shot generation mode	Counts timer RB prescaler underflows (one-shot width is counted)	00h to FFh	R/W
	Programmable wait one-shot generation mode	Counts timer RB prescaler underflows (wait period width is counted)	00h to FFh	R/W

Note:
1. The values of registers TRBPR and TRBSC are reloaded to the counter alternately and counted.

When the TSTOP bit in the TRBCR register is set to 1, the TRBPR register is set to FFh.

18.2.8 Timer RB/RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCCLKSEL1	TRCCLKSEL0	—	—	—	TRBOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRBOSEL0	TRBO pin select bit	0: P1_3 assigned 1: P3_1 assigned	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	TRCCLKSEL0	TRCCLK pin select bit	b5 b4 0 0: TRCCLK pin not used 0 1: P1_4 assigned 1 0: P3_3 assigned 1 1: Do not set.	R/W
b5	TRCCLKSEL1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRBRCSR register selects which pin is assigned to the timer RB and timer RC I/O. To use the I/O pin for timer RB and timer RC, set this register.
Set the TRBOSEL0 bit before setting the timer RB associated registers. Set bits TRCCLKSEL0 to TRCCLKSEL1 before setting the timer RC associated registers. Also, do not change the setting values of the TRBOSEL0 bit during timer RB operation. Do not change the setting values of bits TRCCLKSEL0 to TRCCLKSEL1 during timer RC operation.

18.3 Timer Mode

In timer mode, a count source which is internally generated or timer RA underflows are counted (refer to **Table 18.2 Timer Mode Specifications**). Registers TRBOCR and TRBSC are not used in timer mode.

Table 18.2 Timer Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the reload register contents before the count continues (when timer RB underflows, the contents of timer RB primary reload register is reloaded).
Divide ratio	1/(n+1)(m+1) n: setting value in TRBPRE register, m: setting value in TRBPR register
Count start condition	1 (count starts) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	When timer RB underflows [timer RB interrupt].
TRBO pin function	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written to while count operation is in progress: If the TWRC bit in the TRBMR register is set to 0, the value is written to both the reload register and the counter. If the TWRC bit is set to 1, the value is written to the reload register only (refer to **18.3.2 Timer Write Control during Count Operation**).

18.3.1 Timer RB I/O Control Register (TRBIOC) in Timer Mode

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	Set to 0 in timer mode.	R/W
b1	TOCNT	Timer RB output switch bit		R/W
b2	INOSTG	One-shot trigger control bit		R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.3.2 Timer Write Control during Count Operation

Timer RB has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. In timer mode, the TWRC bit in the TRBMR register can be used to select whether writing to the prescaler or timer during count operation is performed to both the reload register and counter or only to the reload register.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, even if the TWRC bit is set for writing to both the reload register and counter, the counter value is not updated immediately after the WRITE instruction is executed. In addition, if the TWRC bit is set for writing to the reload register only, the synchronization of the writing will be shifted if the prescaler value changes. Figure 18.2 shows an Operating Example of Timer RB when Counter Value is Rewritten during Count Operation.

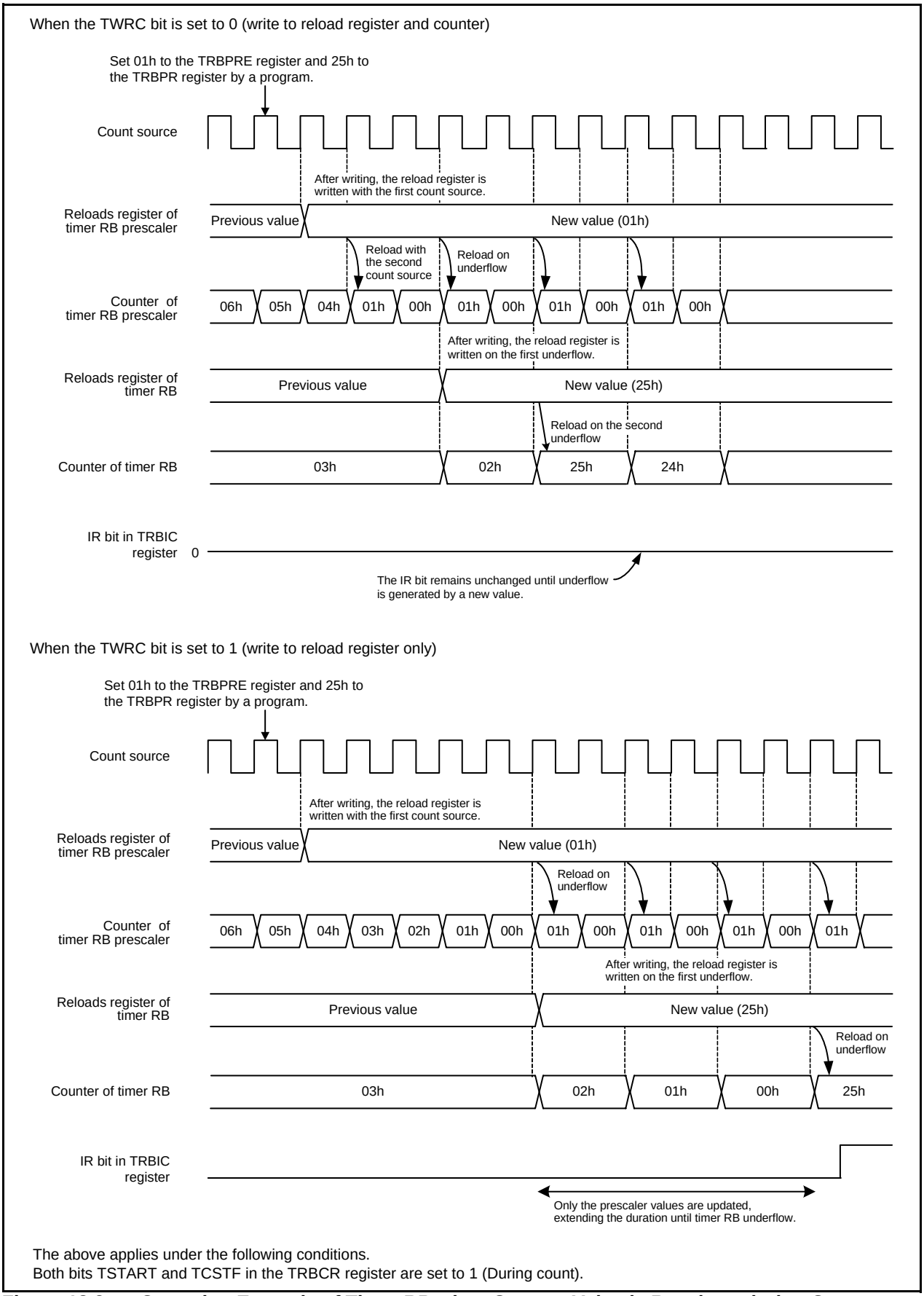


Figure 18.2 Operating Example of Timer RB when Counter Value is Rewritten during Count Operation

18.4 Programmable Waveform Generation Mode

In programmable waveform generation mode, the signal output from the TRBO pin is inverted each time the counter underflows, while the values in registers TRBPR and TRBSC are counted alternately (refer to **Table 18.3 Programmable Waveform Generation Mode Specifications**). Counting starts by counting the setting value in the TRBPR register. The TRBOCR register is unused in this mode.
Figure 18.3 shows an Operating Example of Timer RB in Programmable Waveform Generation Mode.

Table 18.3 Programmable Waveform Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement • When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.
Width and period of output waveform	Primary period: (n+1)(m+1)/fi Secondary period: (n+1)(p+1)/fi Period: (n+1){(m+1)+(p+1)}/fi fi: Count source frequency n: Value set in TRBPRE register, m: Value set in TRBPR register p: Value set in TRBSC register
Count start condition	1 (count start) is written to the TSTART bit in the TRBCR register.
Count stop conditions	• 0 (count stop) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.
Interrupt request generation timing	In half a cycle of the count source, after timer RB underflows during the secondary period (at the same time as the TRBO output change) [timer RB interrupt]
TRBO pin function	Programmable output port or pulse output
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE. (1)
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only. (2)
Selectable functions	• Output level select function The output level during primary and secondary periods is selected by the TOPL bit in the TRBIOC register. • TRBO pin output switch function Timer RB pulse output or P3_1 (P1_3) latch output is selected by the TOCNT bit in the TRBIOC register. (3)

Notes:
1. Even when counting the secondary period, the TRBPR register may be read.
2. The set values are reflected in the waveform output beginning with the following primary period after writing to the TRBPR register.
3. The value written to the TOCNT bit is enabled by the following.
   • When counting starts.
   • When a timer RB interrupt request is generated.
   The contents after the TOCNT bit is changed are reflected from the output of the following primary period.

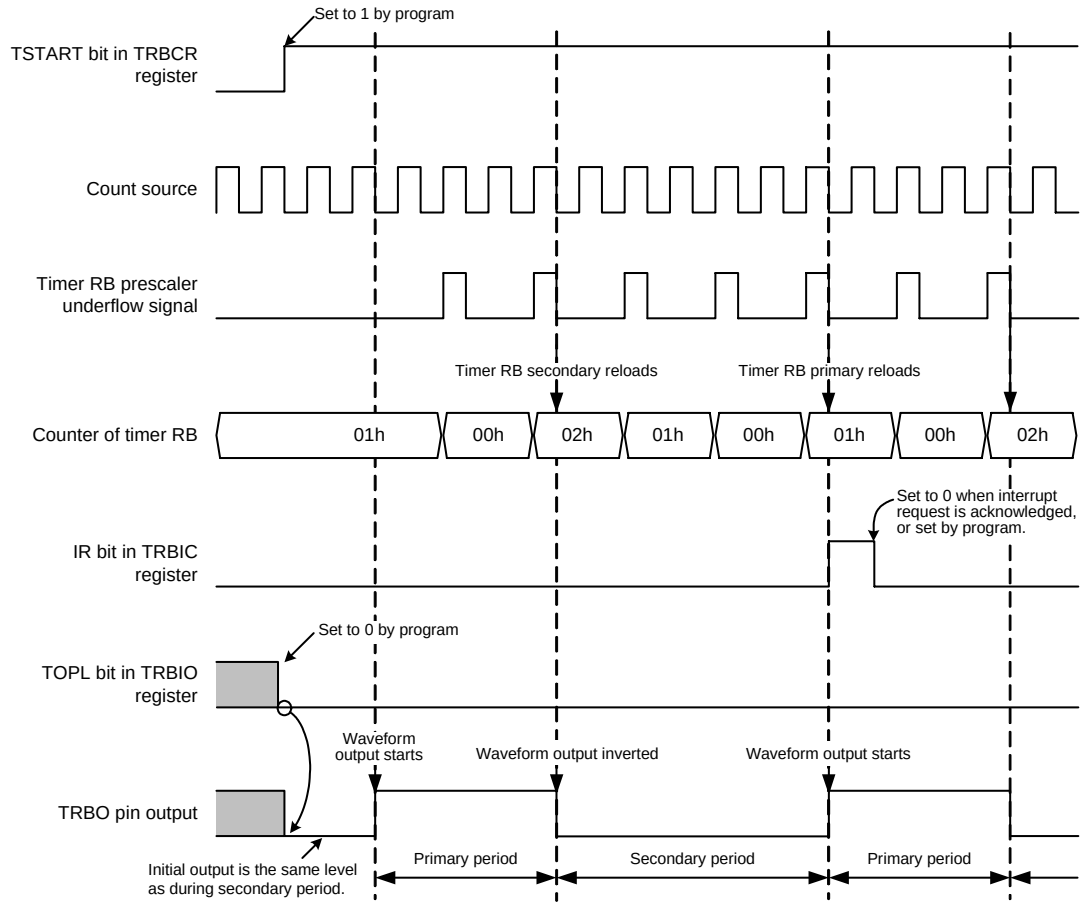
18.4.1 Timer RB I/O Control Register (TRBIOC) in Programmable Waveform Generation Mode

Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: Outputs “H” for primary period Outputs “L” for secondary period Outputs “L” when the timer is stopped 1: Outputs “L” for primary period Outputs “H” for secondary period Outputs “H” when the timer is stopped	R/W
b1	TOCNT	Timer RB output switch bit	0: Outputs timer RB waveform 1: Outputs value in P3_1 (P1_3) port register	R/W
b2	INOSTG	One-shot trigger control bit	Set to 0 in programmable waveform generation mode.	R/W
b3	INOSEG	One-shot trigger polarity select bit		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

18.4.2 Operating Example



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h, TRBSC = 02h
TRBIOC register TOCNT = 0 (timer RB waveform is output from the TRBO pin)

Figure 18.3 Operating Example of Timer RB in Programmable Waveform Generation Mode

18.5 Programmable One-shot Generation Mode

In programmable one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to **Table 18.4 Programmable One-Shot Generation Mode Specifications**). When a trigger is generated, the timer starts operating from the point only once for a given period equal to the set value in the TRBPR register. The TRBSC register is not used in this mode.
Figure 18.4 shows an Operating Example of Programmable One-Shot Generation Mode.

Table 18.4 Programmable One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement the setting value in the TRBPR register • When the timer underflows, it reloads the contents of the reload register before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.
One-shot pulse output time	(n+1)(m+1)/fi fi: Count source frequency, n: Setting value in TRBPRE register, m: Setting value in TRBPR register
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts) • Input trigger to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during primary period • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops) • When the TSTART bit in the TRBCR register is set to 0 (stops counting) • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting)
Interrupt request generation timing	In half a cycle of the count source, after the timer underflows (at the same time as the TRBO output ends) [timer RB interrupt]
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE and TRBPR are written while the count is stopped, values are written to both the reload register and counter. • When registers TRBPRE and TRBPR are written during the count, values are written to the reload register only (the data is transferred to the counter at the following reload). (1)
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register. • One-shot trigger select function Refer to **18.5.3 One-Shot Trigger Selection**.

Note:
1. The set value is reflected at the following one-shot pulse after writing to the TRBPR register.

18.5.1 Timer RB I/O Control Register (TRBIOC) in Programmable One-Shot Generation Mode

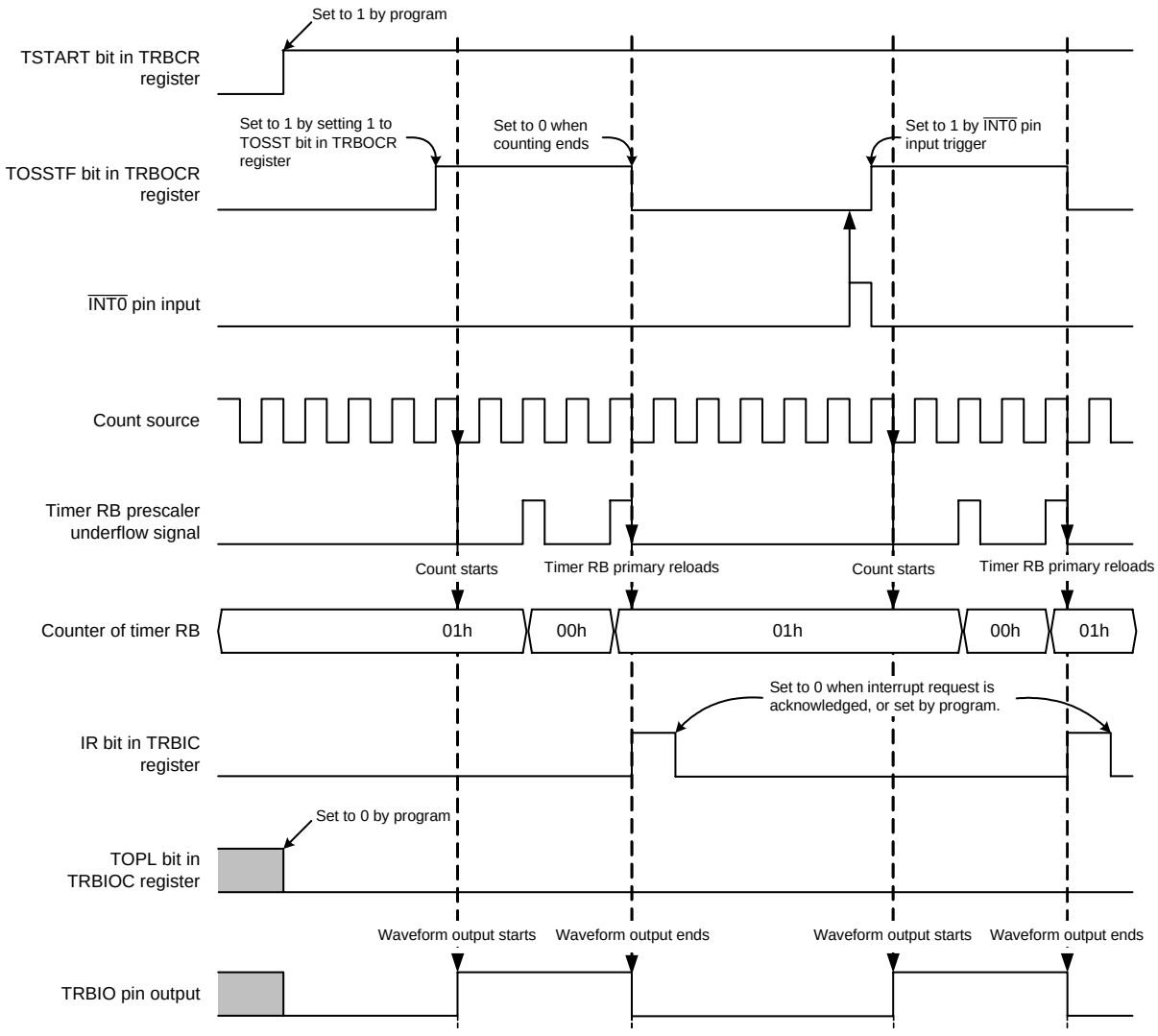
Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: Outputs one-shot pulse “H” Outputs “L” when the timer is stopped 1: Outputs one-shot pulse “L” Outputs “H” when the timer is stopped	R/W
b1	TOCNT	Timer RB output switch bit	Set to 0 in programmable one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INT0}}$ pin one-shot trigger disabled 1: $\overline{\text{INT0}}$ pin one-shot trigger enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **18.5.3 One-Shot Trigger Selection**.

18.5.2 Operating Example



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h
TRBIOC register TOPL = 0, TOCNT = 0
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at rising edge)

Figure 18.4 Operating Example of Programmable One-Shot Generation Mode

18.5.3 One-Shot Trigger Selection

In programmable one-shot generation mode and programmable wait one-shot generation mode, operation starts when a one-shot trigger is generated while the TCSTF bit in the TRBCR register is set to 1 (count starts).
A one-shot trigger can be generated by either of the following causes:

- 1 is written to the TOSST bit in the TRBOCR register by a program.
- Trigger input from the $\overline{\text{INT0}}$ pin.

When a one-shot trigger occurs, the TOSSTF bit in the TRBOCR register is set to 1 (one-shot operation in progress) after one or two cycles of the count source have elapsed. Then, in programmable one-shot generation mode, count operation begins and one-shot waveform output starts. (In programmable wait one-shot generation mode, count operation starts for the wait period.) If a one-shot trigger occurs while the TOSSTF bit is set to 1, no retriggering occurs.

To use trigger input from the $\overline{\text{INT0}}$ pin, input the trigger after making the following settings:

- Set the PD4_5 bit in the PD4 register to 0 (input port).
- Select the $\overline{\text{INT0}}$ digital filter with bits INT0F1 and INT0F0 in the INTF register.
- Select both edges or one edge with the INT0PL bit in INTEN register. If one edge is selected, further select falling or rising edge with the INOSEG bit in TRBIOC register.
- Set the INT0EN bit in the INTEN register to 1 (enabled).
- After completing the above, set the INOSTG bit in the TRBIOC register to 1 ($\overline{\text{INT0}}$ pin one-shot trigger enabled).

Note the following points with regard to generating interrupt requests by trigger input from the $\overline{\text{INT0}}$ pin.

- Processing to handle the interrupts is required. Refer to **11. Interrupts**, for details.
- If one edge is selected, use the POL bit in the INT0IC register to select falling or rising edge. (The INOSEG bit in the TRBIOC register does not affect $\overline{\text{INT0}}$ interrupts).
- If a one-shot trigger occurs while the TOSSTF bit is set to 1, timer RB operation is not affected, but the value of the IR bit in the INT0IC register changes.

18.6 Programmable Wait One-Shot Generation Mode

In programmable wait one-shot generation mode, a one-shot pulse is output from the TRBO pin by a program or an external trigger input (input to the $\overline{\text{INT0}}$ pin) (refer to **Table 18.5 Programmable Wait One-Shot Generation Mode Specifications**). When a trigger is generated from that point, the timer outputs a pulse only once for a given length of time equal to the setting value in the TRBSC register after waiting for a given length of time equal to the setting value in the TRBPR register.
Figure 18.5 shows an Operating Example of Programmable Wait One-Shot Generation Mode.

Table 18.5 Programmable Wait One-Shot Generation Mode Specifications

Item	Specification
Count sources	f1, f2, f8, timer RA underflow
Count operations	• Decrement the timer RB primary setting value. • When a count of the timer RB primary underflows, the timer reloads the contents of timer RB secondary before the count continues. • When a count of the timer RB secondary underflows, the timer reloads the contents of timer RB primary before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.
Wait time	(n+1)(m+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, m Value set in the TRBPR register
One-shot pulse output time	(n+1)(p+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, p: Value set in the TRBSC register
Count start conditions	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated. • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts). • Input trigger to the $\overline{\text{INT0}}$ pin
Count stop conditions	• When reloading completes after timer RB underflows during secondary period. • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops). • When the TSTART bit in the TRBCR register is set to 0 (starts counting). • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting).
Interrupt request generation timing	In half a cycle of the count source after timer RB underflows during secondary period (complete at the same time as waveform output from the TRBO pin) [timer RB interrupt].
TRBO pin function	Pulse output
$\overline{\text{INT0}}$ pin functions	• When the INOSTG bit in the TRBIOC register is set to 0 ($\overline{\text{INT0}}$ one-shot trigger disabled): programmable I/O port or $\overline{\text{INT0}}$ interrupt input • When the INOSTG bit in the TRBIOC register is set to 1 ($\overline{\text{INT0}}$ one-shot trigger enabled): external trigger ($\overline{\text{INT0}}$ interrupt input)
Read from timer	The count value can be read out by reading registers TRBPR and TRBPRE.
Write to timer	• When registers TRBPRE, TRBSC, and TRBPR are written while the count stops, values are written to both the reload register and counter. • When registers TRBPRE, TRBSC, and TRBPR are written to during count operation, values are written to the reload registers only. (1)
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register. • One-shot trigger select function Refer to **18.5.3 One-Shot Trigger Selection**.

Note:
1. The set value is reflected at the following one-shot pulse after writing to registers TRBSC and TRBPR.

18.6.1 Timer RB I/O Control Register (TRBIOC) in Programmable Wait One-Shot Generation Mode

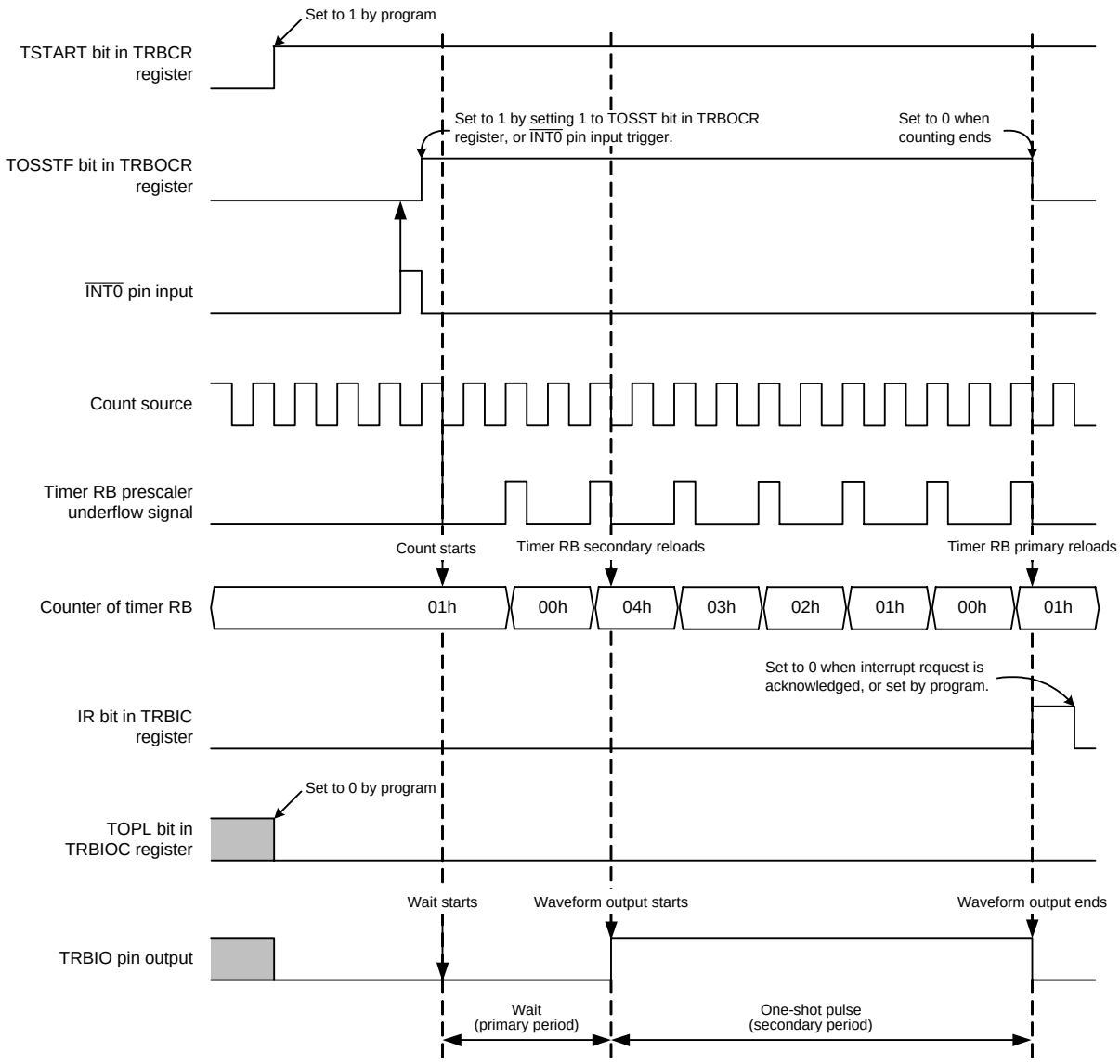
Address 010Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	INOSEG	INOSTG	TOCNT	TOPL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOPL	Timer RB output level select bit	0: Outputs one-shot pulse “H” Outputs “L” when the timer stops or during wait 1: Outputs one-shot pulse “L” Outputs “H” when the timer stops or during wait	R/W
b1	TOCNT	Timer RB output switch bit	Set to 0 in programmable wait one-shot generation mode.	R/W
b2	INOSTG	One-shot trigger control bit (1)	0: $\overline{\text{INT0}}$ pin one-shot trigger disabled 1: $\overline{\text{INT0}}$ pin one-shot trigger enabled	R/W
b3	INOSEG	One-shot trigger polarity select bit (1)	0: Falling edge trigger 1: Rising edge trigger	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

Note:
1. Refer to **18.5.3 One-Shot Trigger Selection**.

18.6.2 Operating Example



The above applies under the following conditions.

TRBPRE = 01h, TRBPR = 01h, TRBSC = 04h
INOSTG = 1 (INT0 one-shot trigger enabled)
INOSEG = 1 (edge trigger at rising edge)

Figure 18.5 Operating Example of Programmable Wait One-Shot Generation Mode

18.7 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit. Timer RB starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

18.7.1 Timer Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

18.7.2 Programmable Waveform Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

18.7.3 Programmable One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

18.7.4 Programmable Wait One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

19. Timer RC

Timer RC is a 16-bit timer with four I/O pins.

19.1 Overview

Timer RC uses f1 as its operation clock. Table 19.1 lists the Timer RC Operation Clock.

Table 19.1 Timer RC Operation Clock

Condition	Timer RC Operation Clock
Count source is f1, f2, f4, f8, f32, or TRCCLK input (bits TCK2 to TCK0 in TRCCR1 register are set to a value from 000b to 101b)	f1

Table 19.2 lists the Pin Configuration of Timer RC and Figure 19.1 shows a Timer RC Block Diagram.
Timer RC has three modes.

- Timer mode
  - Input capture function — The counter value is captured to a register, using an external signal as the trigger.
  - Output compare function — Matches between the counter and register values are detected. (Pin output state changes when a match is detected.)

The following two modes use the output compare function.

- PWM mode — Pulses of a given width are output continuously.
- PWM2 mode — A one-shot waveform or PWM waveform is output following the trigger after the wait time has elapsed.

Input capture function, output compare function, and PWM mode settings may be specified independently for each pin.
In PWM2 mode waveforms are output based on a combination of the counter or the register.

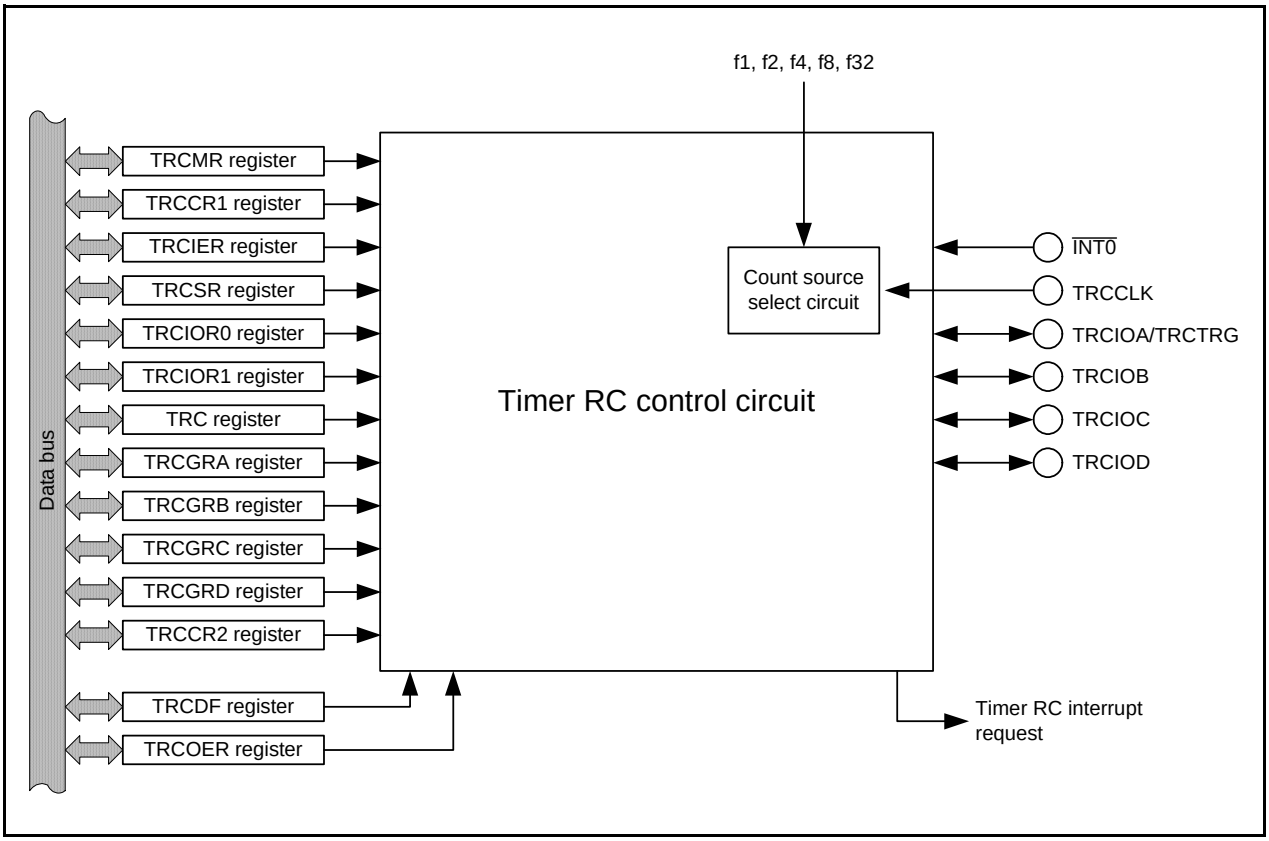


Figure 19.1 Timer RC Block Diagram

Table 19.2 Pin Configuration of Timer RC

Pin Name	Assigned Pin	I/O	Function
TRCIOA	P1_1	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details.
TRCIOB	P0_4 or P1_2		
TRCIOC	P1_3, or P3_4		
TRCIOD	P1_0, or P3_5		
TRCCLK	P1_4, or P3_3	Input	External clock input
TRCTRG	P1_1	Input	PWM2 mode external trigger input

19.2 Registers

Table 19.3 lists the Registers Associated with Timer RC.

Table 19.3 Registers Associated with Timer RC

Address	Symbol	Mode				Related Information
		Timer		PWM	PWM2	
		Input Capture Function	Output Compare Function			
0008h	MSTCR	Valid	Valid	Valid	Valid	19.2.1 Module Standby Control Register (MSTCR)
0120h	TRCMR	Valid	Valid	Valid	Valid	19.2.2 Timer RC Mode Register (TRCMR)
0121h	TRCCR1	Valid	Valid	Valid	Valid	Timer RC control register 1 19.2.3 Timer RC Control Register 1 (TRCCR1) 19.5.1 Timer RC Control Register 1 (TRCCR1) for Output Compare Function 19.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode 19.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode
0122h	TRCIER	Valid	Valid	Valid	Valid	19.2.4 Timer RC Interrupt Enable Register (TRCIER)
0123h	TRCSR	Valid	Valid	Valid	Valid	19.2.5 Timer RC Status Register (TRCSR)
0124h	TRCIOR0	Valid	Valid	—	—	Timer RC I/O control register 0, timer RC I/O control register 1 19.2.6 Timer RC I/O Control Register 0 (TRCIOR0) 19.2.7 Timer RC I/O Control Register 1 (TRCIOR1) 19.4.1 Timer RC I/O Control Register 0 (TRCIOR0) for Input Capture Function 19.4.2 Timer RC I/O Control Register 1 (TRCIOR1) for Input Capture Function 19.5.2 Timer RC I/O Control Register 0 (TRCIOR0) for Output Compare Function 19.5.3 Timer RC I/O Control Register 1 (TRCIOR1) for Output Compare Function
0125h	TRCIOR1					
0126h 0127h	TRC	Valid	Valid	Valid	Valid	19.2.8 Timer RC Counter (TRC)
0128h 0129h	TRCGRA	Valid	Valid	Valid	Valid	19.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)
012Ah 012Bh	TRCGRB					
012Ch 012Dh	TRCGRC					
012Eh 012Fh	TRCGRD					
0130h	TRCCR2	—	Valid	Valid	Valid	19.2.10 Timer RC Control Register 2 (TRCCR2)
0131h	TRCDF	Valid	—	—	Valid	19.2.11 Timer RC Digital Filter Function Select Register (TRCDF)
0132h	TRCOER	—	Valid	Valid	Valid	19.2.12 Timer RC Output Master Enable Register (TRCOER)
0181h	TRBRCSR	Valid	Valid	Valid	Valid	19.2.13 Timer RB/RC Pin Select Register (TRBRCSR)
0182h	TRCPSR0	Valid	Valid	Valid	Valid	19.2.14 Timer RC Pin Select Register 0 (TRCPSR0)
0183h	TRCPSR1	Valid	Valid	Valid	Valid	19.2.15 Timer RC Pin Select Register 1 (TRCPSR1)

—: Invalid

19.2.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRC	—	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (2)	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. Stop the SSU and the I2C bus functions before setting to standby. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. Stop the timer RC function before setting to standby. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0132h) is disabled.

19.2.2 Timer RC Mode Register (TRCMR)

Address 0120h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	—	BFD	BFC	PWM2	PWMD	PWMC	PWMB
After Reset	0	1	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	PWMB	PWM mode of TRCIOB select bit (1)	0: Timer mode 1: PWM mode	R/W
b1	PWMC	PWM mode of TRCIOC select bit (1)	0: Timer mode 1: PWM mode	R/W
b2	PWMD	PWM mode of TRCIOD select bit (1)	0: Timer mode 1: PWM mode	R/W
b3	PWM2	PWM2 mode select bit	0: PWM 2 mode 1: Timer mode or PWM mode	R/W
b4	BFC	TRCGRC register function select bit (2)	0: General register 1: Buffer register of TRCGRA register	R/W
b5	BFD	TRCGRD register function select bit	0: General register 1: Buffer register of TRCGRB register	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	TSTART	TRC count start bit	0: Count stops 1: Count starts	R/W

Notes:
1. These bits are enabled when the PWM2 bit is set to 1 (timer mode or PWM mode).
2. Set the BFC bit to 0 (general register) in PWM2 mode.

For notes on PWM2 mode, refer to **19.9.5 TRCMR Register in PWM2 Mode**.

19.2.3 Timer RC Control Register 1 (TRCCR1)

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Function varies according to the operating mode (function).	R/W
b1	TOB	TRCIOB output level select bit (1)		R/W
b2	TOC	TRCIOC output level select bit (1)		R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear TRC counter by input capture or by compare match in TRCGRA	R/W

Note:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).

19.2.4 Timer RC Interrupt Enable Register (TRCIER)

Address 0122h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVIE	—	—	—	IMIED	IMIEC	IMIEB	IMIEA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	R/W
b1	IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	R/W
b2	IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	R/W
b3	IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVIE	Overflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit 1: Enable interrupt (OVI) by the OVF bit	R/W

19.2.5 Timer RC Status Register (TRCSR)

Address 0123h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	OVF	—	—	—	IMFD	IMFC	IMFB	IMFA
After Reset	0	1	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read. (1) [Source for setting this bit to 1] Refer to **Table 19.4 Source for Setting Bit of Each Flag to 1**.	R/W
b1	IMFB	Input capture/compare match flag B		R/W
b2	IMFC	Input capture/compare match flag C		R/W
b3	IMFD	Input capture/compare match flag D		R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read. (1) [Source for setting this bit to 1] Refer to **Table 19.4 Source for Setting Bit of Each Flag to 1**.	R/W

Note:
1. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.

Table 19.4 Source for Setting Bit of Each Flag to 1

Bit Symbol	Timer Mode		PWM Mode	PWM2 Mode
	Input Capture Function	Output Compare Function		
IMFA	TRCIOA pin input edge (1)	When the values of the registers TRC and TRCGRA match.		
IMFB	TRCIOB pin input edge (1)	When the values of the registers TRC and TRCGRB match.		
IMFC	TRCIOC pin input edge (1)	When the values of the registers TRC and TRCGRC match. (2)		
IMFD	TRCIOD pin input edge (1)	When the values of the registers TRC and TRCGRD match. (2)		
OVF	When the TRC register overflows.			

Notes:
1. Edge selected by bits IOj1 to IOj0 (j = A, B, C, or D).
2. Includes the condition that bits BFC and BFD in the TRCMR register are set to 1 (buffer registers of registers TRCGRA and TRCGRB).

19.2.6 Timer RC I/O Control Register 0 (TRCIOR0)

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	Function varies according to the operating mode (function).	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOA3	TRCGRA input capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA pin input	R/W
b4	IOB0	TRCGRB control bit	Function varies according to the operating mode (function).	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

The TRCIOR0 register is enabled in timer mode. It is disabled in modes PWM and PWM2.

19.2.7 Timer RC I/O Control Register 1 (TRCIOR1)

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	Function varies according to the operating mode (function).	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	0: Output compare function 1: Input capture function	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	Function varies according to the operating mode (function).	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	0: Output compare function 1: Input capture function	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

The TRCIOR1 register is enabled in timer mode. It is disabled in modes PWM and PWM2.

19.2.8 Timer RC Counter (TRC)

Address 0127h to 0126h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	Setting Range	R/W
b15 to b0	Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRCSR register is set to 1.	0000h to FFFFh	R/W

Access the TRC register in 16-bit units. Do not access it in 8-bit units.

19.2.9 Timer RC General Registers A, B, C, and D (TRCGRA, TRCGRB, TRCGRC, TRCGRD)

Address 0129h to 0128h (TRCGRA), 012Bh to 012Ah (TRCGRB), 012Dh to 012Ch (TRCGRC), 012Fh to 012Eh (TRCGRD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b15 to b0	Function varies according to the operating mode.	R/W

Access registers TRCGRA to TRCGRD in 16-bit units. Do not access them in 8-bit units.

19.2.10 Timer RC Control Register 2 (TRCCR2)

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in the output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.5 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

19.2.11 Timer RC Digital Filter Function Select Register (TRCDF)

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)		R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)		R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)		R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)		R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Clock select bits for digital filter function (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

19.2.12 Timer RC Output Master Enable Register (TRCOER)

Address 0132h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	PTO	—	—	—	ED	EC	EB	EA
After Reset	0	1	1	1	1	1	1	1

Bit	Symbol	Bit Name	Function	R/W
b0	EA	TRCIOA output disable bit (1)	0: Enable output 1: Disable output (The TRCIOA pin is used as a programmable I/O port.)	R/W
b1	EB	TRCIOB output disable bit (1)	0: Enable output 1: Disable output (The TRCIOB pin is used as a programmable I/O port.)	R/W
b2	EC	TRCIOC output disable bit (1)	0: Enable output 1: Disable output (The TRCIOC pin is used as a programmable I/O port.)	R/W
b3	ED	TRCIOD output disable bit (1)	0: Enable output 1: Disable output (The TRCIOD pin is used as a programmable I/O port.)	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	PTO	$\overline{\text{INT0}}$ of pulse output forced cutoff signal input enabled bit	0: Pulse output forced cutoff input disabled 1: Pulse output forced cutoff input enabled (Bits EA, EB, EC, and ED are set to 1 (disable output) when “L” is applied to the $\overline{\text{INT0}}$ pin)	R/W

Note:
1. These bits are disabled for input pins set to the input capture function.

19.2.13 Timer RB/RC Pin Select Register (TRBRCSR)

Address 0181h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	TRCCLKSEL1	TRCCLKSEL0	—	—	—	TRBOSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRBOSEL0	TRBO pin select bit	0: P1_3 assigned 1: P3_1 assigned	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	TRCCLKSEL0	TRCCLK pin select bit	b5 b4 0 0: TRCCLK pin not used 0 1: P1_4 assigned 1 0: P3_3 assigned 1 1: Do not set.	R/W
b5	TRCCLKSEL1			R/W
b6	—	Reserved bit	Set to 0.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRBRCSR register selects which pin is assigned to the timer RB and timer RC I/O. To use the I/O pin for timer RB and timer RC, set this register.

Set the TRBOSEL0 bit before setting the timer RB associated registers. Set bits TRCCLKSEL0 to TRCCLKSEL1 before setting the timer RC associated registers. Also, do not change the setting values of the TRBOSEL0 bit during timer RB operation. Do not change the setting values of bits TRCCLKSEL0 to TRCCLKSEL1 during timer RC operation.

19.2.14 Timer RC Pin Select Register 0 (TRCPSR0)

Address 0182h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIOBSEL2	TRCIOBSEL1	TRCIOBSEL0	—	TRCIOASEL2	TRCIOASEL1	TRCIOASEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOASEL0	TRCIOA/TRCTRG pin select bit	b2 b1 b0 0 0 0: TRCIOA/TRCTRG pin not used 0 0 1: P1_1 assigned Other than above: Do not set.	R/W
b1	TRCIOASEL1			R/W
b2	TRCIOASEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIOBSEL0	TRCIOB pin select bit	b6 b5 b4 0 0 0: TRCIOB pin not used 0 0 1: P1_2 assigned 0 1 1: P0_4 assigned Other than above: Do not set.	R/W
b5	TRCIOBSEL1			R/W
b6	TRCIOBSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR0 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR0 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

19.2.15 Timer RC Pin Select Register 1 (TRCPSR1)

Address 0183h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TRCIODSEL2	TRCIODSEL1	TRCIODSEL0	—	TRCIOCSEL2	TRCIOCSEL1	TRCIOCSEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TRCIOCSEL0	TRCIOC pin select bit	b2 b1 b0 0 0 0: TRCIOC pin not used 0 0 1: P1_3 assigned 0 1 0: P3_4 assigned Other than above: Do not set.	R/W
b1	TRCIOCSEL1			R/W
b2	TRCIOCSEL2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	TRCIODSEL0	TRCIOD pin select bit	b6 b5 b4 0 0 0: TRCIOD pin not used 0 0 1: P1_0 assigned 0 1 0: P3_5 assigned Other than above: Do not set.	R/W
b5	TRCIODSEL1			R/W
b6	TRCIODSEL2			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

The TRCPSR1 register selects which pin is assigned to the timer RC I/O. To use the I/O pin for timer RC, set this register.
Set the TRCPSR1 register before setting the timer RC associated registers. Also, do not change the setting value in this register during timer RC operation.

19.3 Common Items for Multiple Modes

19.3.1 Count Source

The method of selecting the count source is common to all modes.
Table 19.5 lists the Count Source Selection and Figure 19.2 shows a Count Source Block Diagram.

Table 19.5 Count Source Selection

Count Source	Selection Method
f1, f2, f4, f8, f32	Count source selected using bits TCK2 to TCK0 in TRCCR1 register
External signal input to TRCCLK pin	Bits TCK2 to TCK0 in TRCCR1 register are set to 101b (count source is rising edge of external clock) and the corresponding direction bit in the corresponding direction register is set to 0 (input mode)

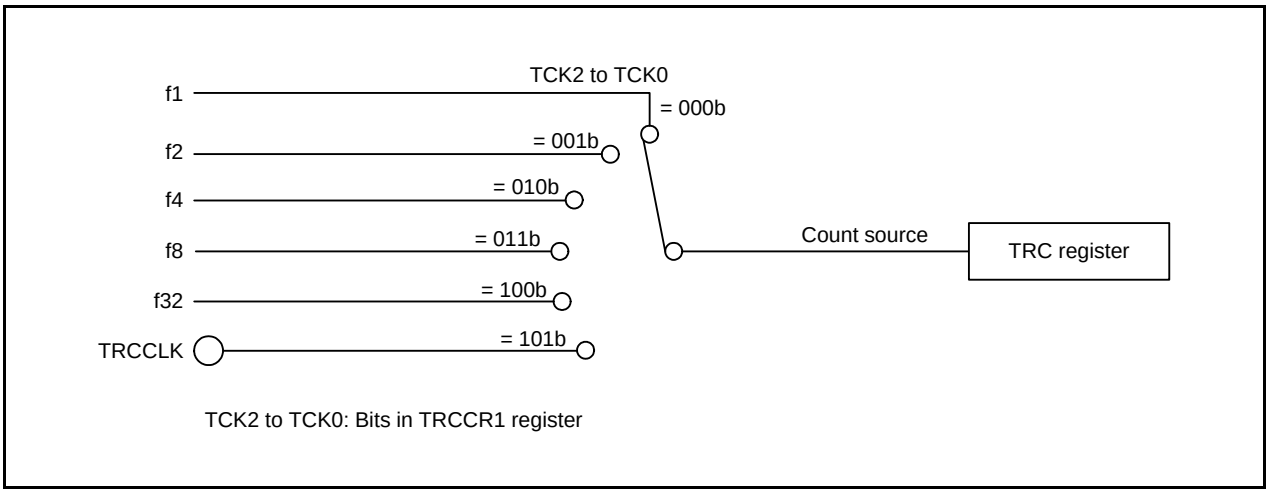


Figure 19.2 Count Source Block Diagram

The pulse width of the external clock input to the TRCCLK pin should be three cycles or more of the timer RC operation clock (refer to **Table 19.1 Timer RC Operation Clock**).

19.3.2 Buffer Operation

Bits BFC and BFD in the TRCMR register are used to select the TRCGRC or TRCGRD register as the buffer register for the TRCGRA or TRCGRB register.

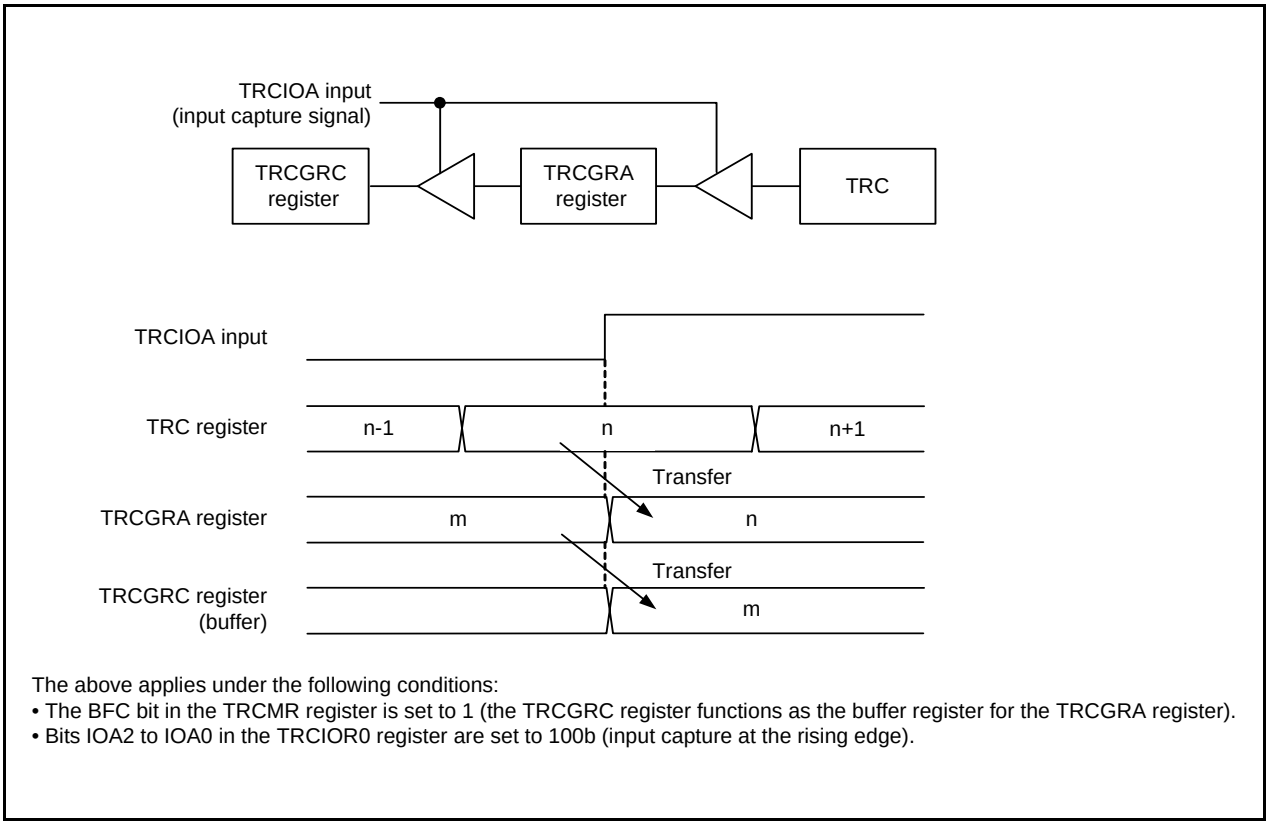
- Buffer register for TRCGRA register: TRCGRC register
- Buffer register for TRCGRB register: TRCGRD register

Buffer operation differs depending on the mode.

Table 19.6 lists the Buffer Operation in Each Mode, Figure 19.3 shows the Buffer Operation for Input Capture Function, and Figure 19.4 shows the Buffer Operation for Output Compare Function.

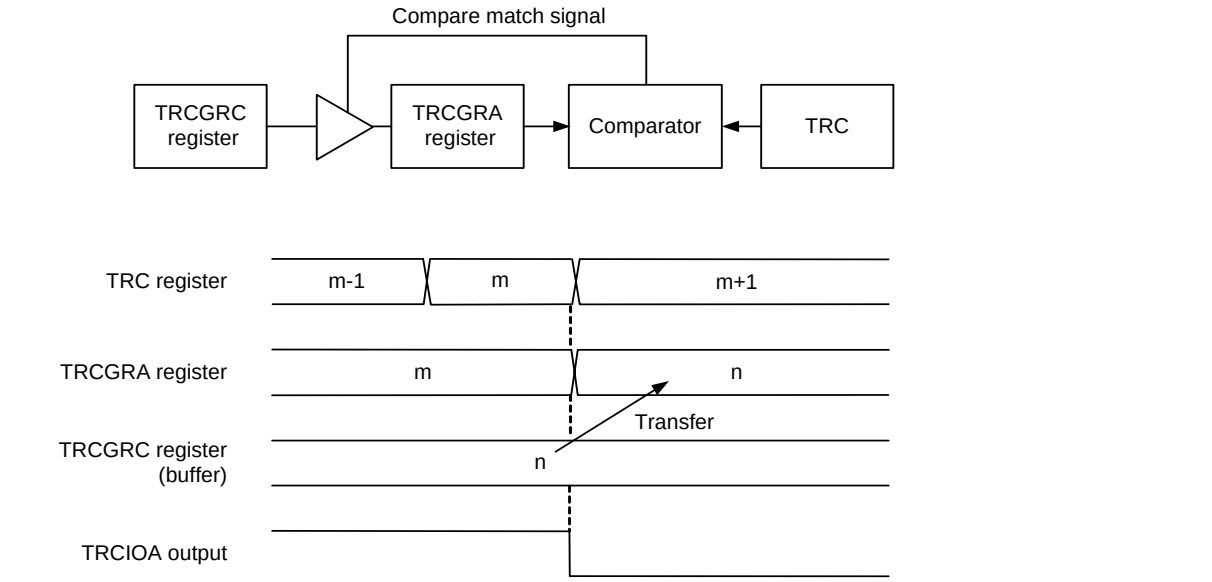
Table 19.6 Buffer Operation in Each Mode

Function, Mode	Transfer Timing	Transfer Destination Register
Input capture function	Input capture signal input	Contents of TRCGRA (TRCGRB) register are transferred to buffer register
Output compare function PWM mode	Compare match between TRC register and TRCGRA (TRCGRB) register	Contents of buffer register are transferred to TRCGRA (TRCGRB) register
PWM2 mode	• Compare match between TRC register and TRCGRA register • TRCTRG pin trigger input	Contents of buffer register (TRCGRD) are transferred to TRCGRB register



The above applies under the following conditions:
- The BFC bit in the TRCMR register is set to 1 (the TRCGRC register functions as the buffer register for the TRCGRA register).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 100b (input capture at the rising edge).

Figure 19.3 Buffer Operation for Input Capture Function



The above applies under the following conditions:
- The BFC bit in the TRCMR register is set to 1 (the TRCGRC register functions as the buffer register for the TRCGRA register).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 001b (“L” output by compare match).

Figure 19.4 Buffer Operation for Output Compare Function

Make the following settings in timer mode.
- To use the TRCGRC register as the buffer register for the TRCGRA register:
  Set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
- To use the TRCGRD register as the buffer register for the TRCGRB register:
  Set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

If the TRCGRC or TRCGRD register is functioning as a buffer register for the output compare function, PWM mode or PWM2 mode, the IMFC bit or IMFD bit in the TRCSR register is set to 1 when a compare match with the TRC register occurs.
If the TRCGRC or TRCGRD register is functioning as a buffer register for the input capture function, the IMFC bit or IMFD bit in the TRCSR register is set to 1 at the input edge of a signal input to the TRCIOC pin or TRCIOD pin.

19.3.3 Digital Filter

The input to TRCTRG or TRCIOj (j = A, B, C, or D) is sampled, and the level is considered to be determined when three matches occur. The digital filter function and sampling clock are selected using the TRCDF register. Figure 19.5 shows a Digital Filter Block Diagram.

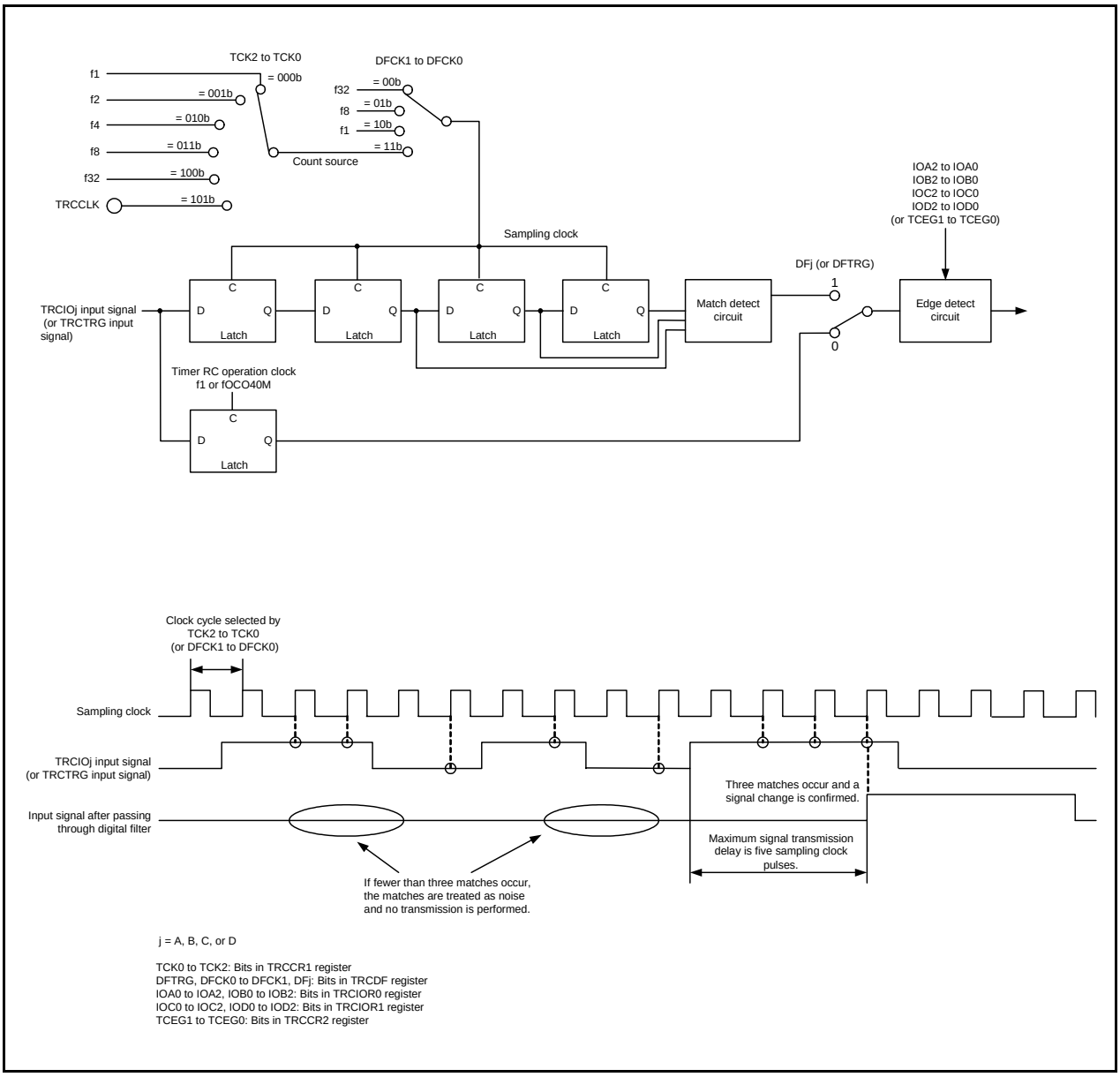


Figure 19.5 Digital Filter Block Diagram

19.3.4 Forced Cutoff of Pulse Output

When using the timer mode's output compare function, the PWM mode, or the PWM2 mode, pulse output from the TRCIOj (j = A, B, C, or D) output pin can be forcibly cut off and the TRCIOj pin set to function as a programmable I/O port by means of input to the $\overline{\text{INT0}}$ pin.
A pin used for output by the timer mode's output compare function, the PWM mode, or the PWM2 mode can be set to function as the timer RC output pin by setting the Ej bit in the TRCOER register to 0 (timer RC output enabled). If "L" is input to the $\overline{\text{INT0}}$ pin while the PTO bit in the TRCOER register is set to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled), bits EA, EB, EC, and ED in the TRCOER register are all set to 1 (timer RC output disabled, TRCIOj output pin functions as the programmable I/O port). When one or two cycles of the timer RC operation clock after "L" input to the $\overline{\text{INT0}}$ pin (refer to **Table 19.1 Timer RC Operation Clock**) have elapsed, the TRCIOj output pin becomes a programmable I/O port.

Make the following settings to use this function:
- Set the pin state following forced cutoff of pulse output (high impedance (input), "L" output, or "H" output) (refer to **7. I/O Ports**).
- Set the INT0EN bit in the INTEN register to 1 ($\overline{\text{INT0}}$ input enabled) and the INT0PL bit to 0 (one edge), and set the POL bit in the INT0IC register to 0 (falling edge selected).
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter by bits INT0F1 to INT0F0 in the INTF register.
- Set the PTO bit in the TRCOER register to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled).

The IR bit in the INT0IC register is set to 1 (interrupt requested) in accordance with the setting of the POL bit in the INT0IC register and the INT0PL bit in the INTEN register, and a change in the $\overline{\text{INT0}}$ pin input (refer to **11.9 Notes on Interrupts**).
For details on interrupts, refer to **11. Interrupts**.

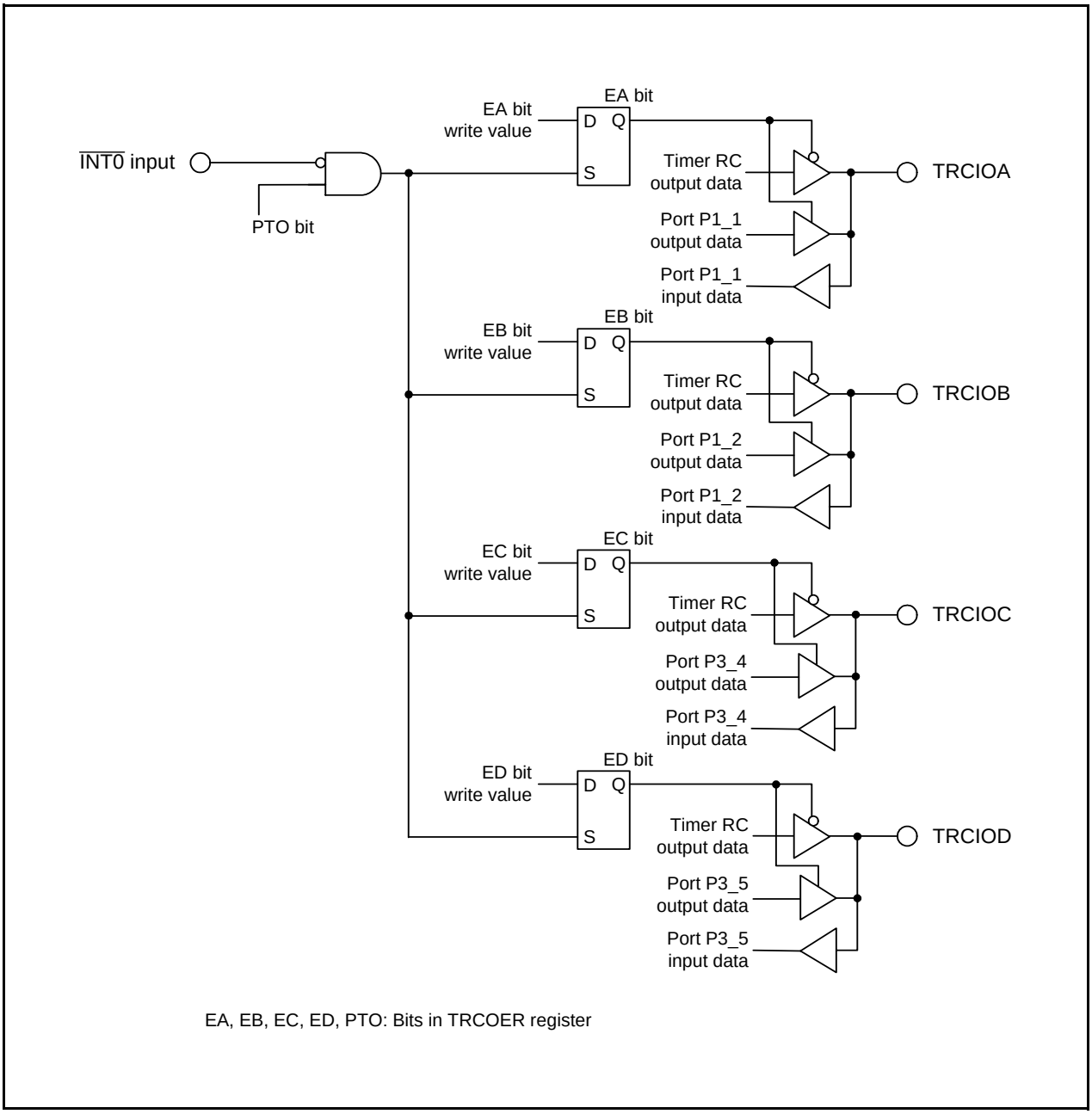


Figure 19.6 Forced Cutoff of Pulse Output

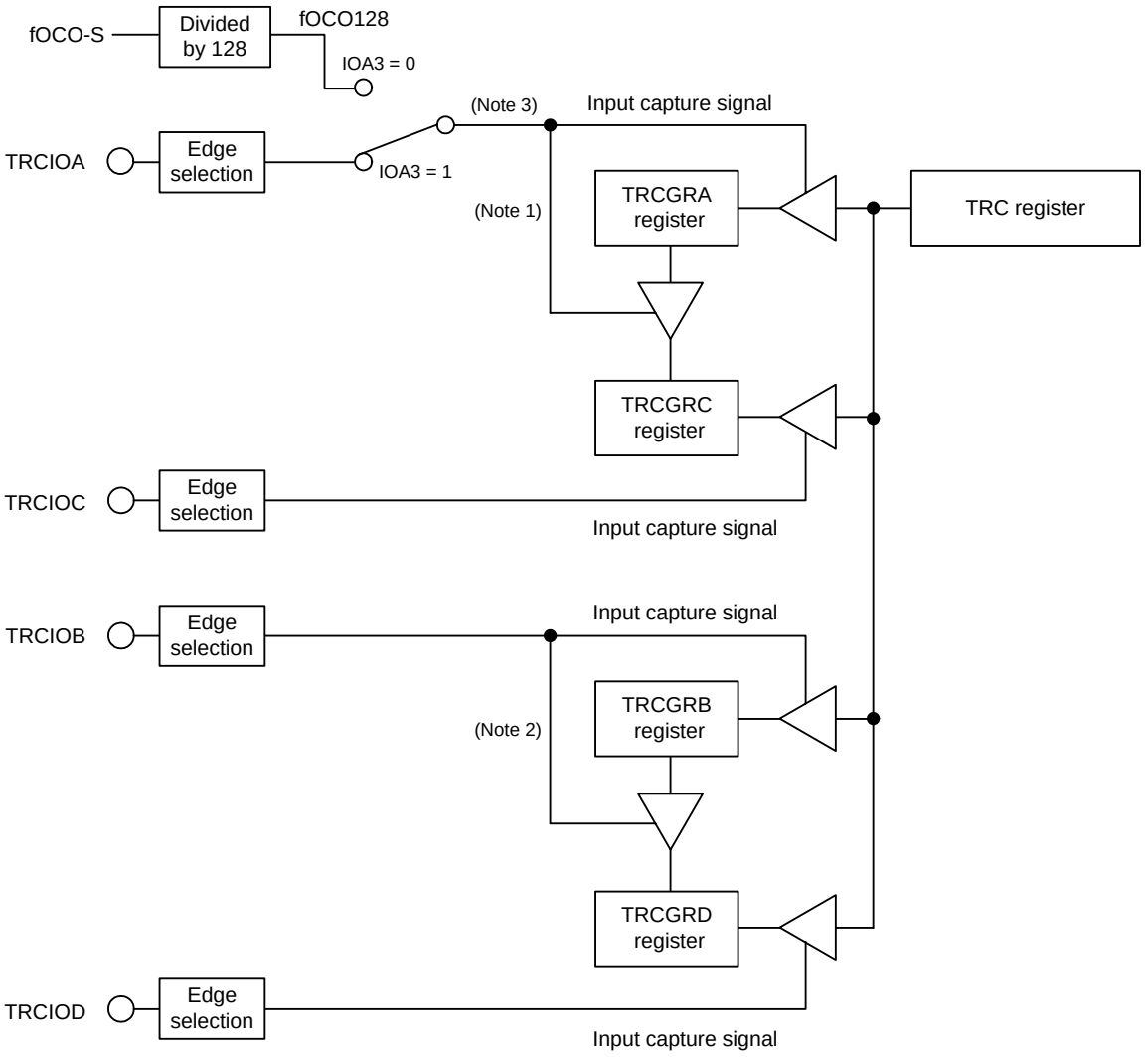
19.4 Timer Mode (Input Capture Function)

This function measures the width or period of an external signal. An external signal input to the TRCIOj (j = A, B, C, or D) pin acts as a trigger for transferring the contents of the TRC register (counter) to the TRCGRj register (input capture). The input capture function, or any other mode or function, can be selected for each individual pin. The TRCGRA register can also select fOCO128 signal as input-capture trigger input.
Table 19.7 lists the Input Capture Function Specifications, Figure 19.7 shows a Block Diagram of Input Capture Function, Table 19.8 lists the Functions of TRCGRj Register when Using Input Capture Function, and Figure 19.8 shows an Operating Example of Input Capture Function.

Table 19.7 Input Capture Function Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32 External signal input to TRCCLK pin (rising edge)
Count operation	Increment
Count period	• The CCLR bit in the TRCCR1 register is set to 0 (free running operation): 1/fk × 65,536 fk: Count source frequency • The CCLR bit in the TRCCR1 register is set to 1 (TRC register set to 0000h at TRCGRA input capture): 1/fk × (n+1) n: TRCGRA register setting value
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRCMR register. The TRC register retains a value before count stops.
Interrupt request generation timing	• Input capture (valid edge of TRCIOj input or fOCO128 signal edge) • The TRC register overflows.
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or input capture input (selectable individually for each pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• Input capture input pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Input capture input valid edge selection Rising edge, falling edge, or both rising and falling edges • Buffer operation (refer to **19.3.2 Buffer Operation**) • Digital filter (refer to **19.3.3 Digital Filter**) • Timing for setting the TRC register to 0000h Overflow or input capture • Input-capture trigger selected fOCO128 can be selected for input-capture trigger input of the TRCGRA register.

j = A, B, C, or D



IOA3: Bit in TRCIOR0 register

Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register for the TRCGRA register)
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register functions as the buffer register for the TRCGRB register)
3. The trigger input of the TRCGRA register can select the TRCIOA pin input or fOCO128 signal.

Figure 19.7 Block Diagram of Input Capture Function

19.4.1 Timer RC I/O Control Register 0 (TRCIOR0) for Input Capture Function

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Input capture to the TRCGRA register at the rising edge 0 1: Input capture to the TRCGRA register at the falling edge 1 0: Input capture to the TRCGRA register at both edges 1 1: Do not set.	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 1 (input capture) in the input capture function.	R/W
b3	IOA3	TRCGRA input capture input switch bit (3)	0: fOCO128 signal 1: TRCIOA pin input	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Input capture to the TRCGRB register at the rising edge 0 1: Input capture to the TRCGRB register at the falling edge 1 0: Input capture to the TRCGRB register at both edges 1 1: Do not set.	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 1 (input capture) in the input capture function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.
3. The IOA3 bit is enabled when the IOA2 bit is set to 1 (input capture function).

19.4.2 Timer RC I/O Control Register 1 (TRCIOR1) for Input Capture Function

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Input capture to the TRCGRC register at the rising edge 0 1: Input capture to the TRCGRC register at the falling edge 1 0: Input capture to the TRCGRC register at both edges 1 1: Do not set.	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 1 (input capture) in the input capture function.	R/W
b3	IOC3	TRCGRC register function select bit	Set to 1.	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Input capture to the TRCGRD register at the rising edge 0 1: Input capture to the TRCGRD register at the falling edge 1 0: Input capture to the TRCGRD register at both edges 1 1: Do not set.	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 1 (input capture) in the input capture function.	R/W
b7	IOD3	TRCGRD register function select bit	Set to 1.	R/W

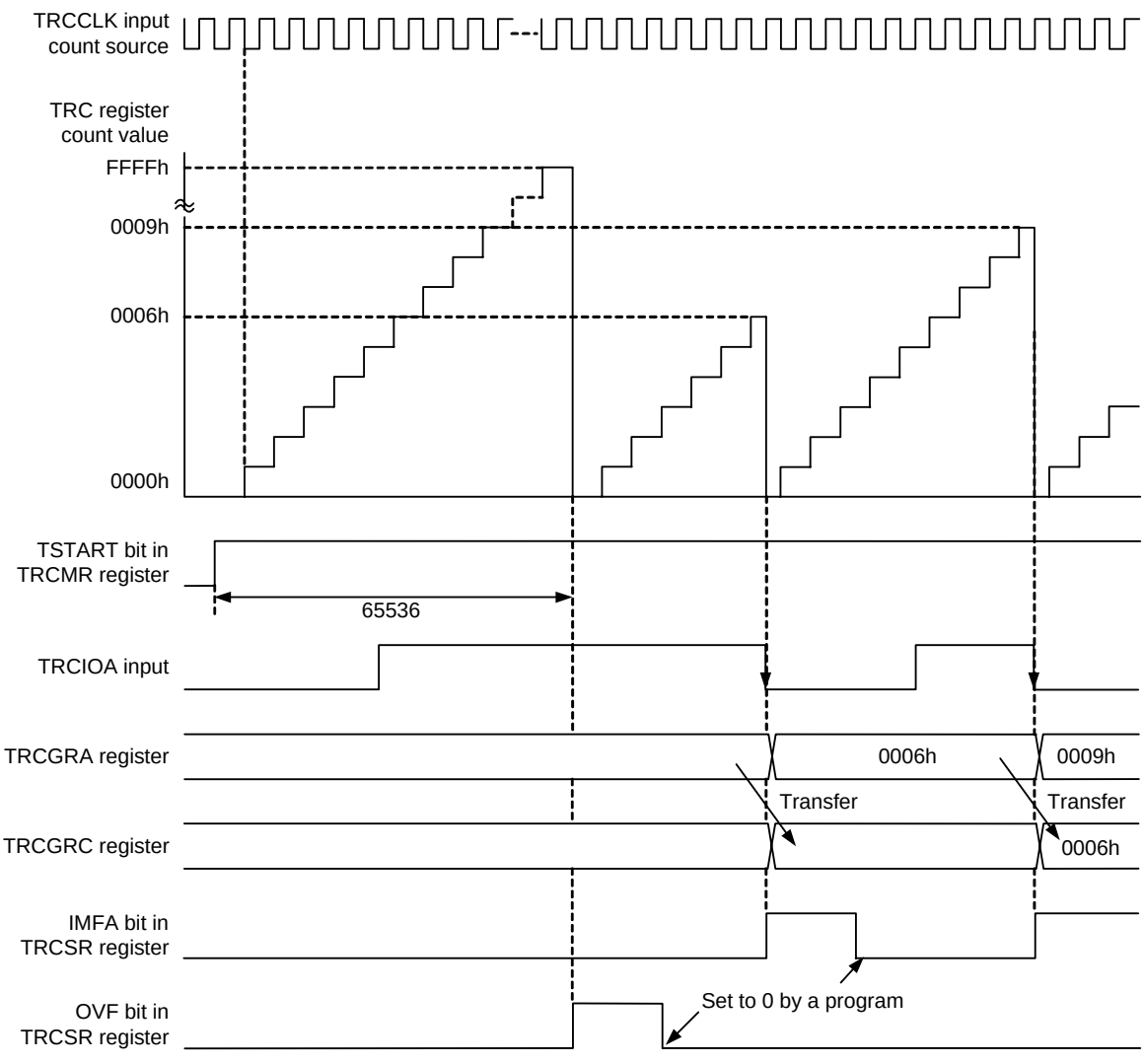
Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

Table 19.8 Functions of TRCGRj Register when Using Input Capture Function

Register	Setting	Register Function	Input Capture Input Pin
TRCGRA	—	General register. Can be used to read the TRC register value at input capture.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Can be used to read the TRC register value at input capture.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer registers. Can be used to hold transferred value from the general register (refer to **19.3.2 Buffer Operation**).	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

19.4.3 Operating Example



The above applies under the following conditions:
- The CCLR bit in the TRCCR1 register is set to 1 (Clear TRC counter by input capture).
- Bits TCK2 to TCK0 in the TRCCR1 register are set to 101b (the count source is TRCCLK input).
- Bits IOA2 to IOA0 in the TRCIORA register are set to 101b (input capture at the falling edge of the TRCIOA input).
- The BFC bit in the TRCMR register is set to 1 (the TRCGRC register functions as the buffer register for the TRCGRA register).

Figure 19.8 Operating Example of Input Capture Function

19.5 Timer Mode (Output Compare Function)

This function detects when the contents of the TRC register (counter) and the TRCGRj register (j = A, B, C, or D) match (compare match). When a match occurs a signal is output from the TRCIOj pin at a given level. The output compare function, or other mode or function, can be selected for each individual pin.
Table 19.9 lists the Output Compare Function Specifications, Figure 19.9 shows a Block Diagram of Output Compare Function, Table 19.10 lists the Functions of TRCGRj Register when Using Output Compare Function, and Figure 19.10 shows an Operating Example of Output Compare Function.

Table 19.9 Output Compare Function Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32 External signal input to TRCCLK pin (rising edge)
Count operation	Increment
Count period	• The CCLR bit in the TRCCR1 register is set to 0 (free running operation): 1/fk × 65,536 fk: Count source frequency • The CCLR bit in the TRCCR1 register is set to 1 (TRC register set to 0000h at TRCGRA compare match): 1/fk × (n+1) n: TRCGRA register setting value
Waveform output timing	Compare match
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with TRCGRA). 0 (count stops) is written to the TSTART bit in the TRCMR register. The output compare output pin retains output level before count stops, the TRC register retains a value before count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with TRCGRA register). The count stops at the compare match with the TRCGRA register. The output compare output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (contents of registers TRC and TRCGRj match) • The TRC register overflows.
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or output compare output (selectable individually for each pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• Output compare output pin selection One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD • Compare match output level selection “L” output, “H” output, or toggle output • Initial output level selection Sets output level for period from count start to compare match • Timing for setting the TRC register to 0000h Overflow or compare match with the TRCGRA register • Buffer operation (refer to **19.3.2 Buffer Operation**) • Pulse output forced cutoff signal input (refer to **19.3.4 Forced Cutoff of Pulse Output**) • Can be used as an internal timer by disabling timer RC output • Changing output pins for registers TRCGRC and TRCGRD TRCGRC can be used for output control of the TRCIOA pin and TRCGRD can be used for output control of the TRCIOB pin.

j = A, B, C, or D

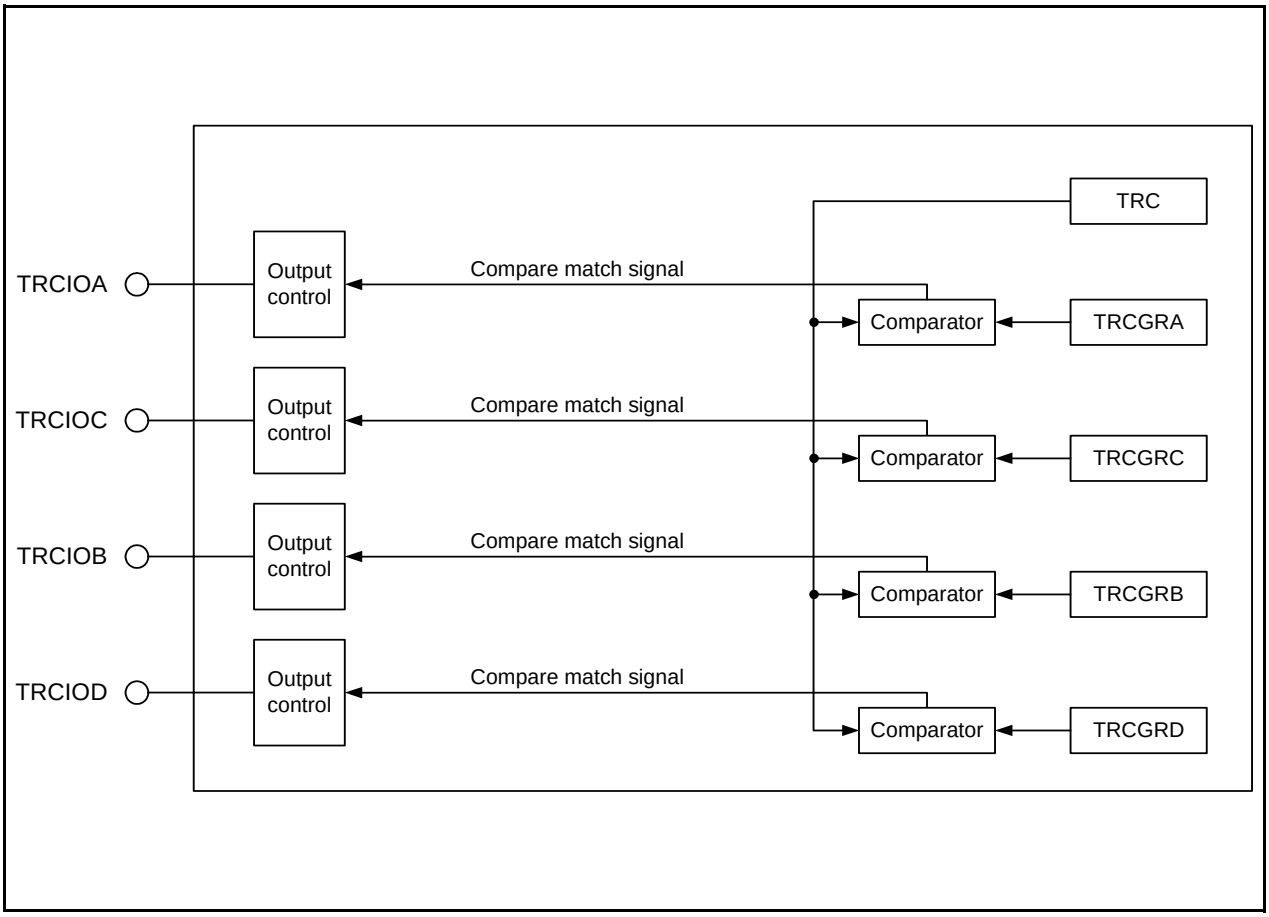


Figure 19.9 Block Diagram of Output Compare Function

19.5.1 Timer RC Control Register 1 (TRCCR1) for Output Compare Function

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1, 2)	0: Initial output “L” 1: Initial output “H”	R/W
b1	TOB	TRCIOB output level select bit (1, 2)		R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.

Table 19.10 Functions of TRCGRj Register when Using Output Compare Function

Register	Setting	Register Function	Output Compare Output Pin
TRCGRA	—	General register. Write a compare value to one of these registers.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Write a compare value to one of these registers.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Write the next compare value to one of these registers (refer to **19.3.2 Buffer Operation**).	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D
BFC, BFD: Bits in TRCMR register

19.5.2 Timer RC I/O Control Register 0 (TRCIOR0) for Output Compare Function

Address 0124h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	IOB2	IOB1	IOB0	IOA3	IOA2	IOA1	IOA0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOA0	TRCGRA control bit	b1 b0 0 0: Disable pin output by compare match (TRCIOA pin functions as the programmable I/O port) 0 1: “L” output by compare match in the TRCGRA register 1 0: “H” output by compare match in the TRCGRA register 1 1: Toggle output by compare match in the TRCGRA register	R/W
b1	IOA1			R/W
b2	IOA2	TRCGRA mode select bit (1)	Set to 0 (output compare) in the output compare function.	R/W
b3	IOA3	TRCGRA input capture input switch bit	Set to 1.	R/W
b4	IOB0	TRCGRB control bit	b5 b4 0 0: Disable pin output by compare match (TRCIOB pin functions as the programmable I/O port) 0 1: “L” output by compare match in the TRCGRB register 1 0: “H” output by compare match in the TRCGRB register 1 1: Toggle output by compare match in the TRCGRB register	R/W
b5	IOB1			R/W
b6	IOB2	TRCGRB mode select bit (2)	Set to 0 (output compare) in the output compare function.	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

19.5.3 Timer RC I/O Control Register 1 (TRCIOR1) for Output Compare Function

Address 0125h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	IOD3	IOD2	IOD1	IOD0	IOC3	IOC2	IOC1	IOC0
After Reset	1	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IOC0	TRCGRC control bit	b1 b0 0 0: Disable pin output by compare match 0 1: “L” output by compare match in the TRCGRC register 1 0: “H” output by compare match in the TRCGRC register 1 1: Toggle output by compare match in the TRCGRC register	R/W
b1	IOC1			R/W
b2	IOC2	TRCGRC mode select bit (1)	Set to 0 (output compare) in the output compare function.	R/W
b3	IOC3	TRCGRC register function select bit	0: TRCIOA output register 1: General register or buffer register	R/W
b4	IOD0	TRCGRD control bit	b5 b4 0 0: Disable pin output by compare match 0 1: “L” output by compare match in the TRCGRD register 1 0: “H” output by compare match in the TRCGRD register 1 1: Toggle output by compare match in the TRCGRD register	R/W
b5	IOD1			R/W
b6	IOD2	TRCGRD mode select bit (2)	Set to 0 (output compare) in the output compare function.	R/W
b7	IOD3	TRCGRD register function select bit	0: TRCIOB output register 1: General register or buffer register	R/W

Notes:
1. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in theTRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
2. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in theTRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

19.5.4 Timer RC Control Register 2 (TRCCR2) for Output Compare Function

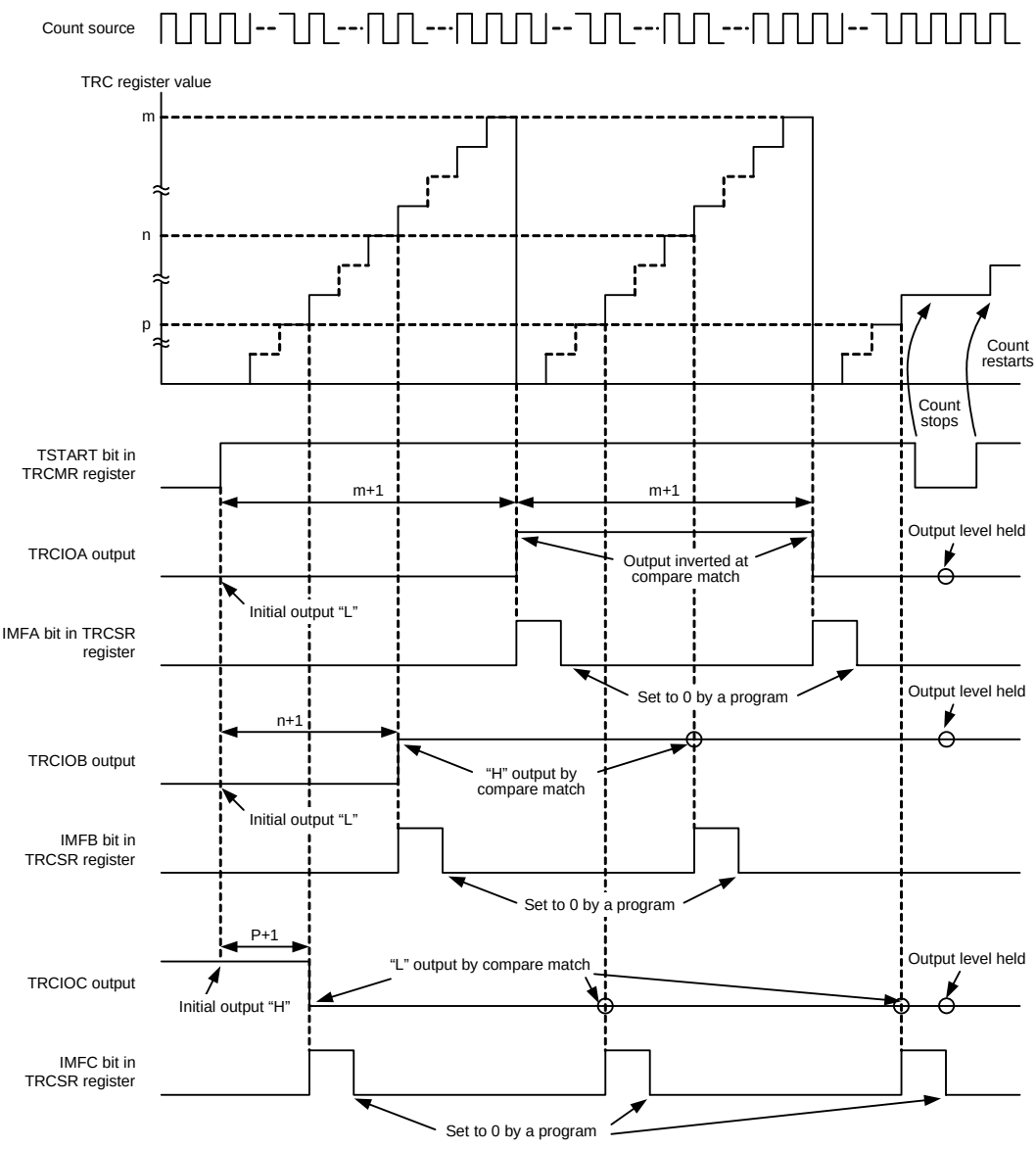
Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in the output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.5 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

19.5.5 Operating Example



The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (TRCGRC and TRCGRD do not operate as buffers).
- Bits EA, EB, and EC in the TRCOER register are set to 0 (output from TRCIOA, TRCIOB, and TRCIOC enabled).
- The CCLR bit in the TRCCR1 register is set to 1 (set the TRC register to 0000h by TRCGRA compare match).
- In the TRCCR1 register, bits TOA and TOB are set to 0 ("L" initial output until compare match) and the TOC bit is set to 1 ("H" initial output until compare match).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted at TRCGRA compare match).
- Bits IOB2 to IOB0 in the TRCIOR0 register are set to 010b ("H" TRCIOB output at TRCGRB compare match).
- Bits IOC2 to IOC2 in the TRCIOR1 register are set to 001b ("L" TRCIOC output at TRCGRC compare match).
- The CSEL bit in the TRCCR2 register is set to 0 (TRC count continues after TRCGRA compare match).

Figure 19.10 Operating Example of Output Compare Function

19.5.6 Changing Output Pins in Registers TRCGRC and TRCGRD

The TRCGRC register can be used for output control of the TRCIOA pin, and the TRCGRD register can be used for output control of the TRCIOB pin. Therefore, each pin output can be controlled as follows:

- TRCIOA output is controlled by the values in registers TRCGRA and TRCGRC.
- TRCIOB output is controlled by the values in registers TRCGRB and TRCGRD.

Change output pins in registers TRCGRC and TRCGRD as follows:

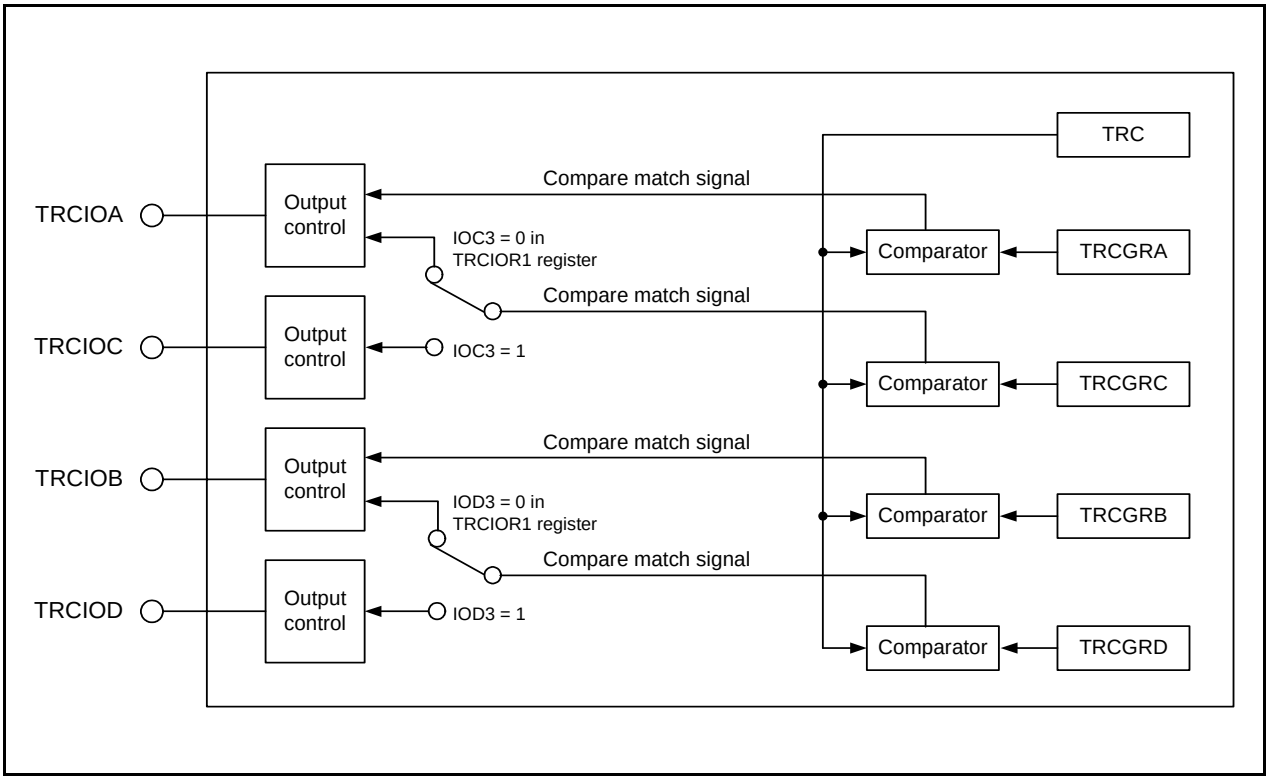
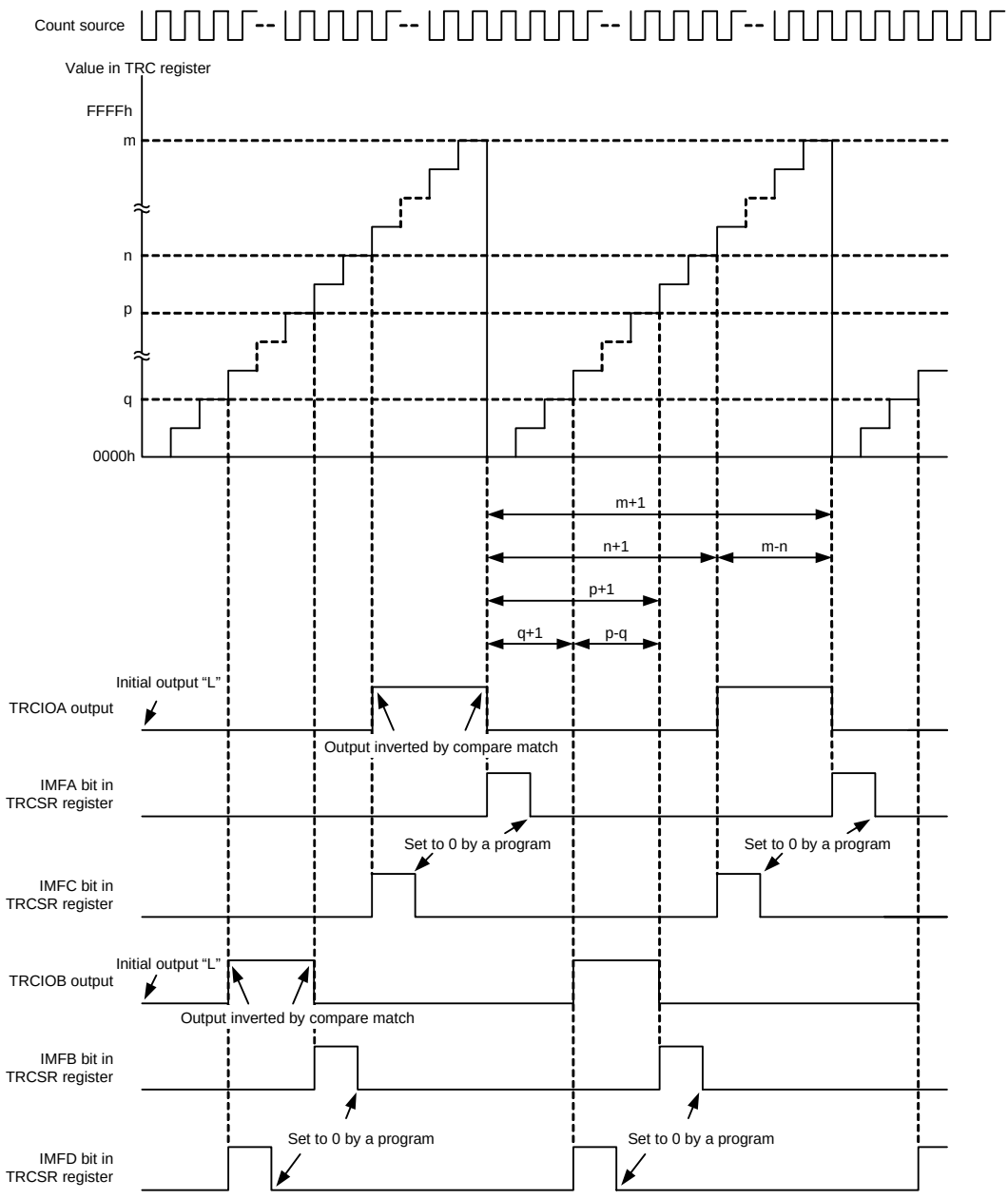


Figure 19.11 Changing Output Pins in Registers TRCGRC and TRCGRD

- Set the IOC3 bit in the TRCIOR1 register to 0 (TRCIOA output register) and set the IOD3 bit to 0 (TRCIOB output register).
- Set bits BFC and BFD in the TRCMR register to 0 (general register).
- Set different values in registers TRCGRC and TRCGRA. Also, set different values in registers TRCGRD and TRCGRB.

Figure 19.12 shows an Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin.



m: Value set in TRCGRA register
n: Value set in TRCGRC register
p: Value set in TRCGRB register
q: Value set in TRCGRD register

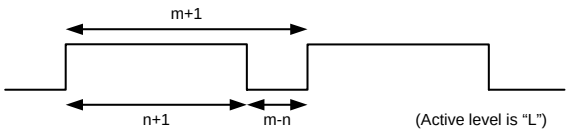
The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD are not used as buffer register).
- Bits EA and EB in the TRCOER register are set to 0 (enable TRCIOA and TRCIOB pin outputs).
- The CCLR bit in the TRCCR1 register are set to 1 (set the TRC register to 0000h by compare match in the TRCGRA register).
- Bits TOA and TOB in the TRCCR1 register are set to 0 (initial output "L" to compare match).
- Bits IOA2 to IOA0 in the TRCIOR0 register are set to 011b (TRCIOA output inverted at TRCGRA register compare match).
- Bits IOB2 to IOB0 in the TRCIOR0 register are set to 011b (TRCIOB output inverted at TRCGRB register compare match).
- Bits IOC2 to IOC0 in the TRCIOR1 register are set to 011b (TRCIOA output inverted at TRCGRC register compare match).
- The IOC3 bit in the TRCIOR1 register are set to 0 (TRCIOA output register).
- Bits IOD2 to IOD0 in the TRCIOR1 register are set to 011b (TRCIOB output inverted at TRCGRD register compare match).
- The IOD3 bit in the TRCIOR1 register are set to 0 (TRCIOB output register).
- The CSEL bit in the TRCCR2 register are set to 0 (TRC continues counting after compare match).

Figure 19.12 Operating Example When TRCGRC Register is Used for Output Control of TRCIOA Pin and TRCGRD Register is Used for Output Control of TRCIOB Pin

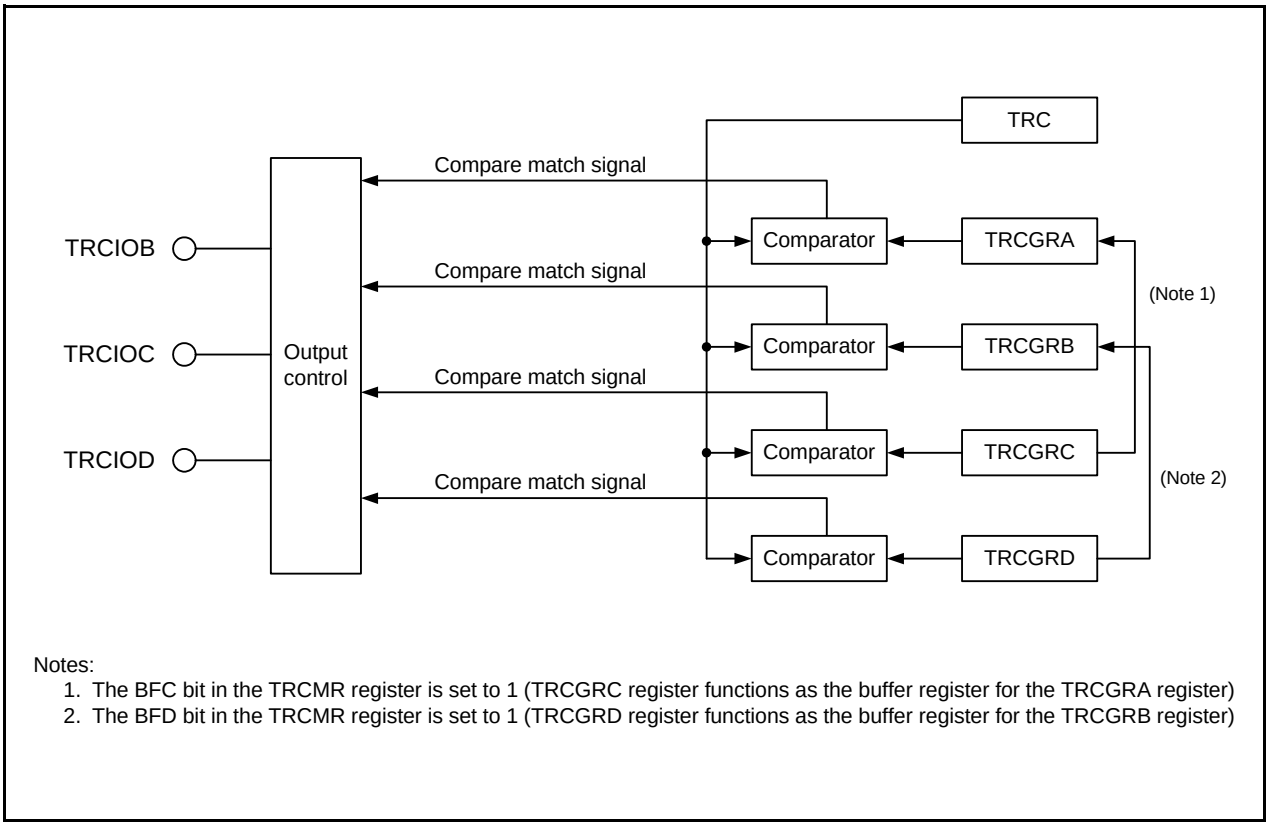
19.6 PWM Mode

This mode outputs PWM waveforms. A maximum of three PWM waveforms with the same period are output. The PWM mode, or the timer mode, can be selected for each individual pin. (However, since the TRCGRA register is used when using any pin for the PWM mode, the TRCGRA register cannot be used for the timer mode.)
Table 19.11 lists the PWM Mode Specifications, Figure 19.13 shows a PWM Mode Block Diagram, Table 19.12 lists the Functions of TRCGRh Register in PWM Mode, and Figures 19.14 and 19.15 show Operating Examples of PWM Mode.

Table 19.11 PWM Mode Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32 External signal input to TRCCLK pin (rising edge)
Count operation	Increment
PWM waveform	PWM period: 1/fk × (m+1) Active level width: 1/fk × (m-n) inactive level width: 1/fk × (n+1) fk: Count source frequency m: TRCGRA register setting value n: TRCGRj register setting value 
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	• When the CSEL bit in the TRCCR2 register is set to 0 (count continues after compare match with TRCGRA). 0 (count stops) is written to the TSTART bit in the TRCMR register. PWM output pin retains output level before count stops, TRC register retains value before count stops. • When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with TRCGRA register). The count stops at the compare match with the TRCGRA register. The PWM output pin retains the level after the output is changed by the compare match.
Interrupt request generation timing	• Compare match (contents of registers TRC and TRCGRh match) • The TRC register overflows.
TRCIOA pin function	Programmable I/O port
TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or PWM output (selectable individually for each pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• One to three pins selectable as PWM output pins One or more of pins TRCIOB, TRCIOC, and TRCIOD • Active level selectable for each pin • Initial level selectable for each pin • Buffer operation (refer to **19.3.2 Buffer Operation**) • Pulse output forced cutoff signal input (refer to **19.3.4 Forced Cutoff of Pulse Output**)

j = B, C, or D
h = A, B, C, or D



Notes:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register for the TRCGRA register)
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register functions as the buffer register for the TRCGRB register)

Figure 19.13 PWM Mode Block Diagram

19.6.1 Timer RC Control Register 1 (TRCCR1) in PWM Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM mode	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Initial output selected as non-active level 1: Initial output selected as active level	R/W
b2	TOC	TRCIOC output level select bit (1, 2)		R/W
b3	TOD	TRCIOD output level select bit (1, 2)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.

19.6.2 Timer RC Control Register 2 (TRCCR2) in PWM Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

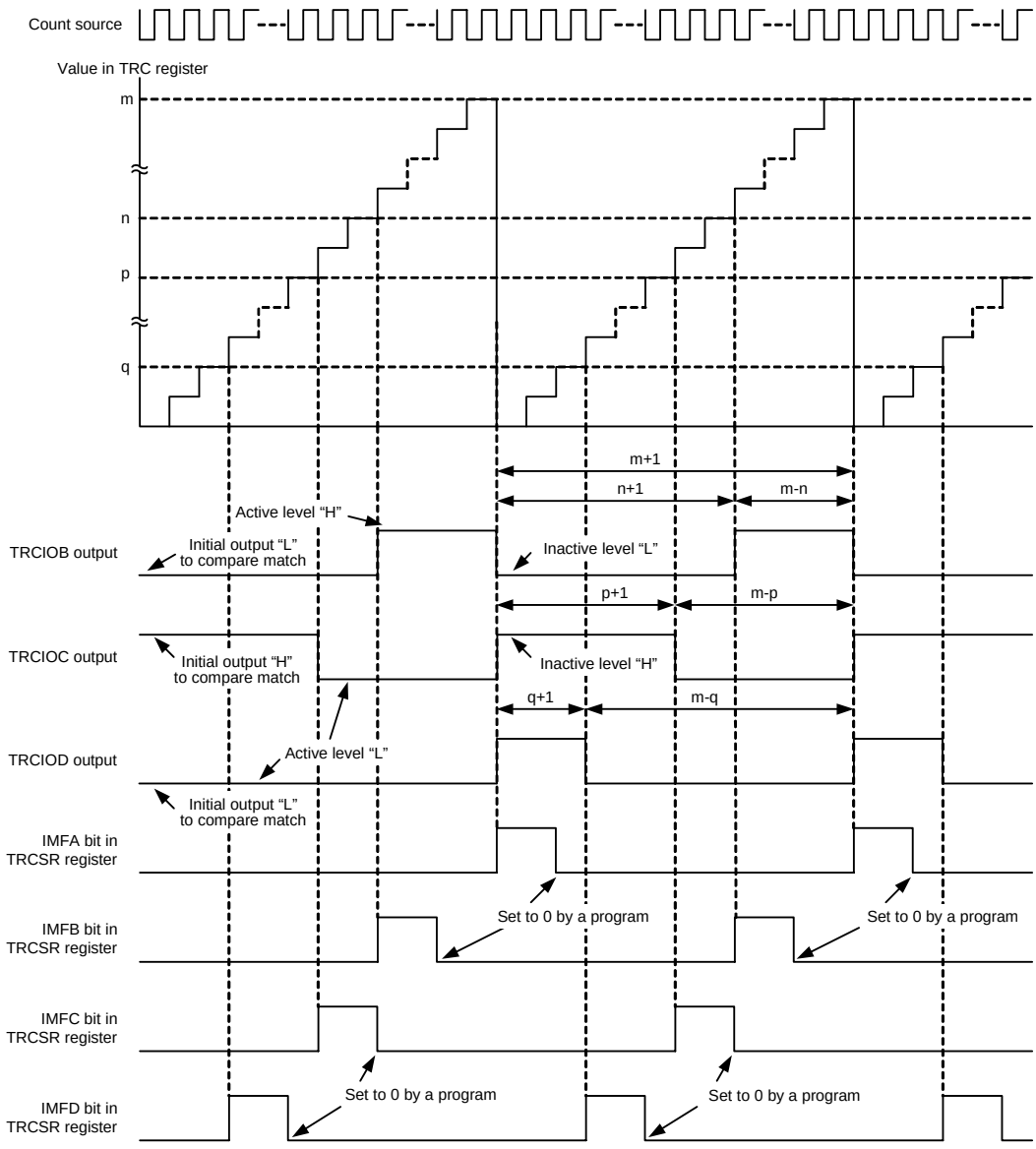
Notes:
1. Enabled when in PWM mode.
2. Enabled when in the output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.5 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

Table 19.12 Functions of TRCGRh Register in PWM Mode

Register	Setting	Register Function	PWM Output Pin
TRCGRA	—	General register. Set the PWM period.	—
TRCGRB	—	General register. Set the PWM output change point.	TRCIOB
TRCGRC	BFC = 0	General register. Set the PWM output change point.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Set the next PWM period (refer to **19.3.2 Buffer Operation**).	—
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point (refer to **19.3.2 Buffer Operation**).	TRCIOB

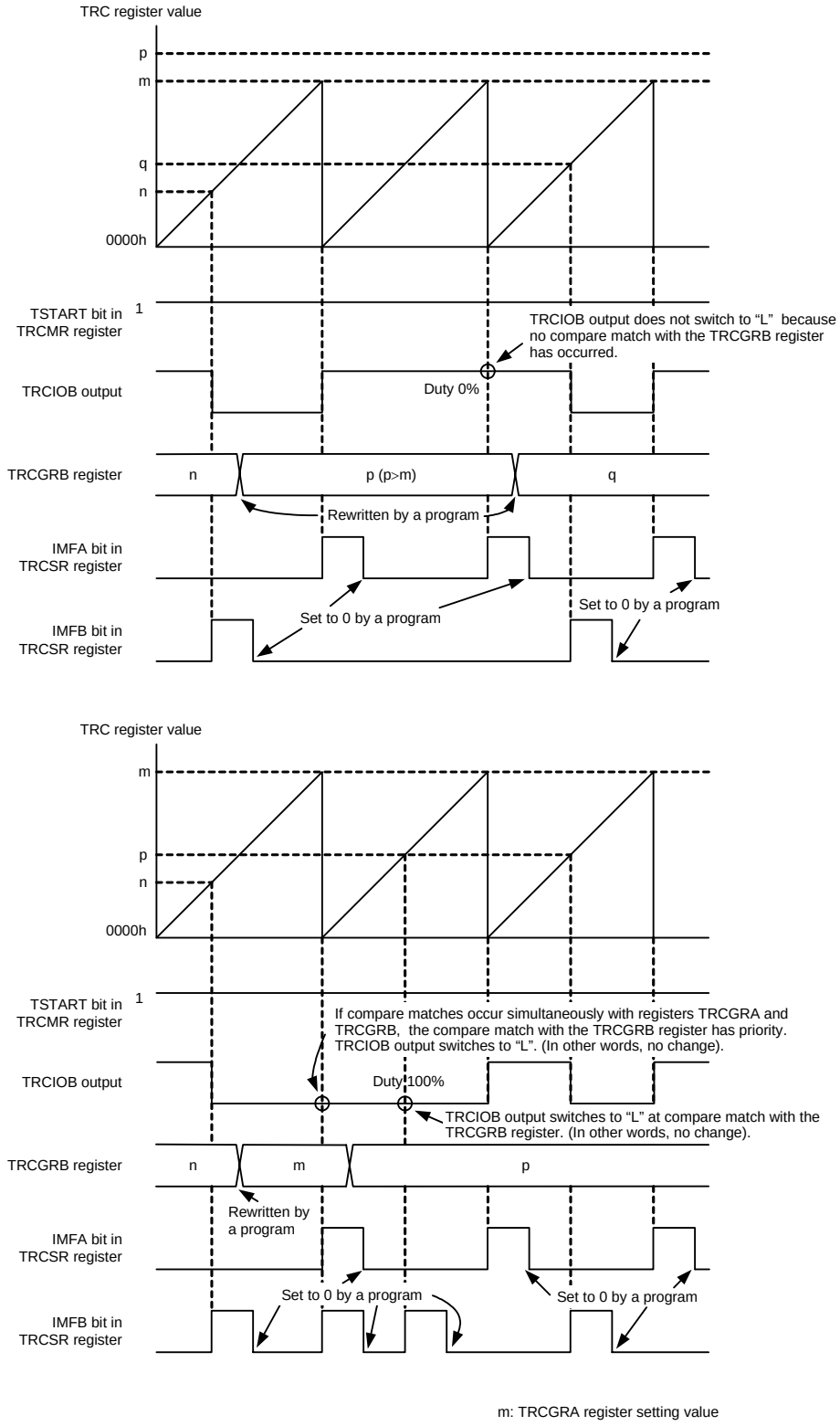
h = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. The output level does not change even when a compare match occurs if the TRCGRA register value (PWM period) is the same as the TRCGRB, TRCGRC, or TRCGRD register value.

19.6.3 Operating Example



The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD do not operate as buffers).
- Bits EB, EC, and ED in the TRCOER register are set to 0 (output from TRCIOB, TRCIOC, and TRCIOD enabled).
- Bits TOB and TOC in the TRCCR1 register are set to 0 (inactive level), the TOD bit is set to 1 (active level).
- The POLB bit in the TRCCR2 register is set to 1 ("H" active), bits POLC and POLD are set to 0 ("L" active).

Figure 19.14 Operating Example of PWM Mode

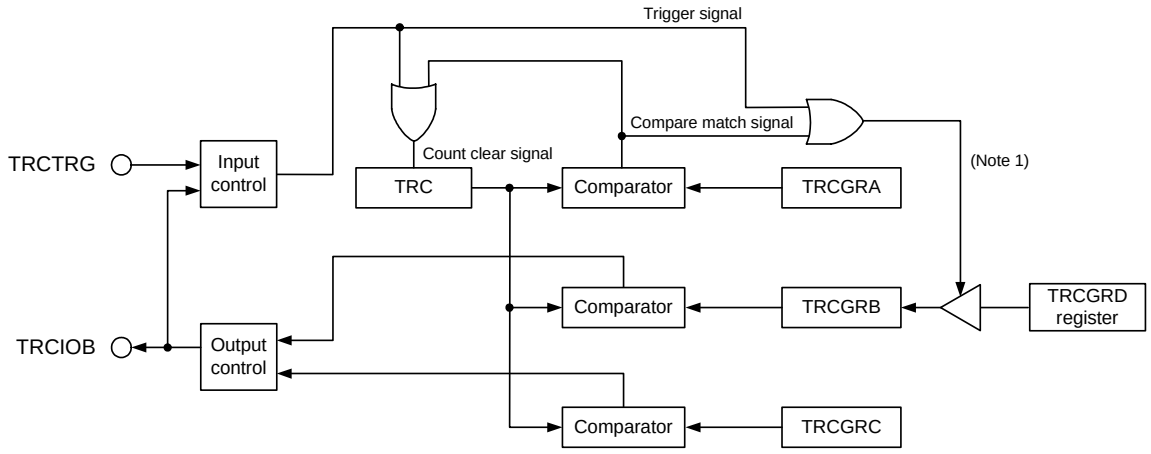


The above applies under the following conditions:
- The EB bit in the TRCOER register is set to 0 (output from TRCIOB enabled).
- The POLB bit in the TRCCR2 register is set to 0 ("L" active).

Figure 19.15 Operating Example of PWM Mode (Duty 0% and Duty 100%)

19.7 PWM2 Mode

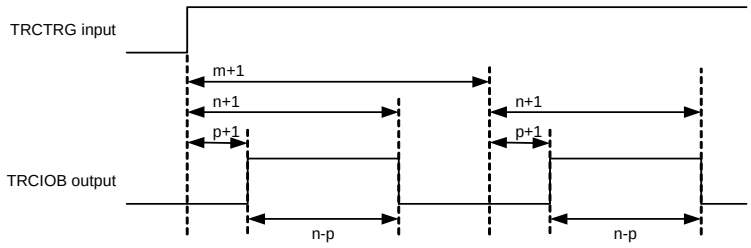
This mode outputs a single PWM waveform. After a given wait duration has elapsed following the trigger, the pin output switches to active level. Then, after a given duration, the output switches back to inactive level. Furthermore, the counter stops at the same time the output returns to inactive level, making it possible to use PWM2 mode to output a programmable wait one-shot waveform.
Since timer RC uses multiple general registers in PWM2 mode, other modes cannot be used in conjunction with it. Figure 19.16 shows a PWM2 Mode Block Diagram, Table 19.13 lists the PWM2 Mode Specifications, Table 19.14 lists the Functions of TRCGRj Register in PWM2 Mode, and Figures 19.17 to 19.19 show Operating Examples of PWM2 Mode.



Note:
1. The BFD bit in the TRCMR register is set to 1 (the TRCGRD register functions as the buffer register for the TRCGRB register).

Figure 19.16 PWM2 Mode Block Diagram

Table 19.13 PWM2 Mode Specifications

Item	Specification
Count source	f1, f2, f4, f8, f32 External signal input to TRCCLK pin (rising edge)
Count operation	Increment TRC register
PWM waveform	PWM period: 1/fk × (m+1) (no TRCTRG input) Active level width: 1/fk × (n-p) Wait time from count start or trigger: 1/fk × (p+1) fk: Count source frequency m: TRCGRA register setting value n: TRCGRB register setting value p: TRCGRC register setting value  (TRCTRG: Rising edge, active level is “H”)
Count start conditions	• Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger disabled) or the CSEL bit in the TRCCR2 register is set to 0 (count continues). 1 (count starts) is written to the TSTART bit in the TRCMR register. • Bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger enabled) and the TSTART bit in the TRCMR register is set to 1 (count starts). A trigger is input to the TRCTRG pin
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRCMR register while the CSEL bit in the TRCCR2 register is set to 0 or 1. The TRCIOB pin outputs the initial level in accordance with the value of the TOB bit in the TRCCR1 register. The TRC register retains the value before count stops. • The count stops due to a compare match with TRCGRA while the CSEL bit in the TRCCR2 register is set to 1 The TRCIOB pin outputs the initial level. The TRC register retains the value before count stops if the CCLR bit in the TRCCR1 register is set to 0. The TRC register is set to 0000h if the CCLR bit in the TRCCR1 register is set to 1.
Interrupt request generation timing	• Compare match (contents of TRC and TRCGRj registers match) • The TRC register overflows
TRCIOA/TRCTRG pin function	Programmable I/O port or TRCTRG input
TRCIOB pin function	PWM output
TRCIOC and TRCIOD pin functions	Programmable I/O port
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Selectable functions	• External trigger and valid edge selection The edge or edges of the signal input to the TRCTRG pin can be used as the PWM output trigger: rising edge, falling edge, or both rising and falling edges • Buffer operation (refer to **19.3.2 Buffer Operation**) • Pulse output forced cutoff signal input (refer to **19.3.4 Forced Cutoff of Pulse Output**) • Digital filter (refer to **19.3.3 Digital Filter**)

j = A, B, or C

19.7.1 Timer RC Control Register 1 (TRCCR1) in PWM2 Mode

Address 0121h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCLR	TCK2	TCK1	TCK0	TOD	TOC	TOB	TOA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TOA	TRCIOA output level select bit (1)	Disabled in PWM2 mode	R/W
b1	TOB	TRCIOB output level select bit (1, 2)	0: Active level “H” (Initial output “L” “H” output by compare match in the TRCGRC register “L” output by compare match in the TRCGRB register) 1: Active level “L” (Initial output “H” “L” output by compare match in the TRCGRC register “H” output by compare match in the TRCGRB register)	R/W
b2	TOC	TRCIOC output level select bit (1)	Disabled in PWM2 mode	R/W
b3	TOD	TRCIOD output level select bit (1)		R/W
b4	TCK0	Count source select bit (1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: Do not set. 1 1 1: Do not set.	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	R/W

Notes:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. If the pin function is set for waveform output (refer to **7.5 Port Settings**), the initial output level is output when the TRCCR1 register is set.

19.7.2 Timer RC Control Register 2 (TRCCR2) in PWM2 Mode

Address 0130h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TCEG1	TCEG0	CSEL	—	—	POLD	POLC	POLB
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	POLB	PWM mode output level control bit B (1)	0: TRCIOB output level selected as “L” active 1: TRCIOB output level selected as “H” active	R/W
b1	POLC	PWM mode output level control bit C (1)	0: TRCIOC output level selected as “L” active 1: TRCIOC output level selected as “H” active	R/W
b2	POLD	PWM mode output level control bit D (1)	0: TRCIOD output level selected as “L” active 1: TRCIOD output level selected as “H” active	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b4	—			
b5	CSEL	TRC count operation select bit (2)	0: Count continues at compare match with the TRCGRA register 1: Count stops at compare match with the TRCGRA register	R/W
b6	TCEG0	TRCTRG input edge select bit (3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin 0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	R/W
b7	TCEG1			R/W

Notes:
1. Enabled when in PWM mode.
2. Enabled when in the output compare function, PWM mode, or PWM2 mode. For notes on PWM2 mode, refer to **19.9.5 TRCMR Register in PWM2 Mode**.
3. Enabled when in PWM2 mode.

19.7.3 Timer RC Digital Filter Function Select Register (TRCDF) in PWM2 Mode

Address 0131h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	DFCK1	DFCK0	—	DFTRG	DFD	DFC	DFB	DFA
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	DFA	TRCIOA pin digital filter function select bit (1)	0: Function is not used 1: Function is used	R/W
b1	DFB	TRCIOB pin digital filter function select bit (1)		R/W
b2	DFC	TRCIOC pin digital filter function select bit (1)		R/W
b3	DFD	TRCIOD pin digital filter function select bit (1)		R/W
b4	DFTRG	TRCTRG pin digital filter function select bit (2)		R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	DFCK0	Clock select bits for digital filter function (1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1 1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRCCR1 register)	R/W
b7	DFCK1			R/W

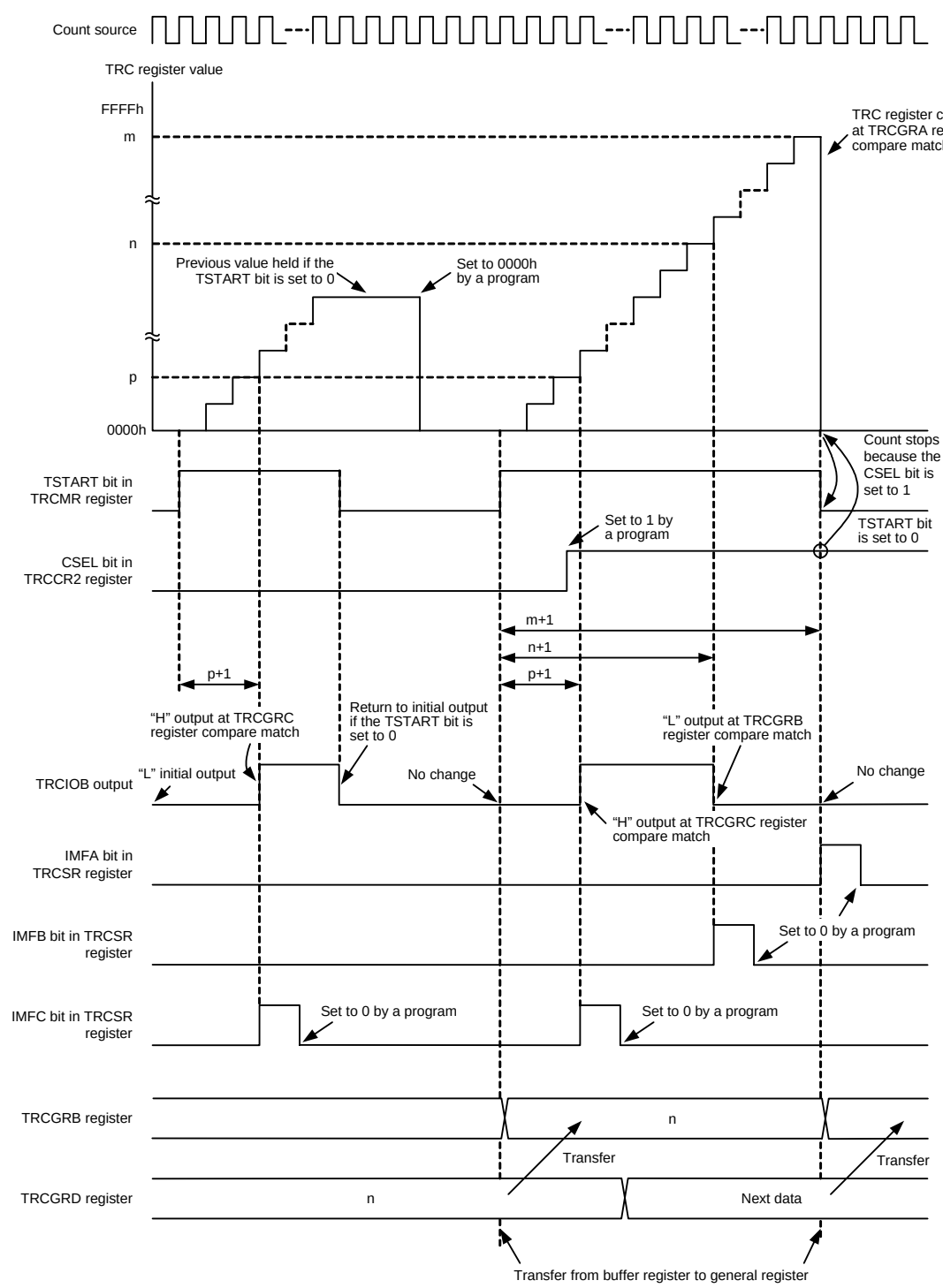
Notes:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

Table 19.14 Functions of TRCGRj Register in PWM2 Mode

Register	Setting	Register Function	PWM2 Output Pin
TRCGRA	—	General register. Set the PWM period.	TRCIOB pin
TRCGRB (1)	—	General register. Set the PWM output change point.	
TRCGRC (1)	BFC = 0	General register. Set the PWM output change point (wait time after trigger).	
TRCGRD	BFD = 0	(Not used in PWM2 mode)	—
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point (refer to **19.3.2 Buffer Operation**).	TRCIOB pin

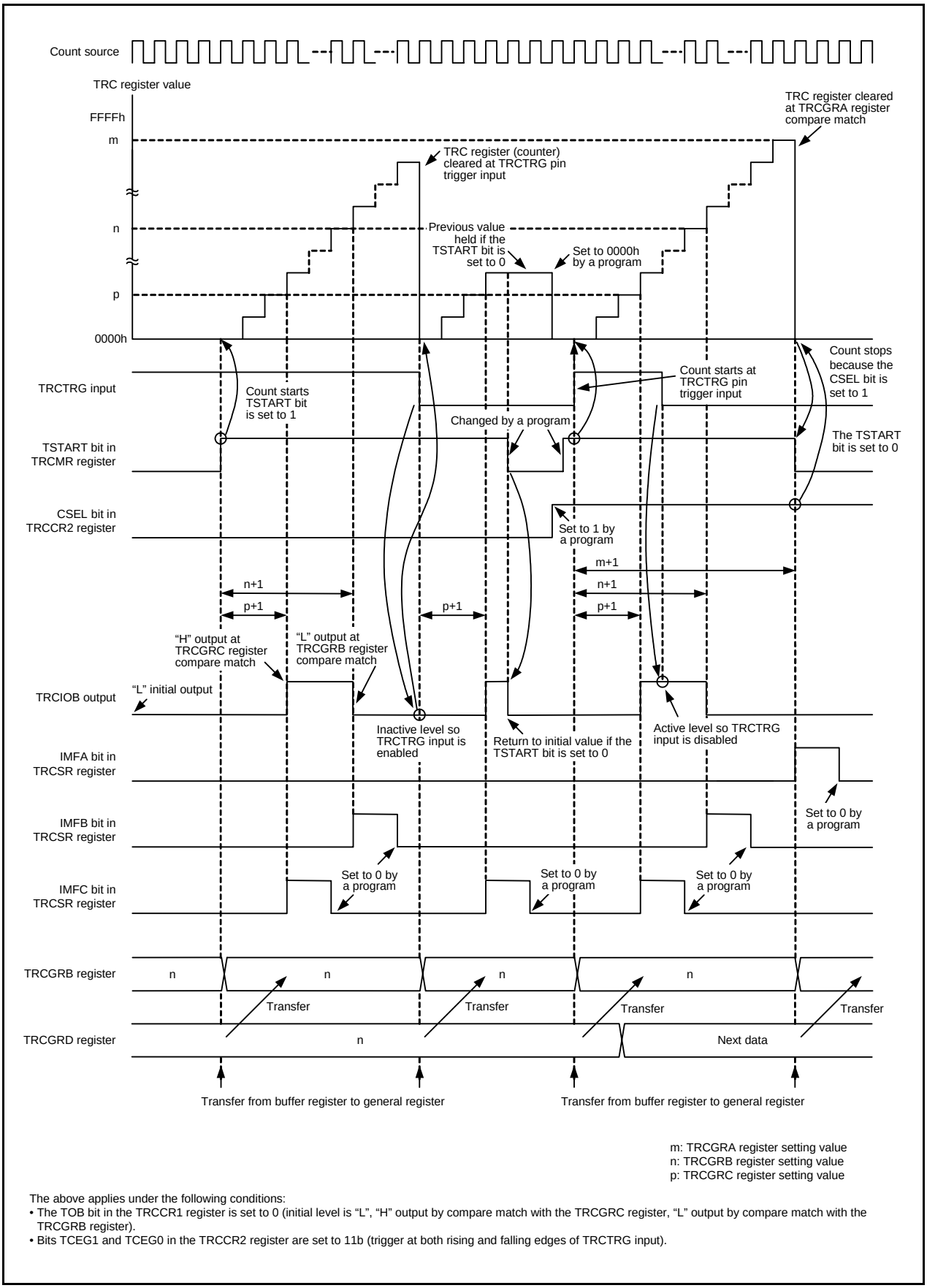
j = A, B, C, or D
BFC, BFD: Bits in TRCMR register
Note:
1. Do not set the TRCGRB and TRCGRC registers to the same value.

19.7.4 Operating Example



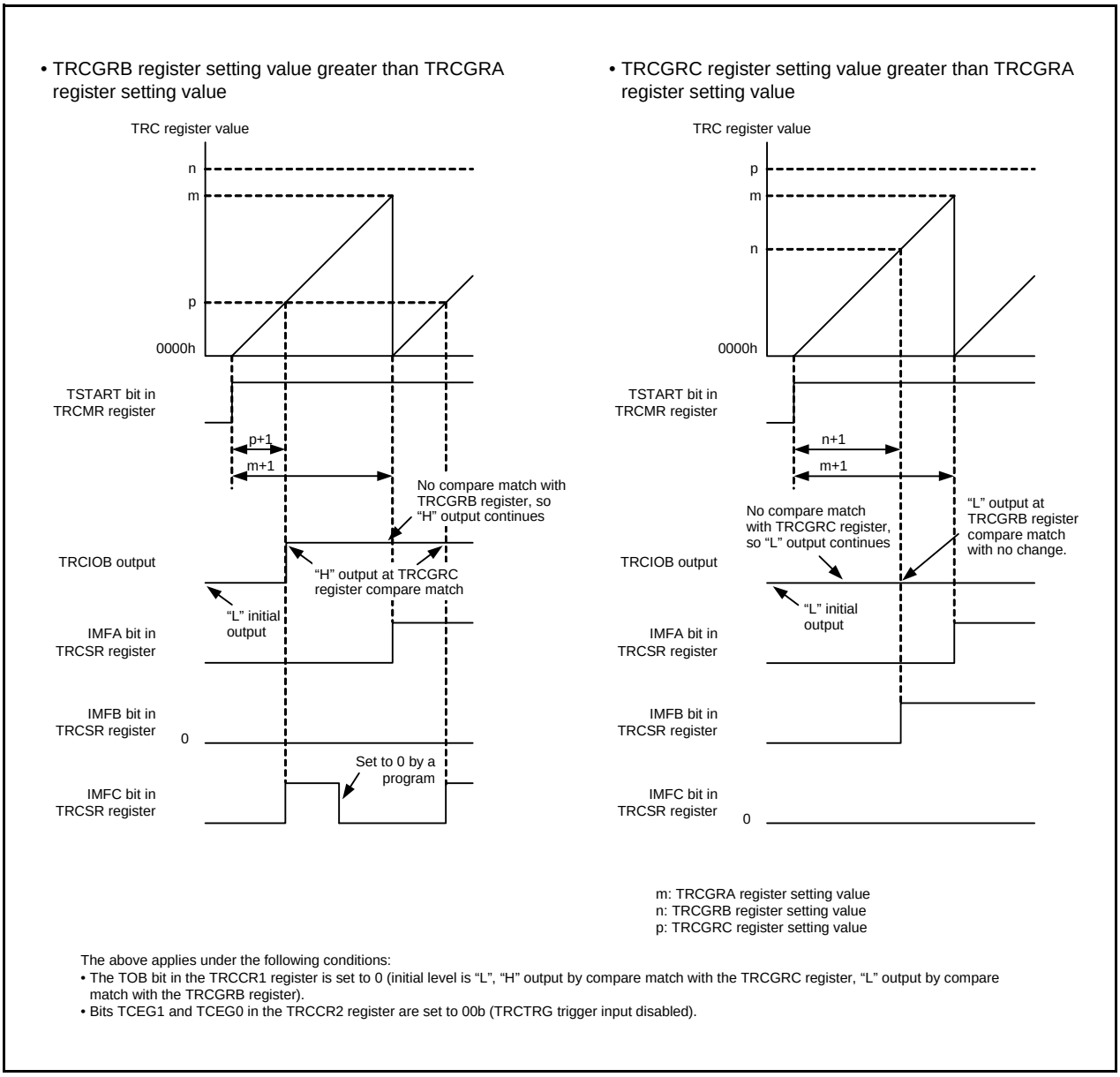
The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is "L", "H" output by compare match with the TRCGRC register, "L" output by compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger input disabled).

Figure 19.17 Operating Example of PWM2 Mode (TRCTRG Trigger Input Disabled)



The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is "L", "H" output by compare match with the TRCGRC register, "L" output by compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 11b (trigger at both rising and falling edges of TRCTRG input).

Figure 19.18 Operating Example of PWM2 Mode (TRCTRG Trigger Input Enabled)



The above applies under the following conditions:
- The TOB bit in the TRCCR1 register is set to 0 (initial level is "L", "H" output by compare match with the TRCGRC register, "L" output by compare match with the TRCGRB register).
- Bits TCEG1 and TCEG0 in the TRCCR2 register are set to 00b (TRCTRG trigger input disabled).

Figure 19.19 Operating Example of PWM2 Mode (Duty 0% and Duty 100%)

19.8 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses the single TRCIC register (bits IR and ILVL0 to ILVL2) and a single vector.
Table 19.15 lists the Registers Associated with Timer RC Interrupt and Figure 19.20 is a Timer RC Interrupt Block Diagram.

Table 19.15 Registers Associated with Timer RC Interrupt

Timer RC Status Register	Timer RC Interrupt Enable Register	Timer RC Interrupt Control Register
TRCSR	TRCIER	TRCIC

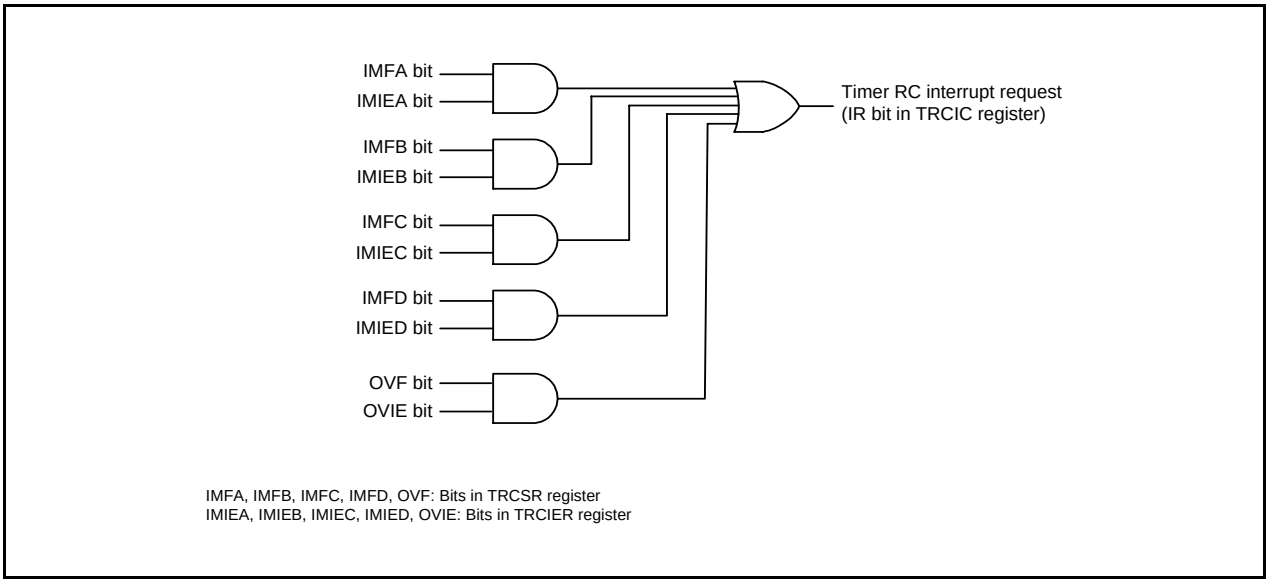


Figure 19.20 Timer RC Interrupt Block Diagram

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRCIC register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt requested) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IR bit is once set to 1 but the interrupt is not acknowledged.
- If another interrupt source is triggered after the IR bit is set to 1, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **19.2.5 Timer RC Status Register (TRCSR)**, for the procedure for setting these bits to 0.

Refer to **19.2.4 Timer RC Interrupt Enable Register (TRCIER)**, for details of the TRCIER register.
Refer to **11.3 Interrupt Control**, for details of the TRCIC register and **11.1.5.2 Relocatable Vector Tables**, for information on interrupt vectors.

19.9 Notes on Timer RC

19.9.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (clear TRC register at compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC    ; Write
                    JMP.B   L1             ; JMP.B instruction
                L1: MOV.W   TRC, DATA      ; Read
```

19.9.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR    ; Write
                    JMP.B   L1             ; JMP.B instruction
                L1: MOV.B   TRCSR, DATA    ; Read
```

19.9.3 Count Source Switching

- Stop the count before switching the count source.

Switching procedure

(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

19.9.4 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 19.1 Timer RC Operation Clock**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 19.5 Digital Filter Block Diagram**)
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).
- When the input capture function is used, if an edge selected by bits IOj0 and IOj1 (j = A, B, C, or D) in the TRCIOR0 or TRCIOR1 register is input to the TRCIOj pin, the IMFj bit in the TRCSR register is set to 1 even when the TSTART bit in the TRCMR register is 0 (count stops).

19.9.5 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

20. Timer RE

Timer RE has an 8-bit counter with a 4-bit prescaler.

20.1 Overview

Timer RE has the following 2 modes:

- Real-time clock mode — Generate 1-second signal from fC4 and count seconds, minutes, hours, and days of the week.
- Output compare mode — Count a count source and detect compare matches.

The count source for timer RE is the operating clock that regulates the timing of timer operations.
Table 20.1 lists the Pin Configuration of Timer RE.

Table 20.1 Pin Configuration of Timer RE

Pin Name	Assigned Pin	I/O	Function
TREO	P0_4	Output	Function differs according to the mode. Refer to descriptions of individual modes for details.

20.2 Real-Time Clock Mode

In real-time clock mode, a 1-second signal is generated from fC4 using a divide-by-2 frequency divider, 4-bit counter, and 8-bit counter and used to count seconds, minutes, hours, and days of the week. Figure 20.1 shows a Block Diagram of Real-Time Clock Mode and Table 20.2 lists the Real-Time Clock Mode Specifications. Table 20.3 lists the Interrupt Sources, Figure 20.2 shows the Definition of Time Representation, and Figure 20.3 shows the Operating Example in Real-Time Clock Mode.

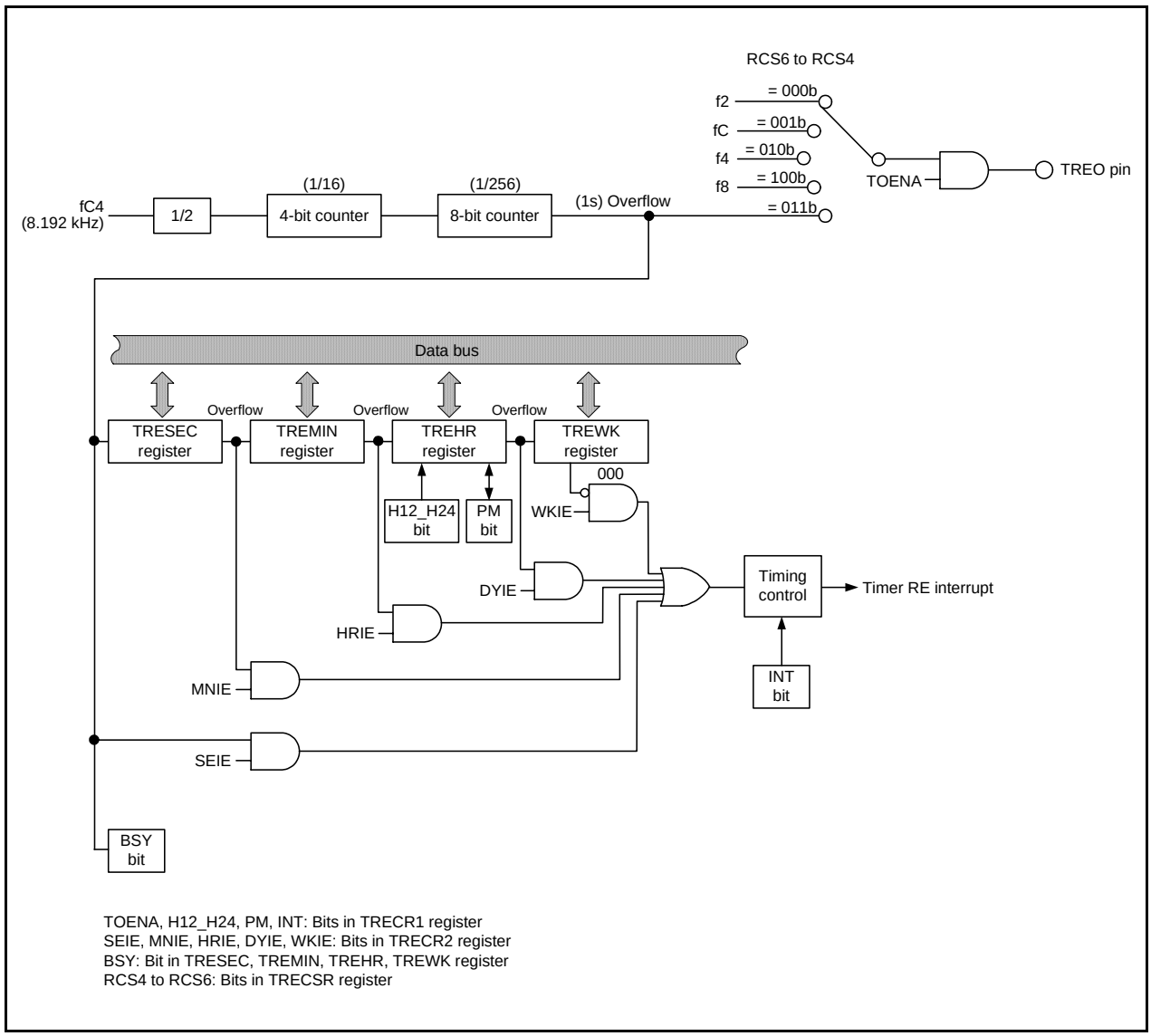


Figure 20.1 Block Diagram of Real-Time Clock Mode

Table 20.2 Real-Time Clock Mode Specifications

Item	Specification
Count source	fC4
Count operation	Increment
Count start condition	1 (count starts) is written to TSTART bit in TRECR1 register
Count stop condition	0 (count stops) is written to TSTART bit in TRECR1 register
Interrupt request generation timing	Select any one of the following: • Update second data • Update minute data • Update hour data • Update day of week data • When day of week data is set to 000b (Sunday)
TREO pin function	Programmable I/O ports or output of f2, fC, f4, f8 or, 1Hz
Read from timer	When reading TRESEC, TREMIN, TREHR, or TREWK register, the count value can be read. The values read from registers TRESEC, TREMIN, and TREHR are represented by the BCD code.
Write to timer	When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), the value can be written to registers TRESEC, TREMIN, TREHR, and TREWK. The values written to registers TRESEC, TREMIN, and TREHR are represented by the BCD codes.
Select function	12-hour mode/24-hour mode switch function

20.2.1 Timer RE Second Data Register (TRESEC) in Real-Time Clock Mode

Address 0118h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BSY	SC12	SC11	SC10	SC03	SC02	SC01	SC00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	SC00	1st digit of second count bit	Count 0 to 9 every second. When the digit moves up, 1 is added to the 2nd digit of second.	0 to 9 (BCD code)	R/W
b1	SC01				R/W
b2	SC02				R/W
b3	SC03				R/W
b4	SC10	2nd digit of second count bit	When counting 0 to 5, 60 seconds are counted.	0 to 5 (BCD code)	R/W
b5	SC11				R/W
b6	SC12				R/W
b7	BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated		R

20.2.2 Timer RE Minute Data Register (TREMIN) in Real-Time Clock Mode

Address 0119h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BSY	MN12	MN11	MN10	MN03	MN02	MN01	MN00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	MN00	1st digit of minute count bit	Count 0 to 9 every minute. When the digit moves up, 1 is added to the 2nd digit of minute.	0 to 9 (BCD code)	R/W
b1	MN01				R/W
b2	MN02				R/W
b3	MN03				R/W
b4	MN10	2nd digit of minute count bit	When counting 0 to 5, 60 minutes are counted.	0 to 5 (BCD code)	R/W
b5	MN11				R/W
b6	MN12				R/W
b7	BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.		R

20.2.3 Timer RE Hour Data Register (TREHR) in Real-Time Clock Mode

Address 011Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BSY	—	HR11	HR10	HR03	HR02	HR01	HR00
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	Setting Range	R/W
b0	HR00	1st digit of hour count bit	Count 0 to 9 every hour. When the digit moves up, 1 is added to the 2nd digit of hour.	0 to 9 (BCD code)	R/W
b1	HR01				R/W
b2	HR02				R/W
b3	HR03				R/W
b4	HR10	2nd digit of hour count bit	Count 0 to 1 when the H12_H24 bit is set to 0 (12-hour mode). Count 0 to 2 when the H12_H24 bit is set to 1 (24-hour mode).	0 to 2 (BCD code)	R/W
b5	HR11				R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.			—
b7	BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.		R

20.2.4 Timer RE Day of Week Data Register (TREWK) in Real-Time Clock Mode

Address 011Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BSY	—	—	—	—	WK2	WK1	WK0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	WK0	Day of week count bit	b2 b1 b0 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Do not set.	R/W
b1	WK1			R/W
b2	WK2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	BSY	Timer RE busy flag	This bit is set to 1 while registers TRESEC, TREMIN, TREHR, and TREWK are updated.	R

20.2.5 Timer RE Control Register 1 (TRECR1) in Real-Time Clock Mode

Address 011Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	H12_H24	PM	TRERST	INT	TOENA	TCSTF	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	TCSTF	Timer RE count status flag	0: Count stopped 1: Counting	R
b2	TOENA	TREO pin output enable bit	0: Disable clock output 1: Enable clock output	R/W
b3	INT	Interrupt request timing bit	Set to 1 in real-time clock mode.	R/W
b4	TRERST	Timer RE reset bit	When setting this bit to 0, after setting it to 1, the followings will occur. • Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2 are set to 00h. • Bits TCSTF, INT, PM, H12_H24, and TSTART in the TRECR1 register are set to 0. • The 8-bit counter is set to 00h and the 4-bit counter is set to 0h.	R/W
b5	PM	A.m./p.m. bit	When the H12_H24 bit is set to 0 (12-hour mode) (1) 0: a.m. 1: p.m. When the H12_H24 bit is set to 1 (24-hour mode), its value is undefined.	R/W
b6	H12_H24	Operating mode select bit	0: 12-hour mode 1: 24-hour mode	R/W
b7	TSTART	Timer RE count start bit	0: Count stops 1: Count starts	R/W

Note:
1. This bit is automatically modified while timer RE counts.

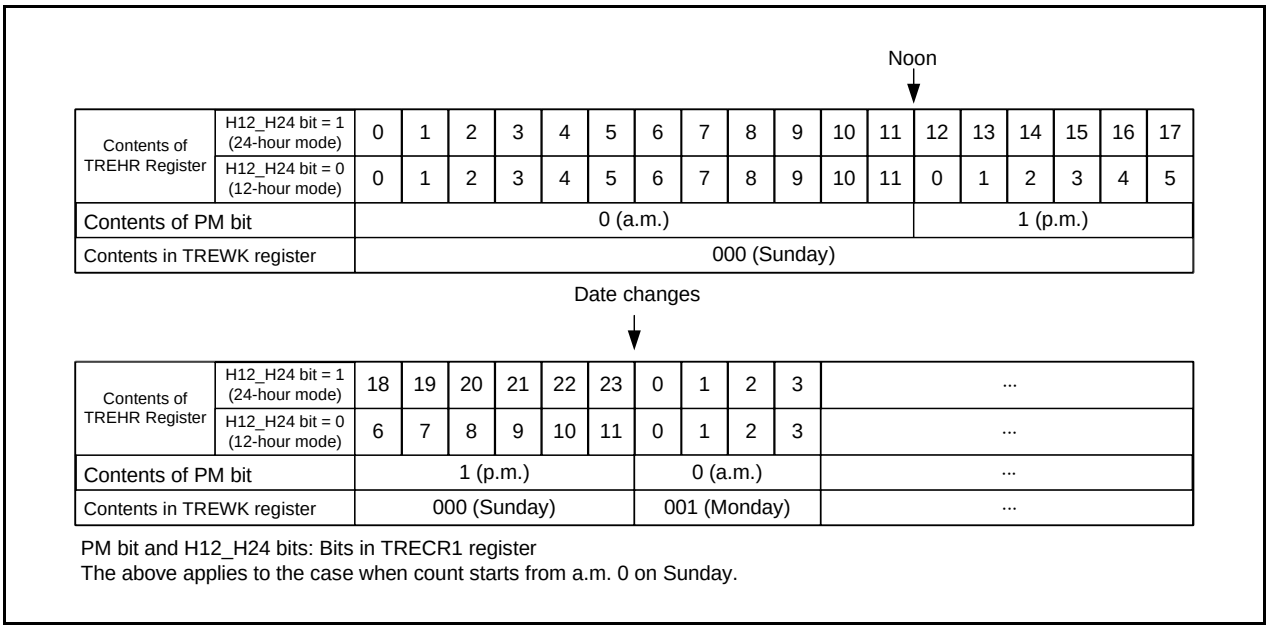


Figure 20.2 Definition of Time Representation

20.2.6 Timer RE Control Register 2 (TRECR2) in Real-Time Clock Mode

Address 011Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	COMIE	WKIE	DYIE	HRIE	MNIE	SEIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SEIE	Periodic interrupt triggered every second enable bit (1)	0: Disable periodic interrupt triggered every second 1: Enable periodic interrupt triggered every second	R/W
b1	MNIE	Periodic interrupt triggered every minute enable bit (1)	0: Disable periodic interrupt triggered every minute 1: Enable periodic interrupt triggered every minute	R/W
b2	HRIE	Periodic interrupt triggered every hour enable bit (1)	0: Disable periodic interrupt triggered every hour 1: Enable periodic interrupt triggered every hour	R/W
b3	DYIE	Periodic interrupt triggered every day enable bit (1)	0: Disable periodic interrupt triggered every day 1: Enable periodic interrupt triggered every day	R/W
b4	WKIE	Periodic interrupt triggered every week enable bit (1)	0: Disable periodic interrupt triggered every week 1: Enable periodic interrupt triggered every week	R/W
b5	COMIE	Compare match interrupt enable bit	Set to 0 in real-time clock mode.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Note:
1. Do not set multiple enable bits to 1 (enable interrupt).

Table 20.3 Interrupt Sources

Factor	Interrupt Source	Interrupt Enable Bit
Periodic interrupt triggered every week	Value in TREWK register is set to 000b (Sunday) (1-week period)	WKIE
Periodic interrupt triggered every day	TREWK register is updated (1-day period)	DYIE
Periodic interrupt triggered every hour	TREHR register is updated (1-hour period)	HRIE
Periodic interrupt triggered every minute	TREMIN register is updated (1-minute period)	MNIE
Periodic interrupt triggered every second	TRESEC register is updated (1-second period)	SEIE

20.2.7 Timer RE Count Source Select Register (TRECSR) in Real-Time Clock Mode

Address 011Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RCS6	RCS5	RCS4	RCS3	RCS2	RCS1	RCS0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RCS0	Count source select bit	Set to 00b in real-time clock mode.	R/W
b1	RCS1			R/W
b2	RCS2	4-bit counter select bit	Set to 0 in real-time clock mode.	R/W
b3	RCS3	Real-time clock mode select bit	Set to 1 in real-time clock mode.	R/W
b4	RCS4	Clock output select bit (1)	b6 b5 b4 0 0 0: f2 0 0 1: fC 0 1 0: f4 0 1 1: 1Hz 1 0 0: f8 Other than above: Do not set.	R/W
b5	RCS5			R/W
b6	RCS6			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Note:
1. Write to bits RCS4 to RCS6 when the TOENA bit in the TRECR1 register is set to 0 (disable clock output).

20.2.8 Operating Example

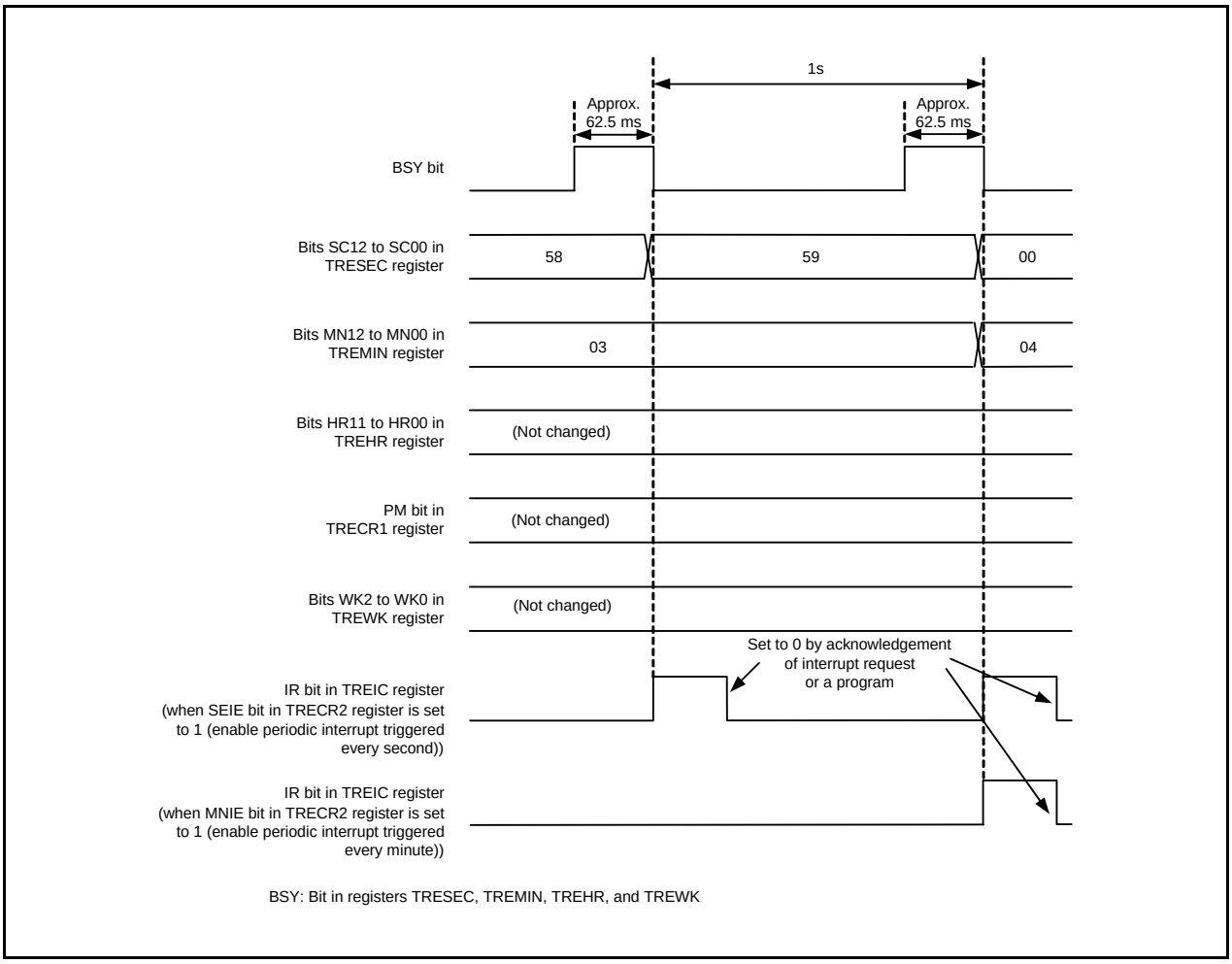


Figure 20.3 Operating Example in Real-Time Clock Mode

20.3 Output Compare Mode

In output compare mode, the internal count source divided by 2 is counted using the 4-bit or 8-bit counter and compare value match is detected with the 8-bit counter. Figure 20.4 shows a Block Diagram of Output Compare Mode and Table 20.4 lists the Output Compare Mode Specifications. Figure 20.5 shows the Operating Example in Output Compare Mode.

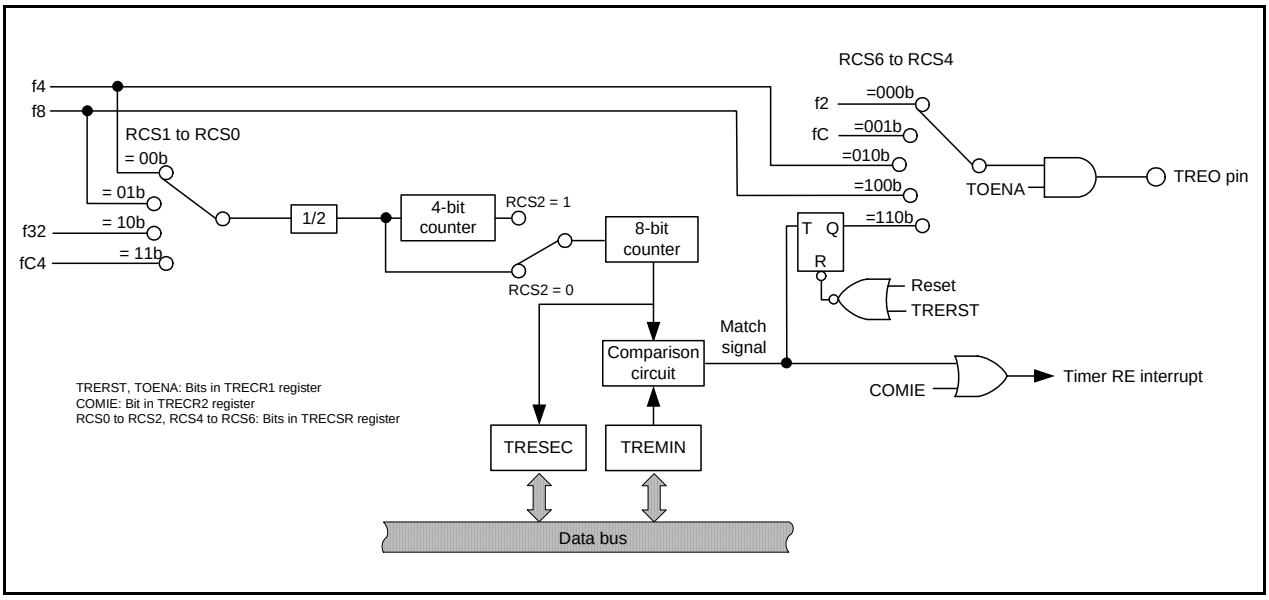


Figure 20.4 Block Diagram of Output Compare Mode

Table 20.4 Output Compare Mode Specifications

Item	Specification
Count sources	f4, f8, f32, fC4
Count operations	• Increment • When the 8-bit counter content matches with the TREMIN register content, the value returns to 00h and count continues. The count value is held while count stops.
Count period	• When RCS2 = 0 (4-bit counter is not used) 1/fi x 2 x (n+1) • When RCS2 = 1 (4-bit counter is used) 1/fi x 32 x (n+1) fi: Frequency of count source n: Setting value of TREMIN register
Count start condition	1 (count starts) is written to the TSTART bit in the TRECR1 register
Count stop condition	0 (count stops) is written to the TSTART bit in the TRECR1 register
Interrupt request generation timing	When the 8-bit counter content matches with the TREMIN register content
TREO pin function	Select any one of the following: • Programmable I/O ports • Output f2, fC, f4, or f8 • Compare output
Read from timer	When reading the TRESEC register, the 8-bit counter value can be read. When reading the TREMIN register, the compare value can be read.
Write to timer	Writing to the TRESEC register is disabled. When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), writing to the TREMIN register is enabled.
Selectable functions	• Select use of 4-bit counter • Compare output function Every time the 8-bit counter value matches the TREMIN register value, TREO output polarity is reversed. The TREO pin outputs “L” after reset is deasserted and the timer RE is reset by the TRERST bit in the TRECR1 register. Output level is held by setting the TSTART bit to 0 (count stops).

20.3.1 Timer RE Counter Data Register (TRESEC) in Output Compare Mode

Address 0118h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b7 to b0	8-bit counter data can be read. Although Timer RE stops counting, the count value is held. The TRESEC register is set to 00h at the compare match.	R

20.3.2 Timer RE Compare Data Register (TREMIN) in Output Compare Mode

Address 0119h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b7 to b0	8-bit compare data is stored.	R/W

20.3.3 Timer RE Control Register 1 (TRECR1) in Output Compare Mode

Address 011Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TSTART	H12_H24	PM	TRERST	INT	TOENA	TCSTF	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	TCSTF	Timer RE count status flag	0: Count stopped 1: Counting	R
b2	TOENA	TREO pin output enable bit	0: Disable clock output 1: Enable clock output	R/W
b3	INT	Interrupt request timing bit	Set to 0 in output compare mode.	R/W
b4	TRERST	Timer RE reset bit	When setting this bit to 0, after setting it to 1, the following will occur. • Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2 are set to 00h. • Bits TCSTF, INT, PM, H12_H24, and TSTART in the TRECR1 register are set to 0. • The 8-bit counter is set to 00h and the 4-bit counter is set to 0h.	R/W
b5	PM	A.m./p.m. bit	Set to 0 in output compare mode.	R/W
b6	H12_H24	Operating mode select bit		R/W
b7	TSTART	Timer RE count start bit	0: Count stops 1: Count starts	R/W

20.3.4 Timer RE Control Register 2 (TRECR2) in Output Compare Mode

Address 011Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	COMIE	WKIE	DYIE	HRIE	MNIE	SEIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SEIE	Periodic interrupt triggered every second enable bit	Set to 0 in output compare mode.	R/W
b1	MNIE	Periodic interrupt triggered every minute enable bit		R/W
b2	HRIE	Periodic interrupt triggered every hour enable bit		R/W
b3	DYIE	Periodic interrupt triggered every day enable bit		R/W
b4	WKIE	Periodic interrupt triggered every week enable bit		R/W
b5	COMIE	Compare match interrupt enable bit	0: Disable compare match interrupt 1: Enable compare match interrupt	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

20.3.5 Timer RE Count Source Select Register (TRECSR) in Output Compare Mode

Address 011Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RCS6	RCS5	RCS4	RCS3	RCS2	RCS1	RCS0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RCS0	Count source select bit (1)	b1 b0 0 0: f4 0 1: f8 1 0: f32 1 1: fC4	R/W
b1	RCS1			R/W
b2	RCS2	4-bit counter select bit (1)	0: Not used 1: Used	R/W
b3	RCS3	Real-time clock mode select bit	Set to 0 in output compare mode.	R/W
b4	RCS4	Clock output select bit (2)	b6 b5 b4 0 0 0: f2 0 0 1: fC 0 1 0: f4 1 0 0: f8 1 1 0: Compare output Other than above: Do not set.	R/W
b5	RCS5			R/W
b6	RCS6			R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. Write to bits RCS0 to RCS2 when the TCSTF bit in the TRECR1 register is set to 0 (count stopped).
2. Write to bits RCS4 to RCS6 when the TOENA bit in the TRECR1 register is set to 0 (disable clock output).

20.3.6 Operating Example

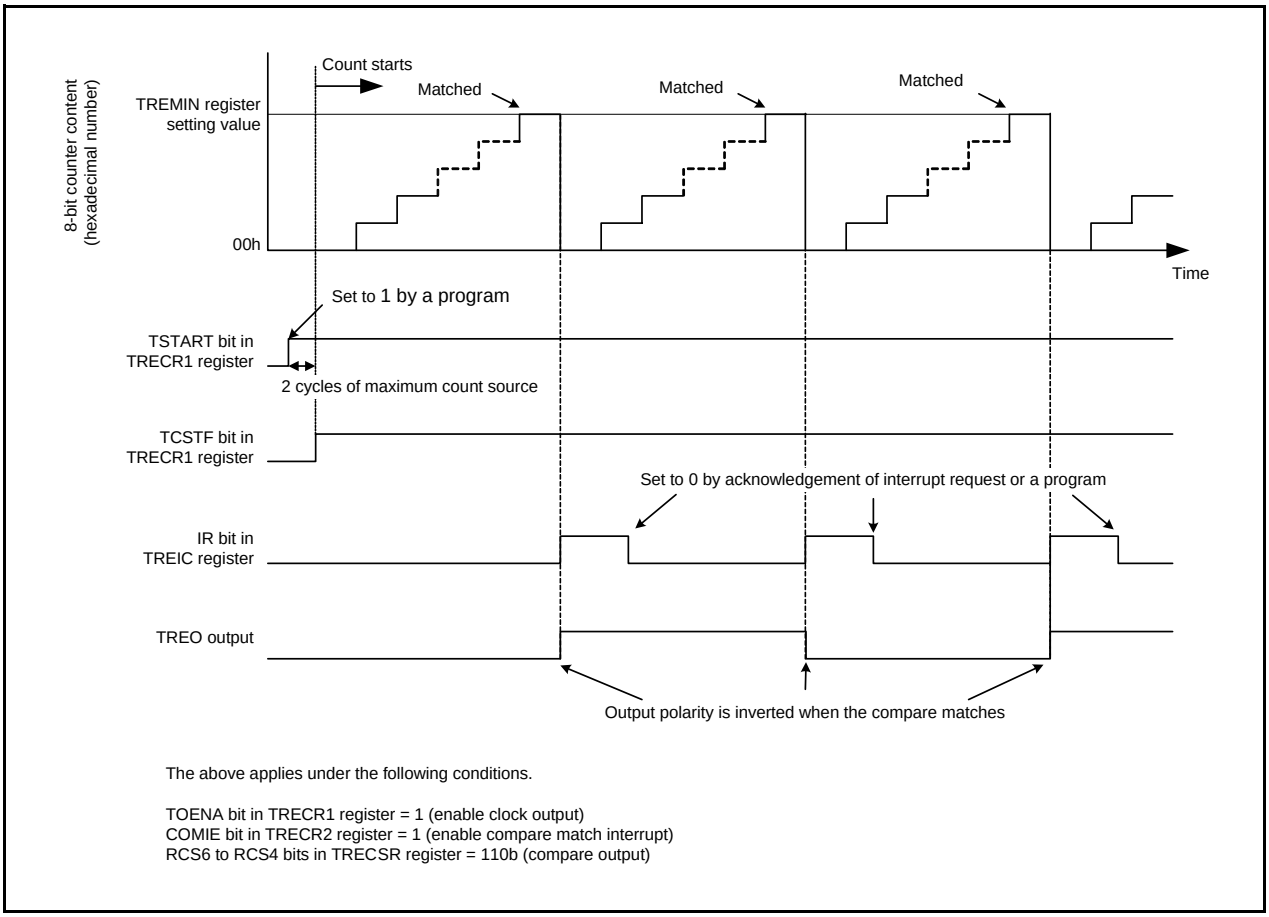


Figure 20.5 Operating Example in Output Compare Mode

20.4 Notes on Timer RE

20.4.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the TRECR1 register.
Timer RE starts counting and the TCSTF bit is set to 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to 2 cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE (1) other than the TCSTF bit.
Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

Note:
1. Registers associated with timer RE: TREMIN, TREHR, TREWK, TRECR1, TRECR2, and TRECSR.

20.4.2 Register Setting

Write to the following registers or bits when timer RE is stopped.
- Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2
- Bits H12_H24, PM, and INT in TRECR1 register
- Bits RCS0 to RCS3 in TRECSR register

Timer RE is stopped when bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer RE stopped).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.
Figure 20.6 shows a Setting Example in Real-Time Clock Mode.

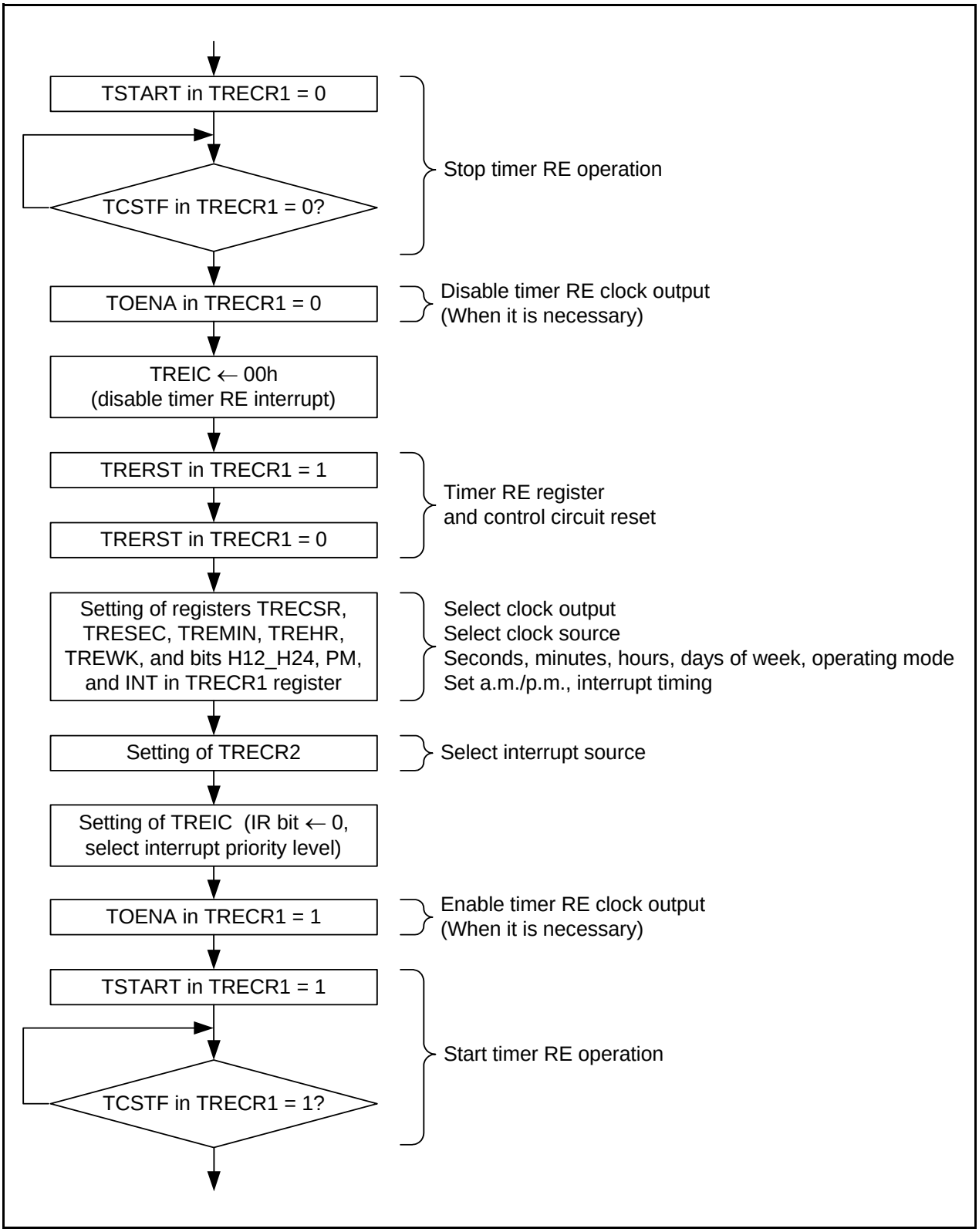


Figure 20.6 Setting Example in Real-Time Clock Mode

20.4.3 Time Reading Procedure of Real-Time Clock Mode

In real-time clock mode, read registers TRESEC, TREMIN, TREHR, and TREWK when time data is updated and read the PM bit in the TRECR1 register when the BSY bit is set to 0 (not while data is updated).
Also, when reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.
In order to prevent this, use the reading procedure shown below.

- Using an interrupt
  Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register in the timer RE interrupt routine.

- Monitoring with a program 1
  Monitor the IR bit in the TREIC register with a program and read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the IR bit in the TREIC register is set to 1 (timer RE interrupt request generated).

- Monitoring with a program 2

(1) Monitor the BSY bit.
(2) Monitor until the BSY bit is set to 0 after the BSY bit is set to 1 (approximately 62.5 ms while the BSY bit is set to 1).
(3) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the BSY bit is set to 0.

- Using read results if they are the same value twice

(1) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register.
(2) Read the same register as (1) and compare the contents.
(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.

Also, when reading several registers, read them as continuously as possible.

21. Serial Interface (UART0)

The serial interface consists of one channel, UART0.

21.1 Overview

UART0 has a dedicated timer to generate a transfer clock and operate independently. UART0 supports clock synchronous serial I/O mode and clock asynchronous serial I/O mode (UART mode).
Figure 21.1 shows a UART0 Block Diagram. Figure 21.2 shows a Block Diagram of UART0 Transmit/Receive Unit. Table 21.1 lists the Pin Configuration of UART0.

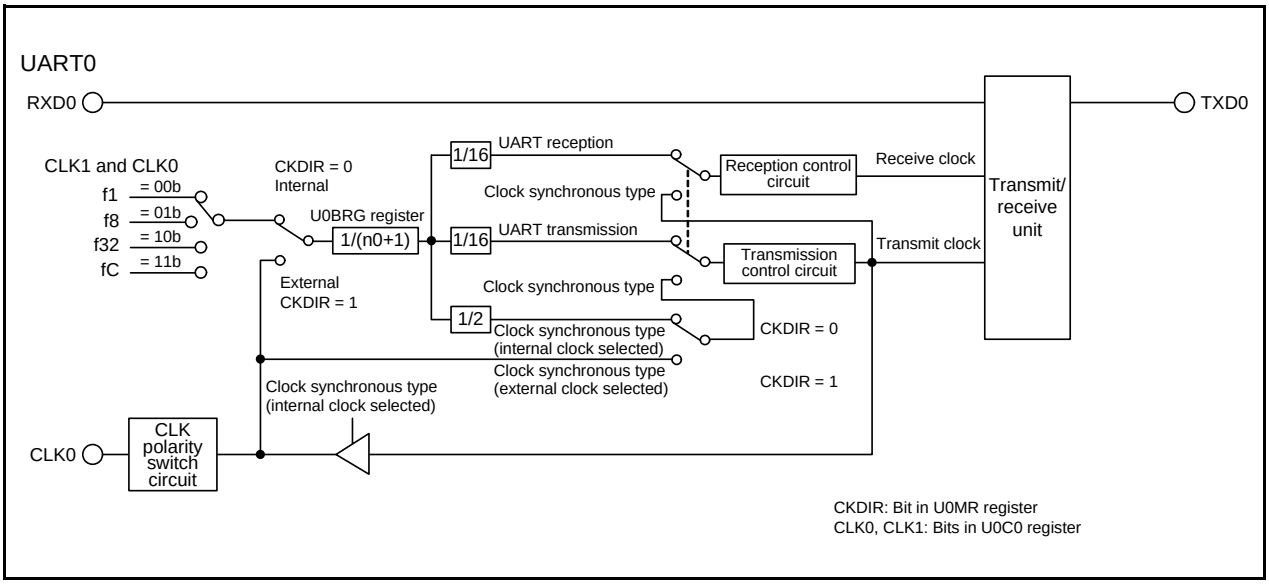


Figure 21.1 UART0 Block Diagram

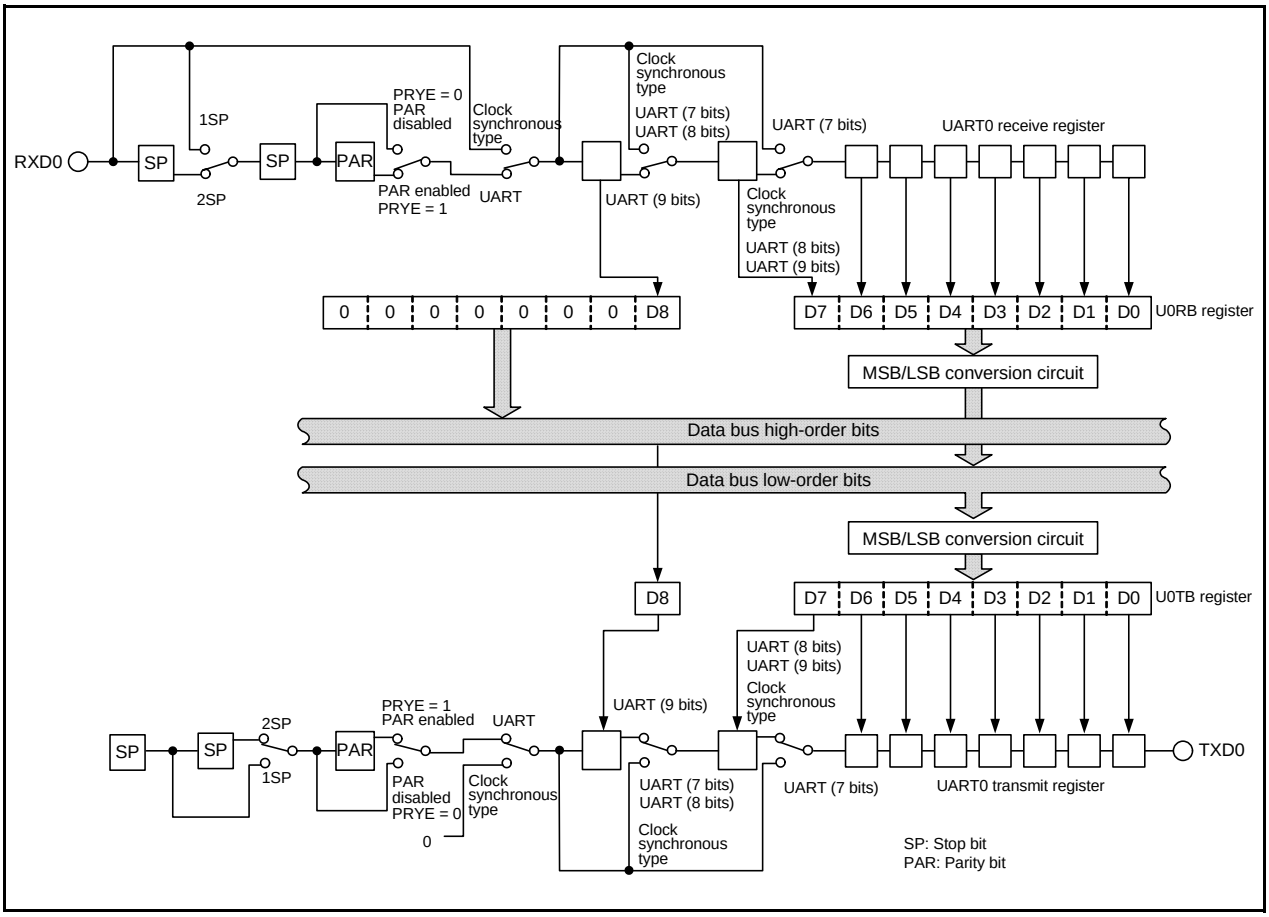


Figure 21.2 Block Diagram of UART0 Transmit/Receive Unit

Table 21.1 Pin Configuration of UART0

Pin Name	Assigned Pin	I/O	Function
TXD0	P1_4	Output	Serial data output
RXD0	P1_5	Input	Serial data input
CLK0	P1_6	I/O	Transfer clock I/O

21.2 Registers

21.2.1 UART0 Transmit/Receive Mode Register (U0MR)

Address 00A0h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	PRYE	PRY	STPS	CKDIR	SMD2	SMD1	SMD0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 0: Serial interface disabled 0 0 1: Clock synchronous serial I/O mode 1 0 0: UART mode, transfer data 7 bits long 1 0 1: UART mode, transfer data 8 bits long 1 1 0: UART mode, transfer data 9 bits long Other than above: Do not set.	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock 1: External clock	R/W
b4	STPS	Stop bit length select bit	0: One stop bit 1: Two stop bits	R/W
b5	PRY	Odd/even parity select bit	Enabled when PRYE = 1 0: Odd parity 1: Even parity	R/W
b6	PRYE	Parity enable bit	0: Parity disabled 1: Parity enabled	R/W
b7	—	Reserved bit	Set to 0.	R/W

21.2.2 UART0 Bit Rate Register (U0BRG)

Address 00A1h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, U0BRG divides the count source by n+1.	00h to FFh	W

Write to the U0BRG register while transmission and reception stop.
Use the MOV instruction to write to this register.
Set bits CLK0 and CLK1 in the U0C0 register before writing to the U0BRG register.

21.2.3 UART0 Transmit Buffer Register (U0TB)

Address 00A3h to 00A2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Function	R/W
b0	—	Transmit data	W
b1	—		
b2	—		
b3	—		
b4	—		
b5	—		
b6	—		
b7	—		
b8	—		
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.	—
b10	—		
b11	—		
b12	—		
b13	—		
b14	—		
b15	—		

If the transfer data is 9 bits long, write data to the high-order byte first, then low-order byte of the U0TB register.
Use the MOV instruction to write to this register.

21.2.4 UART0 Transmit/Receive Control Register 0 (U0C0)

Address 00A4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	UFORM	CKPOL	NCH	—	TXEPT	—	CLK1	CLK0
After Reset	0	0	0	0	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	BRG count source select bit (1)	b1 b0 0 0: f1 selected 0 1: f8 selected 1 0: f32 selected 1 1: fC selected	R/W
b1	CLK1			R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	TXEPT	Transmit register empty flag	0: Data present in the transmit register (transmission in progress) 1: No data in the transmit register (transmission completed)	R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	NCH	Data output select bit	0: TXD0 pin set to CMOS output 1: TXD0 pin set to N-channel open-drain output	R/W
b6	CKPOL	CLK polarity select bit	0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock 1: Transmit data output at the rising edge and receive data input at the falling edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit	0: LSB first 1: MSB first	R/W

Note:
1. If the BRG count source is switched, set the U0BRG register again.

21.2.5 UART0 Transmit/Receive Control Register 1 (U0C1)

Address 00A5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	U0RRM	U0IRS	RI	RE	TI	TE
After Reset	0	0	0	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	0: Transmission disabled 1: Transmission enabled	R/W
b1	TI	Transmit buffer empty flag	0: Data present in the U0TB register 1: No data in the U0TB register	R
b2	RE	Receive enable bit	0: Reception disabled 1: Reception enabled	R/W
b3	RI	Receive complete flag (1)	0: No data in the U0RB register 1: Data present in the U0RB register	R
b4	U0IRS	UART0 transmit interrupt source select bit	0: Transmission buffer empty (TI = 1) 1: Transmission completed (TXEPT = 1)	R/W
b5	U0RRM	UART0 continuous receive mode enable bit (2)	0: Continuous receive mode disabled 1: Continuous receive mode enabled	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. The RI bit is set to 0 when the higher byte of the U0RB register is read.
2. In UART mode, set the U0RRM bit to 0 (continuous receive mode disabled).

21.2.6 UART0 Receive Buffer Register (U0RB)

Address 00A7h to 00A6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	SUM	PER	FER	OER	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b0	—	—	Receive data (D7 to D0)	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			
b8	—	—	Receive data (D8)	R
b9	—	Nothing is assigned. If necessary, set to 0. When read, the content is undefined.		—
b10	—			
b11	—			
b12	OER	Overrun error flag (1)	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag (1, 2)	0: No framing error 1: Framing error	R
b14	PER	Parity error flag (1, 2)	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag (1, 2)	0: No error 1: Error	R

Notes:
1. Bits SUM, PER, FER, and OER are set to 0 (no error) when either of the following is set:
   - Bits SMD2 to SMD0 in the U0MR register are set to 000b (serial interface disabled), or
   - The RE bit in the U0C1 register is set to 0 (reception disabled)

   The SUM bit is set to 0 (no error) when all of bits PER, FER, and OER are set to 0 (no error).
   Bits PER and FER are also set to 0 when the high-order byte of the U0RB register is read.
   When setting bits SMD2 to SMD0 in the U0MR register to 000b, set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
2. These error flags are invalid when bits SMD2 to SMD0 in the U0MR register are set to 001b (clock synchronous serial I/O mode). When read, the content is undefined.

Always read the U0RB register in 16-bit units.

21.2.7 UART0 Pin Select Register (U0SR)

Address 0188h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CLK0SEL0	—	RXD0SEL0	—	TXD0SEL0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	0: TXD0 pin not used 1: P1_4 assigned	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	RXD0SEL0	RXD0 pin select bit	0: RXD0 pin not used 1: P1_5 assigned	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	CLK0SEL0	CLK0 pin select bit	0: CLK0 pin not used 1: P1_6 assigned	R/W
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

The U0SR register selects which pin is assigned to the UART0 I/O. To use the I/O pin for UART0, set this register.
Set the U0SR register before setting the UART0 associated registers. Also, do not change the setting value in this register during UART0 operation.

21.3 Clock Synchronous Serial I/O Mode

In clock synchronous serial I/O mode, data is transmitted and received using a transfer clock.
Table 21.2 lists the Clock Synchronous Serial I/O Mode Specifications. Table 21.3 lists the Registers Used and Settings in Clock Synchronous Serial I/O Mode.

Table 21.2 Clock Synchronous Serial I/O Mode Specifications

Item	Specification
Transfer data format	Transfer data length: 8 bits
Transfer clocks	• The CKDIR bit in the U0MR register is set to 0 (internal clock): fi/(2(n+1)) fi = f1, f8, f32, fC n = setting value in the U0BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): Input from the CLK0 pin
Transmit start conditions	• To start transmission, the following requirements must be met: (1) - The TE bit in the U0C1 register is set to 1 (transmission enabled). - The TI bit in the U0C1 register is set to 0 (data present in the U0TB register).
Receive start conditions	• To start reception, the following requirements must be met: (1) - The RE bit in the U0C1 register is set to 1 (reception enabled). - The TE bit in the U0C1 register is set to 1 (transmission enabled). - The TI bit in the U0C1 register is set to 0 (data present in the U0TB register).
Interrupt request generation timing	• For transmission: One of the following can be selected. - The U0IRS bit is set to 0 (transmit buffer empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). - The U0IRS bit is set to 1 (transmission completed): When data transmission from the UART0 transmit register is completed. • For reception: When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	Overrun error (2) This error occurs if the serial interface starts receiving the next unit of data before reading the U0RB register and receives the 7th bit of the next unit of data.
Selectable functions	• CLK polarity selection Transfer data input/output can be selected to occur synchronously with the rising or the falling edge of the transfer clock. • LSB first, MSB first selection Whether transmitting or receiving data begins with bit 0 or begins with bit 7 can be selected. • Continuous receive mode selection Reception is enabled immediately by reading the U0RB register.

Notes:
1. When an external clock is selected, the requirements must be met in either of the following states:
   - The external clock is held high when the CKPOL bit in the U0C0 register is set to 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
   - The external clock is held low when the CKPOL bit in the U0C0 register is set to 1 (transmit data output at the rising edge and receive data input at the falling edge of the transfer clock)
2. If an overrun error occurs, the receive data (b0 to b8) in the U0RB register will be undefined. The IR bit in the S0RIC register remains unchanged.

Table 21.3 Registers Used and Settings in Clock Synchronous Serial I/O Mode (1)

Register	Bit	Function
U0TB	b0 to b7	Set data transmission.
U0RB	b0 to b7	Receive data can be read.
	OER	Overrun error flag
U0BRG	b0 to b7	Set a bit rate.
U0MR	SMD2 to SMD0	Set to 001b.
	CKDIR	Select the internal clock or external clock.
U0C0	CLK1, CLK0	Select the count source for the U0BRG register.
	TXEPT	Transmit register empty flag
	NCH	Select TXD0 pin output mode.
	CKPOL	Select the transfer clock polarity.
	UFORM	Select LSB first or MSB first.
U0C1	TE	Set to 1 to enable transmission/reception
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U0IRS	Select the UART0 transmit interrupt source.
	U0RRM	Set to 1 to use continuous receive mode.

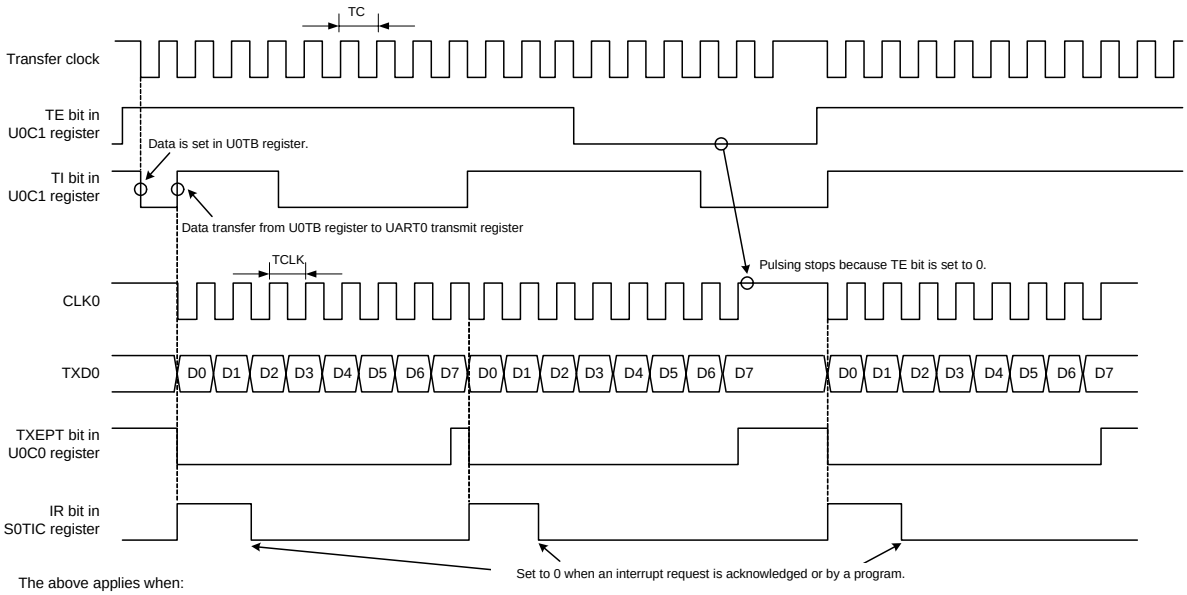
Note:
1. Set the bits not listed in this table to 0 when writing to the above registers in clock synchronous serial I/O mode.

Table 21.4 lists the I/O Pin Functions in Clock Synchronous Serial I/O Mode.
After UART0 operating mode is selected, the TXD0 pin outputs a “H” level until transfer starts. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

Table 21.4 I/O Pin Functions in Clock Synchronous Serial I/O Mode

Pin Name	Function	Selection Method
TXD0 (P1_4)	Serial data output	TXD0SEL0 bit in U0SR register = 1 For reception only: P1_4 can be used as a port by setting TXD0SEL0 bit = 0.
RXD0 (P1_5)	Serial data input	RXD0SEL0 bit in U0SR register = 1 PD1_5 bit in PD1 register = 0 For transmission only: P1_5 can be used as a port by setting RXD0SEL0 bit = 0.
CLK0 (P1_6)	Transfer clock output	CLK0SEL0 bit in U0SR register = 1 CKDIR bit in U0MR register = 0
	Transfer clock input	CLK0SEL0 bit in U0SR register = 1 CKDIR bit in U0MR register = 1 PD1_6 bit in PD1 register = 0

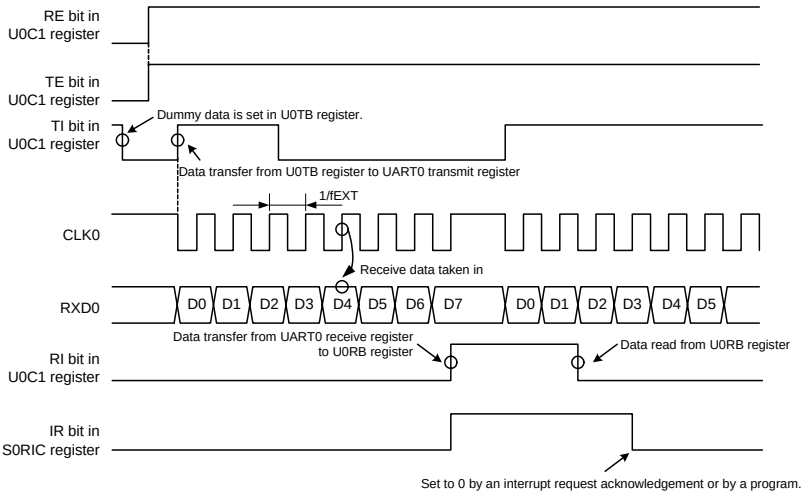
• Transmit Timing Example (Internal Clock Selected)



The above applies when:
- CKDIR bit in U0MR register = 0 (internal clock)
- CKPOL bit in U0C0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)
- U0IRS bit in U0C1 register = 0 (interrupt request generation when the transmit buffer is empty)

TC = TCLK = 2(n+1)/fi
fi: Frequency of U0BRG count source (f1, f8, f32, fC)
n: Setting value in U0BRG register

• Receive Timing Example (External Clock Selected)



The above applies when:
- CKDIR bit in U0MR register = 1 (external clock)
- CKPOL bit in U0C0 register = 0 (transmit data output at the falling edge and receive data input at the rising edge of the transfer clock)

The following should be met when “H” is applied to the CLK0 pin before receiving data:
- TE bit in U0C1 register = 1 (transmission enabled)
- RE bit in U0C1 register = 1 (reception enabled)
- Dummy data is written to U0TB register

fEXT: Frequency of external clock

Figure 21.3 Transmit and Receive Timing in Clock Synchronous Serial I/O Mode

21.3.1 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in clock synchronous serial I/O mode, follow the procedures below:

(1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U0MR register to 001b (clock synchronous serial I/O mode).
(4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

21.3.2 Polarity Select Function

Figure 21.4 shows the Transfer Clock Polarity. Use the CKPOL bit in the U0C0 register to select the transfer clock polarity.

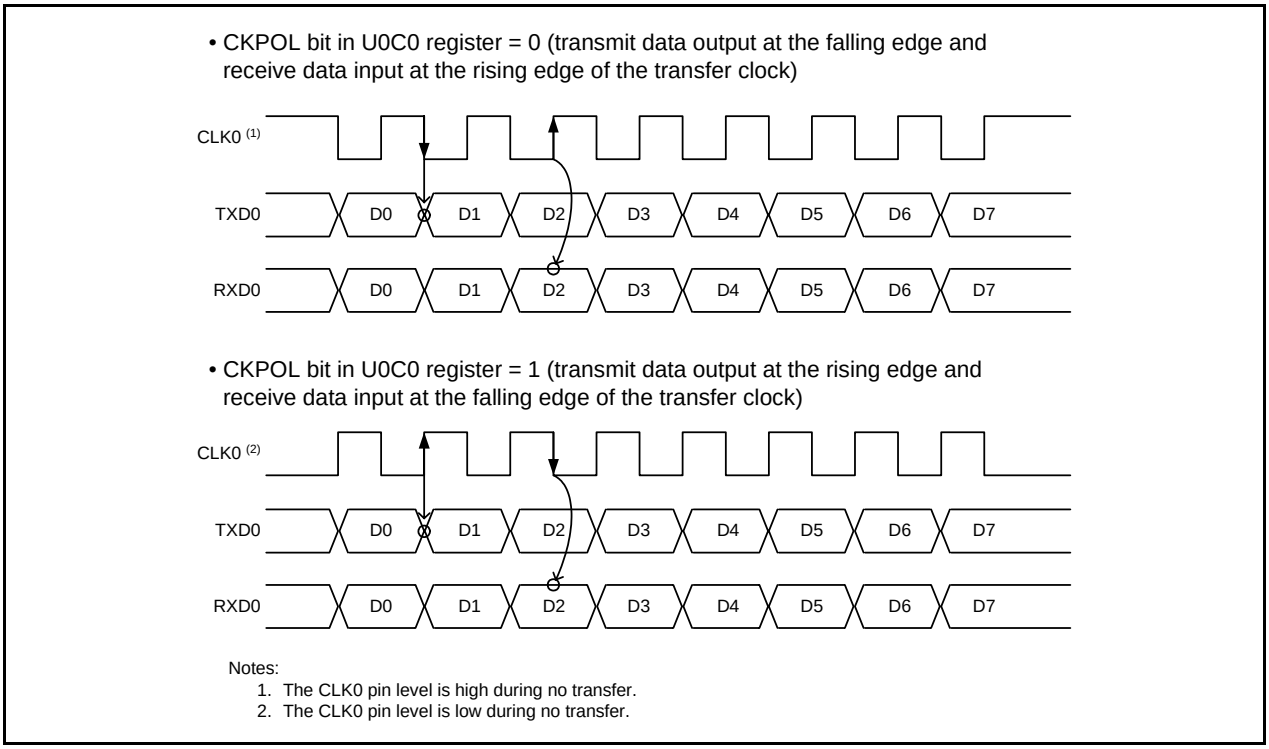


Figure 21.4 Transfer Clock Polarity

21.3.3 LSB First/MSB First Select Function

Figure 21.5 shows the Transfer Format. Use the UFORM bit in the U0C0 register to select the transfer format.

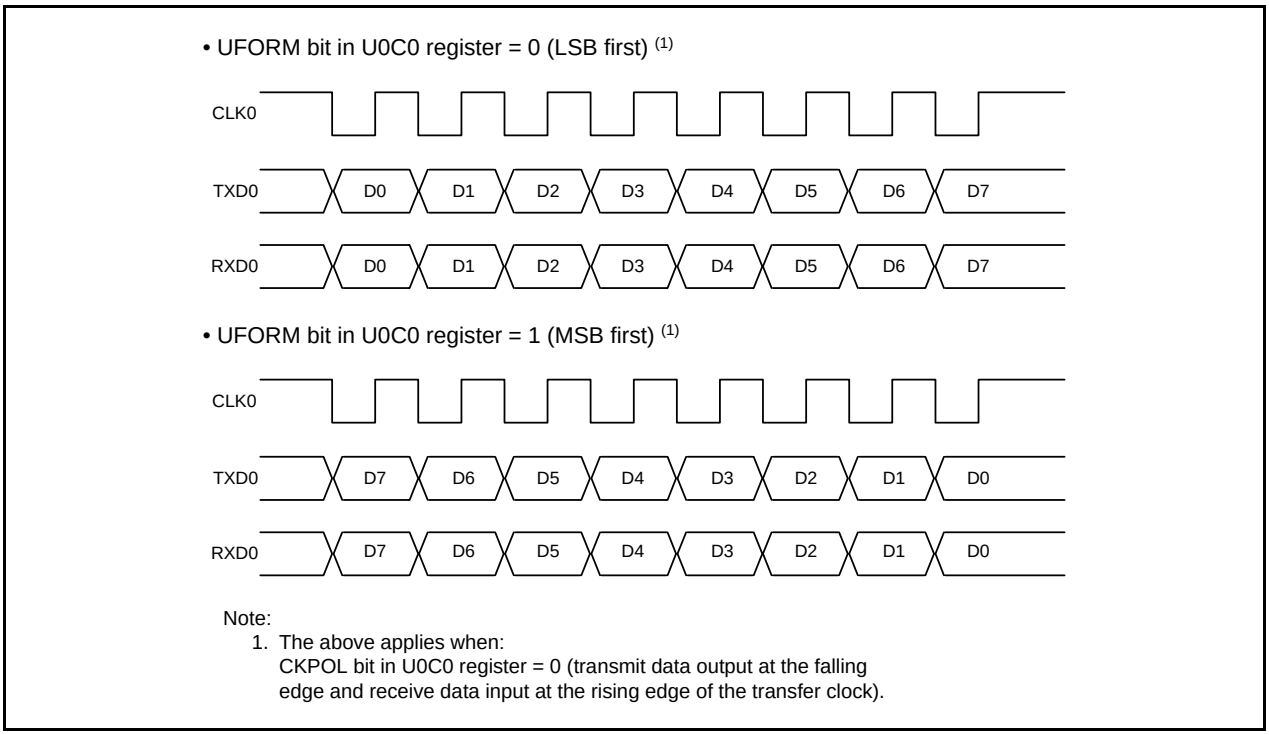


Figure 21.5 Transfer Format

21.3.4 Continuous Receive Mode

Continuous receive mode is selected by setting the U0RRM bit in the U0C1 register to 1 (continuous receive mode enabled). In this mode, reading the U0RB register sets the TI bit in the U0C1 register to 0 (data present in the U0TB register). If the U0RRM bit is set to 1, do not write dummy data to the U0TB register by a program.

21.4 Clock Asynchronous Serial I/O (UART) Mode

The UART mode allows data transmission and reception after setting the desired bit rate and transfer data format. Table 21.5 lists the UART Mode Specifications. Table 21.6 lists the Registers Used and Settings in UART Mode.

Table 21.5 UART Mode Specifications

Item	Specification
Transfer data formats	• Character bits (transfer data): Selectable among 7, 8 or 9 bits • Start bit: 1 bit • Parity bit: Selectable among odd, even, or none • Stop bits: Selectable among 1 or 2 bits
Transfer clocks	• The CKDIR bit in the U0MR register is set to 0 (internal clock): fj/(16(n+1)) fj = f1, f8, f32, fC n = setting value in the U0BRG register: 00h to FFh • The CKDIR bit is set to 1 (external clock): fEXT/(16(n+1)) fEXT: Input from the CLK0 pin n = setting value in the U0BRG register: 00h to FFh
Transmit start conditions	• To start transmission, the following requirements must be met: - The TE bit in the U0C1 register is set to 1 (transmission enabled). - The TI bit in the U0C1 register is set to 0 (data present in the U0TB register).
Receive start conditions	• To start reception, the following requirements must be met: - The RE bit in the U0C1 register is set to 1 (reception enabled). - Start bit detection
Interrupt request generation timing	• For transmission: One of the following can be selected. - The U0IRS bit is set to 0 (transmit buffer empty): When data is transferred from the U0TB register to the UART0 transmit register (at start of transmission). - The U0IRS bit is set to 1 (transfer completed): When data transmission from the UART0 transmit register is completed. • For reception: When data is transferred from the UART0 receive register to the U0RB register (at completion of reception).
Error detection	• Overrun error (1) This error occurs if the serial interface starts receiving the next unit of data before reading the U0RB register and receive the bit one before the last stop bit of the next unit of data. • Framing error This error occurs when the set number of stop bits is not detected. (2) • Parity error This error occurs when parity is enabled, and the number of 1's in the parity and character bits do not match the set number of 1's. (2) • Error sum flag This flag is set to 1 if an overrun, framing, or parity error occurs.

Notes:
1. If an overrun error occurs, the receive data (b0 to b8) in the U0RB register will be undefined.
2. The framing error flag and the parity error flag are set to 1 when data is transferred from the UART0 receive register to the U0RB register.

Table 21.6 Registers Used and Settings in UART Mode

Register	Bit	Function
U0TB	b0 to b8	Set transmit data. (1)
U0RB	b0 to b8	Receive data can be read. (2)
	OER, FER, PER, SUM	Error flag
U0BRG	b0 to b7	Set a bit rate.
U0MR	SMD2 to SMD0	Set to 100b when transfer data is 7 bits long. Set to 101b when transfer data is 8 bits long. Set to 110b when transfer data is 9 bits long.
	CKDIR	Select the internal clock or external clock.
	STPS	Select the stop bit.
	PRY, PRYE	Select whether parity is included and whether odd or even.
U0C0	CLK0, CLK1	Select the count source for the U0BRG register.
	TXEPT	Transmit register empty flag
	NCH	Select TXD0 pin output mode.
	CKPOL	Set to 0.
	UFORM	Select LSB first or MSB first when transfer data is 8 bits long. Set to 0 when transfer data is 7 bits or 9 bits long.
U0C1	TE	Set to 1 to enable transmission.
	TI	Transmit buffer empty flag
	RE	Set to 1 to enable reception.
	RI	Receive complete flag
	U0IRS	Select the UART0 transmit interrupt source.
	U0RRM	Set to 0.

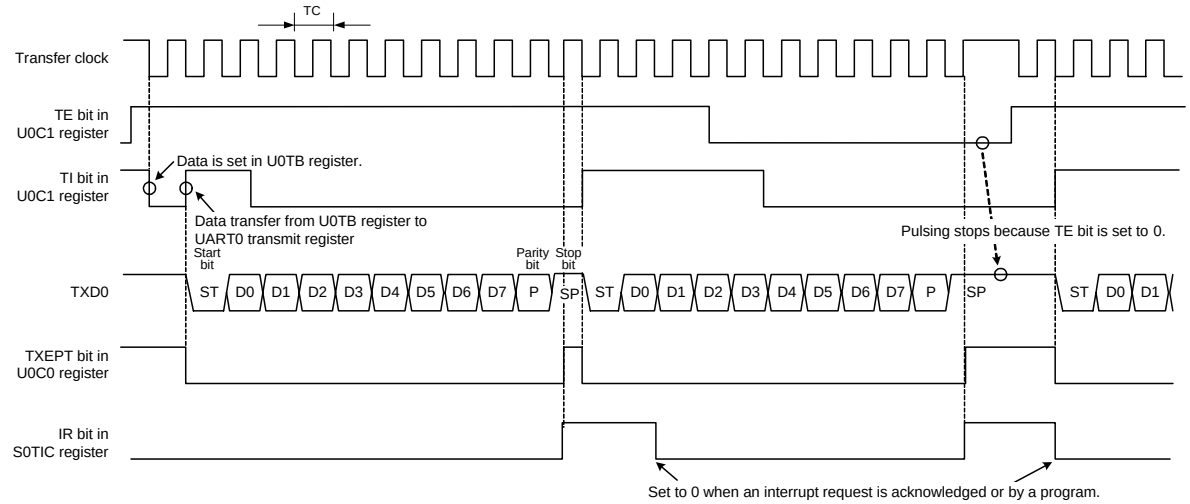
Notes:
1. The bits used for transmission/receive data are as follows:
   - Bits b0 to b6 when transfer data is 7 bits long
   - Bits b0 to b7 when transfer data is 8 bits long
   - Bits b0 to b8 when transfer data is 9 bits long
2. The contents of the following are undefined:
   - Bits 7 and 8 when the transfer data is 7 bits long
   - Bit 8 when the transfer data is 8 bits long

Table 21.7 lists the I/O Pin Functions in UART Mode.
After the UART0 operating mode is selected, the TXD0 pin outputs a “H” level until transfer starts. (If the NCH bit is set to 1 (N-channel open-drain output), this pin is in the high-impedance state.)

Table 21.7 I/O Pin Functions in UART Mode

Pin name	Function	Selection Method
TXD0 (P1_4)	Serial data output	TXD0SEL0 bit in U0SR register = 1 For reception only: P1_4 can be used as a port by setting TXD0SEL0 bit = 0.
RXD0 (P1_5)	Serial data input	RXD0SEL0 bit in U0SR register = 1 PD1_5 bit in PD1 register = 0 For transmission only: P1_5 can be used as a port by setting RXD0SEL0 bit = 0.
CLK0 (P1_6)	Programmable I/O port	CLK0SEL0 bit in U0SR register = 0 (CLK0 pin not used)
	Transfer clock input	CLK0SEL0 bit in U0SR register = 1 CKDIR bit in U0MR register = 1 PD1_6 bit in PD1 register = 0

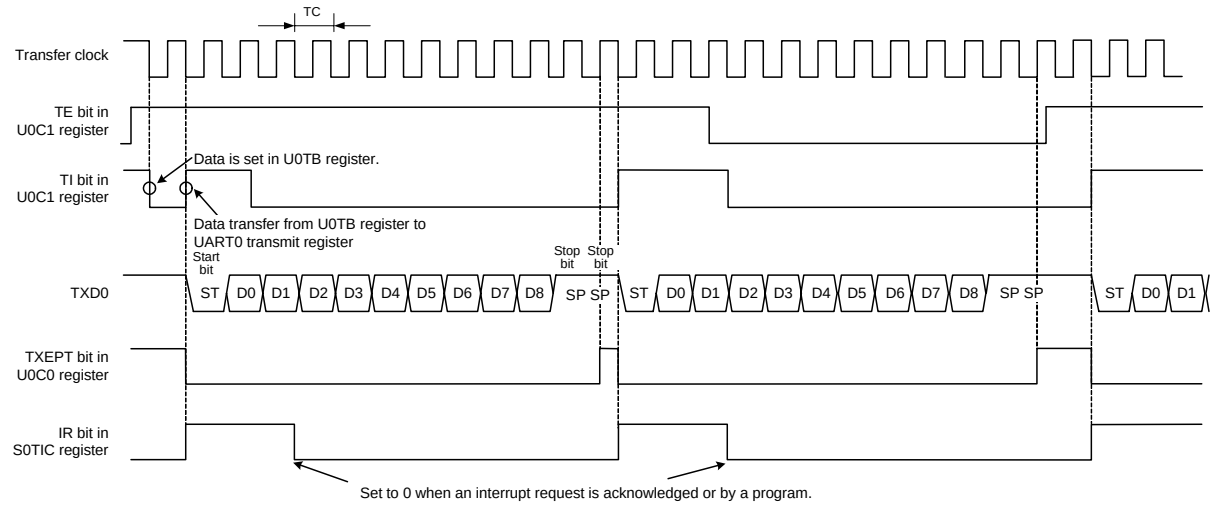
• Transmit Timing Example When Transfer Data 8 Bits is Long (Parity Enabled, One Stop Bit)



The above applies when:
- PRYE bit in U0MR register = 1 (parity enabled)
- STPS bit in U0MR register = 0 (one stop bit)
- U0IRS bit in U0C1 register = 1
  (interrupt request generation when transmission is completed)

TC = 16(n+1)/fj or 16(n+1)/fEXT
fj: Frequency of U0BRG count source (f1, f8, f32, fC)
fEXT: Frequency of U0BRG count source (external clock)
n: Setting value in U0BRG register

• Transmit Timing Example When Transfer Data is 9 Bits Long (Parity Disabled, Two Stop Bits)



The above applies when:
- PRYE bit in U0MR register = 0 (parity disabled)
- STPS bit in U0MR register = 1 (two stop bits)
- U0IRS bit in U0C1 register = 0
  (interrupt request generation when the transmit buffer is empty)

TC = 16(n+1)/fj or 16(n+1)/fEXT
fj: Frequency of U0BRG count source (f1, f8, f32, fC)
fEXT: Frequency of U0BRG count source (external clock)
n: Setting value in U0BRG register

Figure 21.6 Transmit Timing in UART Mode

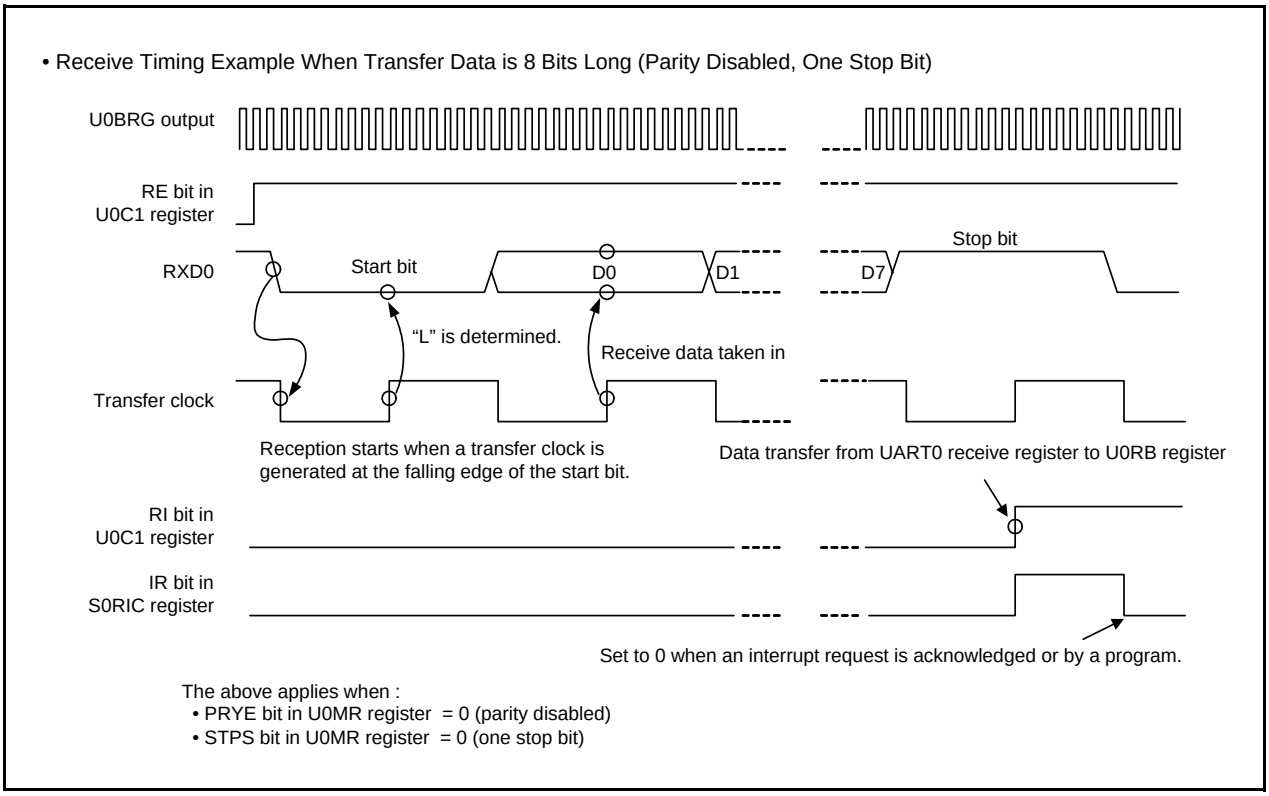


Figure 21.7 Receive Timing in UART Mode

21.4.1 Bit Rate

In UART mode, the bit rate is the frequency divided by the U0BRG register and divided by 16.

UART mode

- Internal clock selected

$$\text{Setting value in U0BRG register} = \frac{fj}{\text{Bit Rate} \times 16} - 1$$

fj: Count source frequency of U0BRG register (f1, f8, f32, or fC)

- External clock selected

$$\text{Setting value in U0BRG register} = \frac{fEXT}{\text{Bit Rate} \times 16} - 1$$

fEXT: Count source frequency of U0BRG register (external clock)

Figure 21.8 Formula for Calculating Setting Value in U0BRG Register

Table 21.8 Bit Rate Setting Example in UART Mode (Internal Clock Selected)

Bit Rate (bps)	U0BRG Count Source	System Clock = 16 MHz		
		U0BRG Setting Value	Actual Time (bps)	Setting Error (%)
1200	f8	103 (67h)	1201.92	0.16
2400	f8	51 (33h)	2403.85	0.16
4800	f8	25 (19h)	4807.69	0.16
9600	f1	103 (67h)	9615.38	0.16
14400	f1	68 (44h)	14492.75	0.64
19200	f1	51 (33h)	19230.77	0.16
28800	f1	34 (22h)	28571.43	–0.79
38400	f1	25 (19h)	38461.54	0.16
57600	f1	16 (10h)	58823.53	2.12
115200	f1	8 (08h)	111111.11	–3.55

21.4.2 Measure for Dealing with Communication Errors

If communication is aborted or a communication error occurs while transmitting or receiving in UART mode, follow the procedures below:

(1) Set the TE bit in the U0C1 register to 0 (transmission disabled) and the RE bit to 0 (reception disabled).
(2) Set bits SMD2 to SMD0 in the U0MR register to 000b (serial interface disabled).
(3) Set bits SMD2 to SMD0 in the U0MR register to 100b (UART mode, transfer data 7 bits long), 101b (UART mode, transfer data 8 bits long), or 110b (UART mode, transfer data 9 bits long).
(4) Set the TE bit in the U0C1 register to 1 (transmission enabled) and the RE bit to 1 (reception enabled).

21.5 Notes on Serial Interface (UART0)

- When reading data from the U0RB register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
  When the high-order byte of the U0RB register is read, bits PER and FER in the U0RB register and the RI bit in the U0C1 register are set to 0.
  To check receive errors, read the U0RB register and then use the read data.

  Program example to read the receive buffer register:

```
MOV.W    00A6H, R0    ; Read the U0RB register
```

- When writing data to the U0TB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

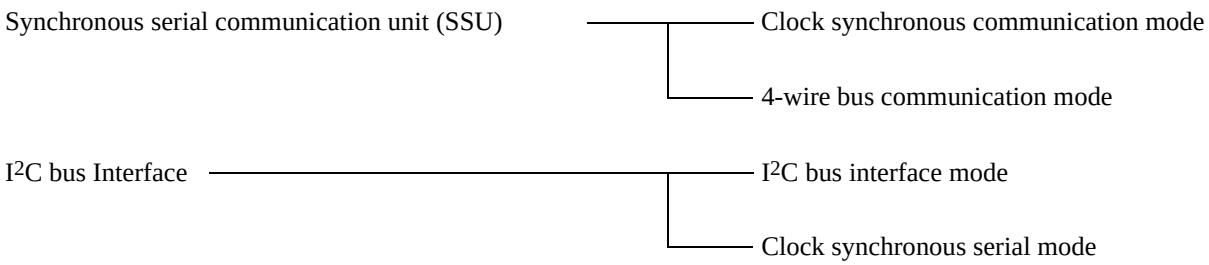
  Program example to write to the transmit buffer register:

```
MOV.B    #XXH, 00A3H  ; Write to the high-order byte of the U0TB register
MOV.B    #XXH, 00A2H  ; Write to the low-order byte of the U0TB register
```

22. Clock Synchronous Serial Interface

The clock synchronous serial interface is configured as follows.

Clock synchronous serial interface



The clock synchronous serial interface uses the registers at addresses 0193h to 019Dh. Registers, bits, symbols, and functions vary even for the same addresses depending on the mode. Refer to the registers of each function for details. Also, the differences between clock synchronous communication mode and clock synchronous serial mode are the options of the transfer clock, clock output format, and data output format.

22.1 Mode Selection

The clock synchronous serial interface has four modes.
Table 22.1 lists the Mode Selections. Refer to **23. Synchronous Serial Communication Unit (SSU)**, **24. I2C bus Interface** and the sections that follow for details of each mode.

Table 22.1 Mode Selections

IICSEL Bit in SSUIICSR Register	Bit 7 in 0198h (ICE Bit in ICCR1 Register)	Bit 0 in 019Dh (SSUMS Bit in SSMR2 Register, FS Bit in SAR Register)	Function	Mode
0	0	0	Synchronous serial communication unit	Clock synchronous communication mode
0	0	1		4-wire bus communication mode
1	1	0	I2C bus interface	I2C bus interface mode
1	1	1		Clock synchronous serial mode

23. Synchronous Serial Communication Unit (SSU)

Synchronous serial communication unit (SSU) supports clock synchronous serial data communication.

23.1 Overview

Table 23.1 shows a Synchronous Serial Communication Unit Specifications and Figure 23.1 shows a Block Diagram of Synchronous Serial Communication Unit. Table 23.2 Pin Configuration of Synchronous Serial Communication Unit

Table 23.1 Synchronous Serial Communication Unit Specifications

Item	Specification
Transfer data format	Transfer data length: 8 to 16 bits Continuous transmission and reception of serial data are supported since both transmitter and receiver have buffer structures.
Operating modes	• Clock synchronous communication mode • 4-wire bus communication mode (including bidirectional communication)
Master/slave device	Selectable
I/O pins	SSCK (I/O): Clock I/O pin SSI (I/O): Data I/O pin SSO (I/O): Data I/O pin SCS (I/O): Chip-select I/O pin
Transfer clocks	• When the MSS bit in the SSCRH register is set to 0 (operates as slave device), external clock is selected (input from SSCK pin). • When the MSS bit in the SSCRH register is set to 1 (operates as master device), internal clock (selectable among f1/256, f1/128, f1/64, f1/32, f1/16, f1/8 and f1/4, output from SSCK pin) is selected. • Clock polarity and phase of SSCK can be selected.
Receive error detection	• Overrun error Overrun error occurs during reception and completes in error. While the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and when next serial data receive is completed, the ORER bit is set to 1.
Multimaster error detection	• Conflict error When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operates as master device) and when starting a serial communication, the CE bit in the SSSR register is set to 1 if “L” applies to the SCS pin input. When the SSUMS bit in the SSMR2 register is set to 1 (4-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operates as slave device) and the SCS pin input changes state from “L” to “H”, the CE bit in the SSSR register is set to 1.
Interrupt requests	5 interrupt requests (transmit-end, transmit-data-empty, receive-data-full, overrun error, and conflict error). (1)
Selectable functions	• Data transfer direction Selects MSB-first or LSB-first • SSCK clock polarity Selects “L” or “H” level when clock stops • SSCK clock phase Selects edge of data change and data download

Note:
1. Synchronous serial communication unit has only one interrupt vector table.

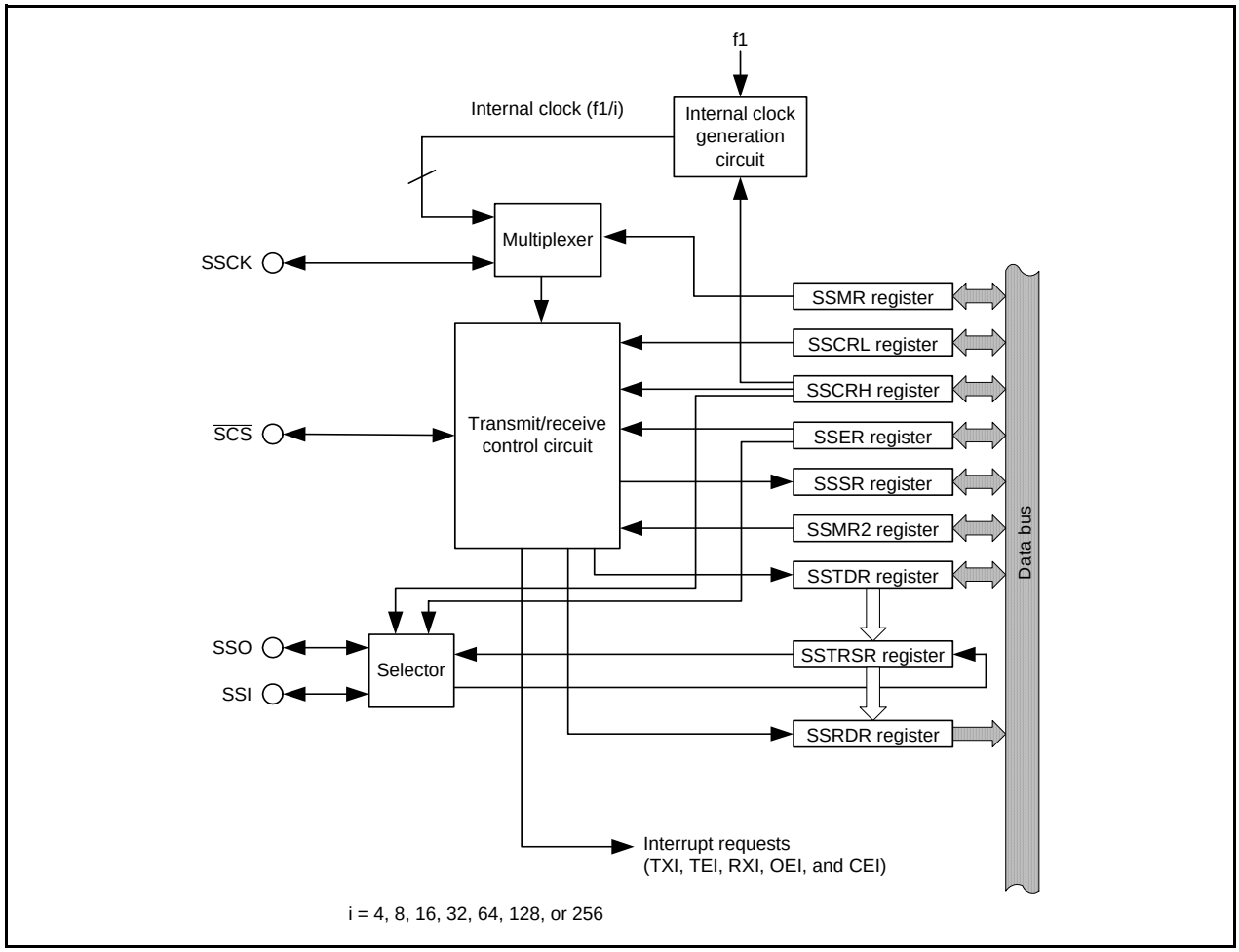


Figure 23.1 Block Diagram of Synchronous Serial Communication Unit

Table 23.2 Pin Configuration of Synchronous Serial Communication Unit

Pin Name	Assigned Pin	I/O	Function
SSI	P3_4	I/O	Data I/O pin
$\overline{\text{SCS}}$	P3_3	I/O	Chip-select signal I/O pin
SSCK	P3_5	I/O	Clock I/O pin
SSO	P3_7	I/O	Data I/O pin

23.2 Registers

23.2.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRC	—	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (2)	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. Stop the SSU and the I2C bus functions before setting to standby. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. Stop the timer RC function before setting to standby. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0132h) is disabled.

23.2.2 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I2C bus switch bit	0: SSU function selected 1: I2C bus function selected	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

23.2.3 SS Bit Counter Register (SSBR)

Address 0193h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	BS3	BS2	BS1	BS0
After Reset	1	1	1	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BS0	SSU data transfer length set bit (1)	b3 b2 b1 b0 0 0 0 0: 16 bits 1 0 0 0: 8 bits 1 0 0 1: 9 bits 1 0 1 0: 10 bits 1 0 1 1: 11 bits 1 1 0 0: 12 bits 1 1 0 1: 13 bits 1 1 1 0: 14 bits 1 1 1 1: 15 bits	R/W
b1	BS1			R/W
b2	BS2			R/W
b3	BS3			R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—			
b6	—			
b7	—			

Note:
1. Do not write to bits BS0 to BS3 during SSU operation.

To set the SSBR register, set the RE bit in the SSER register to 0 (reception disabled) and the TE bit to 0 (transmission disabled).

Bits BS0 to BS3 (SSU Data Transfer Length Set Bit)

As the SSU data transfer length, 8 to 16 bits can be used.

23.2.4 SS Transmit Data Register (SSTDR)

Address 0195h to 0194h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
b15 to b0	—	Store the transmit data. (1) The stored transmit data is transferred to the SSTRSR register and transmission is started when it is detected that the SSTRSR register is empty. When the next transmit data is written to the SSTDR register during the data transmission from the SSTRSR register, the data can be transmitted continuously. When the MLS bit in the SSMR register is set to 1 (transfer data with LSB-first), the data in which MSB and LSB are reversed is read, after writing to the SSTDR register.	R/W

Note:
1. When the SSU data transfer length is set to 9 bits or more with the SSBR register, access the SSTDR register in 16-bit units.

23.2.5 SS Receive Data Register (SSRDR)

Address 0197h to 0196h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Symbol	Function	R/W
b15 to b0	—	Store the receive data. (1, 2) The receive data is transferred to the SSRDR register and the receive operation is completed when 1 byte of data has been received by the SSTRSR register. At this time, the next receive operation is possible. Continuous reception is possible using registers SSTRSR and SSRDR.	R

Notes:
1. The SSRDR register retains the data received before an overrun error occurs (ORER bit in the SSSR register set to 1 (overrun error)). When an overrun error occurs, the receive data may contain errors and therefore should be discarded.
2. When the SSU data transfer length is set to 9 bits or more with the SSBR register, access the SSRDR register in 16-bit units.

23.2.6 SS Control Register H (SSCRH)

Address 0198h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RSSTP	MSS	—	—	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transfer clock select bit (1)	b2 b1 b0 0 0 0: f1/256 0 0 1: f1/128 0 1 0: f1/64 0 1 1: f1/32 1 0 0: f1/16 1 0 1: f1/8 1 1 0: f1/4 1 1 1: Do not set.	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	MSS	Master/slave device select bit (2)	0: Operates as slave device 1: Operates as master device	R/W
b6	RSSTP	Receive single stop bit (3)	0: Maintains receive operation after receiving 1 byte of data 1: Completes receive operation after receiving 1 byte of data	R/W
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. The set clock is used when the MSS bit is set to 1 (operates as master device).
2. The SSCK pin functions as the transfer clock output pin when the MSS bit is set to 1 (operates as master device). The MSS bit is set to 0 (operates as slave device) when the CE bit in the SSSR register is set to 1 (conflict error occurs).
3. The RSSTP bit is disabled when the MSS bit is set to 0 (operates as slave device).

23.2.7 SS Control Register L (SSCRL)

Address 0199h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	SOL	SOLP	—	—	SRES	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	SRES	SSU control unit reset bit	Writing 1 to this bit resets the SSU control unit and the SSTRSR register. The value in the SSU internal register (1) is retained.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b3	—			
b4	SOLP	SOL write protect bit (2)	The output level can be changed by the SOL bit when this bit is set to 0. The SOLP bit remains unchanged even if 1 is written to it. When read, the content is 1.	R/W
b5	SOL	Serial data output value setting bit	When read 0: The serial data output is set to “L”. 1: The serial data output is set to “H”. When written (2, 3) 0: The data output is “L”. 1: The data output is “H”.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Notes:
1. Registers SSBR, SSCRH, SSCRL, SSMR, SSER, SSSR, SSMR2, SSTDR, and SSRDR.
2. For the data output after serial data transmission, the last bit value of the transmitted serial data is retained. If the content of the SOL bit is rewritten before or after serial data transmission, the change is immediately reflected in the data output. When writing to the SOL bit, set the SOLP bit to 0 and the SOL bit to 0 or 1 simultaneously by the MOV instruction.
3. Do not write to the SOL bit during data transfer.

23.2.8 SS Mode Register (SSMR)

Address 019Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	CPOS	CPHS	—	BC3	BC2	BC1	BC0
After Reset	0	0	0	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bits counter 3 to 0	b3 b2 b1 b0 0 0 0 0: 16 bits left 0 0 0 1: 1 bit left 0 0 1 0: 2 bits left 0 0 1 1: 3 bits left 0 1 0 0: 4 bits left 0 1 0 1: 5 bits left 0 1 1 0: 6 bits left 0 1 1 1: 7 bits left 1 0 0 0: 8 bits left 1 0 0 1: 9 bits left 1 0 1 0: 10 bits left 1 0 1 1: 11 bits left 1 1 0 0: 12 bits left 1 1 0 1: 13 bits left 1 1 1 0: 14 bits left 1 1 1 1: 15 bits left	R
b1	BC1			R
b2	BC2			R
b3	BC3			R
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	CPHS	SSCK clock phase select bit (1)	0: Change data at odd edge (Download data at even edge) 1: Change data at even edge (Download data at odd edge)	R/W
b6	CPOS	SSCK clock polarity select bit (1)	0: “H” when clock stops 1: “L” when clock stops	R/W
b7	MLS	MSB first/LSB first select bit	0: Transfers data MSB first 1: Transfers data LSB first	R/W

Note:

1. Refer to **23.3.1.1 Association between Transfer Clock Polarity, Phase, and Data** for the settings of the CPHS and CPOS bits.
   When the SSUMS bit in the SSMR2 register is set to 0 (clock synchronous communication mode), set the CPHS bit to 0 and the CPOS bit to 0.

23.2.9 SS Enable Register (SSER)

Address 019Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	TE	RE	—	—	CEIE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CEIE	Conflict error interrupt enable bit	0: Disables conflict error interrupt request 1: Enables conflict error interrupt request	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	RE	Receive enable bit	0: Disables receive 1: Enables receive	R/W
b4	TE	Transmit enable bit	0: Disables transmit 1: Enables transmit	R/W
b5	RIE	Receive interrupt enable bit	0: Disables receive data full and overrun error interrupt request 1: Enables receive data full and overrun error interrupt request	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Disables transmit end interrupt request 1: Enables transmit end interrupt request	R/W
b7	TIE	Transmit interrupt enable bit	0: Disables transmit data empty interrupt request 1: Enables transmit data empty interrupt request	R/W

23.2.10 SS Status Register (SSSR)

Address 019Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	—	—	ORER	—	CE
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CE	Conflict error flag (1)	0: No conflict errors generated 1: Conflict errors generated (2)	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	ORER	Overrun error flag (1)	0: No overrun errors generated 1: Overrun errors generated (3)	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	RDRF	Receive data register full flag (1, 4)	0: No data in SSRDR register 1: Data in SSRDR register	R/W
b6	TEND	Transmit end flag (1, 5)	0: The TDRE bit is set to 0 when transmitting the last bit of transmit data 1: The TDRE bit is set to 1 when transmitting the last bit of transmit data	R/W
b7	TDRE	Transmit data empty flag (1, 5, 6)	0: Data is not transferred from registers SSTDR to SSTRSR 1: Data is transferred from registers SSTDR to SSTRSR	R/W

Notes:

1. Writing 1 to CE, ORER, RDRF, TEND, or TDRE bits is invalid. To set any of these bits to 0, first read 1 then write 0.
2. When the serial communication is started while the SSUMS bit in the SSMR2 register is set to 1 (four-wire bus communication mode) and the MSS bit in the SSCRH register is set to 1 (operates as master device), the CE bit is set to 1 if “L” is applied to the $\overline{\text{SCS}}$ pin input. Refer to **23.5.4 SCS Pin Control and Arbitration** for more information.
   When the SSUMS bit in the SSMR2 register is set to 1 (four-wire bus communication mode), the MSS bit in the SSCRH register is set to 0 (operates as slave device) and the $\overline{\text{SCS}}$ pin input changes the level from “L” to “H” during transfer, the CE bit is set to 1.
3. Indicates when overrun errors occur and receive completes by error reception. If the next serial data receive operation is completed while the RDRF bit is set to 1 (data in the SSRDR register), the ORER bit is set to 1.
   After the ORER bit is set to 1 (overrun error), receive operation is disabled while the bit remains 1.
4. The RDRF bit is set to 0 when reading out the data from the SSRDR register.
5. Bits TEND and TDRE are set to 0 when writing data to the SSTDR register.
   When reading these bits immediately after writing to the SSTDR register, insert three or more NOP instructions between the instructions used for writing and reading.
6. The TDRE bit is set to 1 when the TE bit in the SSER register is set to 1 (transmit enabled).

If the SSSR register is accessed continuously, insert one or more NOP instructions between the instructions used for access.

23.2.11 SS Mode Register 2 (SSMR2)

Address 019Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BIDE	SCKS	CSS1	CSS0	SCKOS	SOOS	CSOS	SSUMS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	SSUMS	SSU mode select bit (1)	0: Clock synchronous communication mode 1: Four-wire bus communication mode	R/W
b1	CSOS	$\overline{SCS}$ pin open drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b2	SOOS	Serial data pin open drain output select bit (1)	0: CMOS output (5) 1: N-channel open-drain output	R/W
b3	SCKOS	SSCK pin open drain output select bit	0: CMOS output 1: N-channel open-drain output	R/W
b4	CSS0	$\overline{SCS}$ pin select bit (2)	b5 b4 0 0: Functions as port 0 1: Functions as $\overline{SCS}$ input pin 1 0: Functions as $\overline{SCS}$ output pin (3) 1 1: Functions as $\overline{SCS}$ output pin (3)	R/W
b5	CSS1			R/W
b6	SCKS	SSCK pin select bit	0: Functions as port 1: Functions as serial clock pin	R/W
b7	BIDE	Bidirectional mode enable bit (1, 4)	0: Standard mode (communication using 2 pins of data input and data output) 1: Bidirectional mode (communication using 1 pin of data input and data output)	R/W

Notes:
1. Refer to **23.3.2.1 Association between Data I/O Pins and SS Shift Register** for information on combinations of data I/O pins.
2. The $\overline{SCS}$ pin functions as a port, regardless of the values of bits CSS0 and CSS1 when the SSUMS bit is set to 0 (clock synchronous communication mode).
3. This bit functions as the $\overline{SCS}$ input pin before starting transfer.
4. The BIDE bit is disabled when the SSUMS bit is set to 0 (clock synchronous communication mode).
5. When the SOOS bit is set to 0 (CMOS output), set the port direction register bits corresponding to pins SSI and SSO to 0 (input mode).

23.3 Common Items for Multiple Modes

23.3.1 Transfer Clock

The transfer clock can be selected from among seven internal clocks (f1/256, f1/128, f1/64, f1/32, f1/16, f1/8, and f1/4) and an external clock.
When using synchronous serial communication unit, set the SCKS bit in the SSMR2 register to 1 and select the SSCK pin as the serial clock pin.
When the MSS bit in the SSCRH register is set to 1 (operates as master device), an internal clock can be selected and the SSCK pin functions as output. When transfer is started, the SSCK pin outputs clocks of the transfer rate selected by bits CKS0 to CKS2 in the SSCRH register.
When the MSS bit in the SSCRH register is set to 0 (operates as slave device), an external clock can be selected and the SSCK pin functions as input.

23.3.1.1 Association between Transfer Clock Polarity, Phase, and Data

The association between the transfer clock polarity, phase and data changes according to the combination of the SSUMS bit in the SSMR2 register and bits CPHS and CPOS in the SSMR register. Figure 23.2 shows the Association between Transfer Clock Polarity, Phase, and Transfer Data.
Also, the MSB-first transfer or LSB-first transfer can be selected by setting the MLS bit in the SSMR register. When the MLS bit is set to 1, transfer is started from the LSB and proceeds to the MSB. When the MLS bit is set to 0, transfer is started from the MSB and proceeds to the LSB.

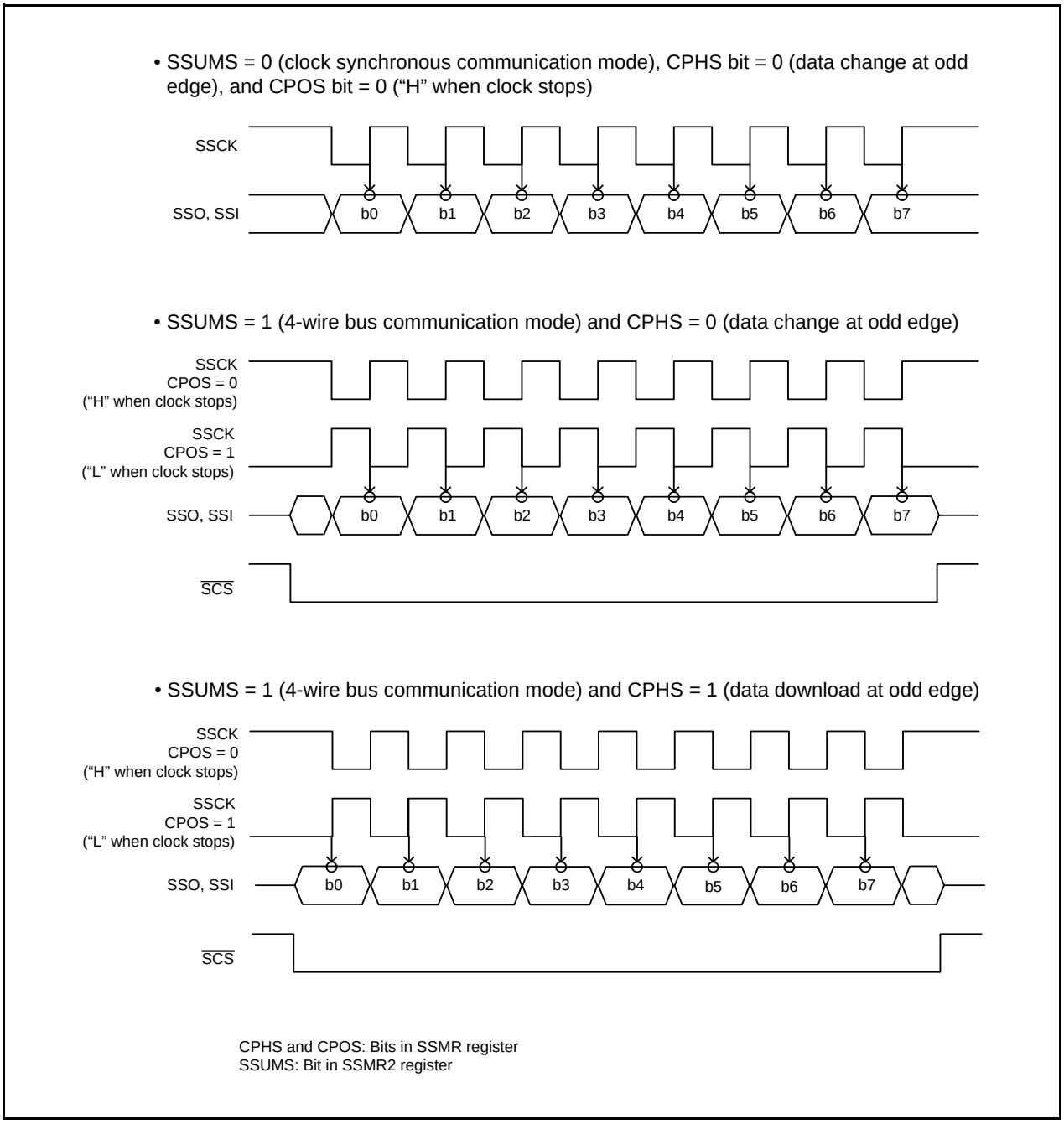


Figure 23.2 Association between Transfer Clock Polarity, Phase, and Transfer Data

23.3.2 SS Shift Register (SSTRSR)

The SSTRSR register is a shift register for transmitting and receiving serial data.
When transmit data is transferred from the SSTDR register to the SSTRSR register and the MLS bit in the SSMR register is set to 0 (MSB-first), the bit 0 in the SSTDR register is transferred to bit 0 in the SSTRSR register. When the MLS bit is set to 1 (LSB-first), bit 7 in the SSTDR register is transferred to bit 0 in the SSTRSR register.

23.3.2.1 Association between Data I/O Pins and SS Shift Register

The connection between the data I/O pins and SSTRSR register (SS shift register) changes according to a combination of the MSS bit in the SSCRH register and the SSUMS bit in the SSMR2 register. The connection also changes according to the BIDE bit in the SSMR2 register. Figure 23.3 shows the Association between Data I/O Pins and SSTRSR Register.

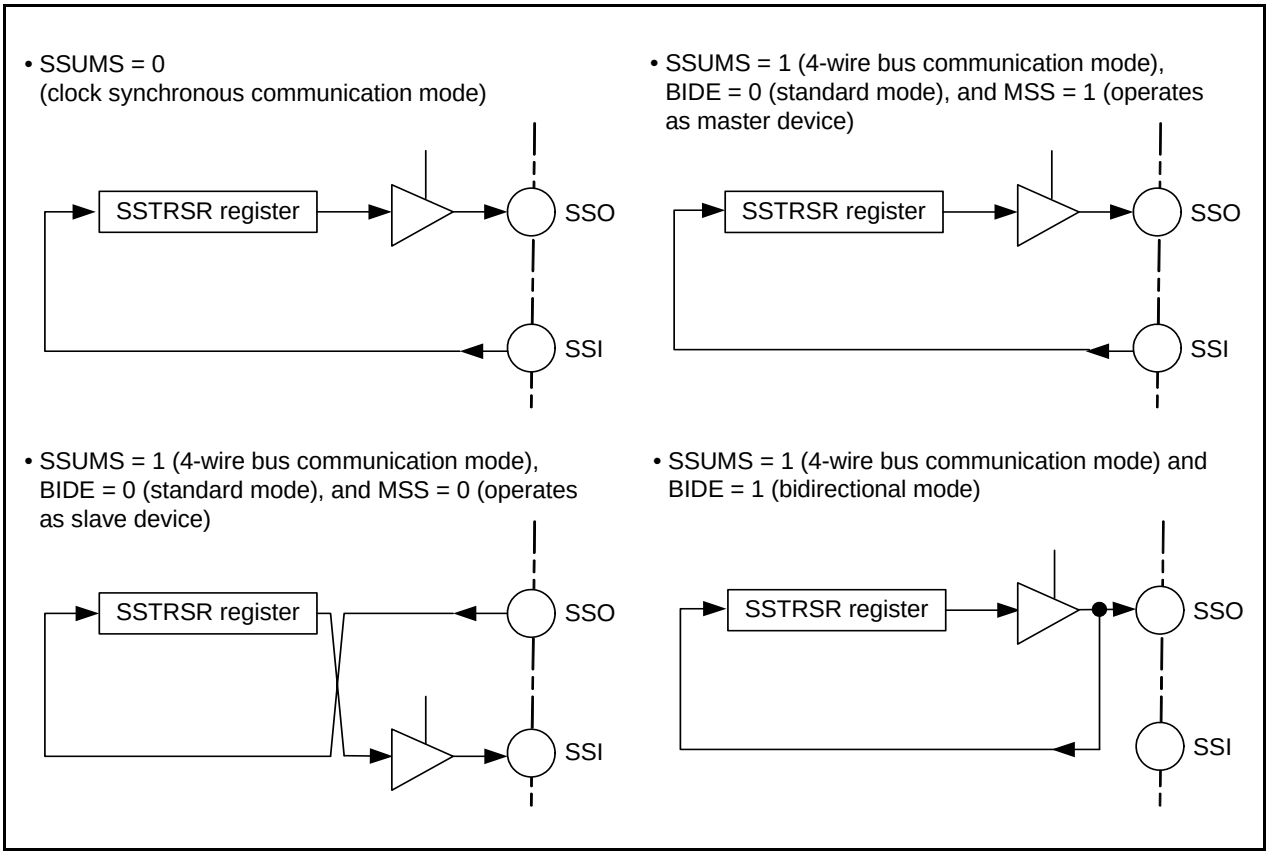


Figure 23.3 Association between Data I/O Pins and SSTRSR Register

23.3.3 Interrupt Requests

Synchronous serial communication unit has five interrupt requests: transmit data empty, transmit end, receive data full, overrun error, and conflict error. Since these interrupt requests are assigned to the synchronous serial communication unit interrupt vector table, determining interrupt sources by flags is required. Table 23.3 shows the Synchronous Serial Communication Unit Interrupt Requests.

Table 23.3 Synchronous Serial Communication Unit Interrupt Requests

Interrupt Request	Abbreviation	Generation Condition
Transmit data empty	TXI	TIE = 1, TDRE = 1
Transmit end	TEI	TEIE = 1, TEND = 1
Receive data full	RXI	RIE = 1, RDRF = 1
Overrun error	OEI	RIE = 1, ORER = 1
Conflict error	CEI	CEIE = 1, CE = 1

CEIE, RIE, TEIE and TIE: Bits in SSER register
ORER, RDRF, TEND and TDRE: Bits in SSSR register

If the generation conditions in Table 23.3 are met, a synchronous serial communication unit interrupt request is generated. Set each interrupt source to 0 by a synchronous serial communication unit interrupt routine.

However, the TDRE and TEND bits are automatically set to 0 by writing transmit data to the SSTDR register and the RDRF bit is automatically set to 0 by reading the SSRDR register. In particular, the TDRE bit is set to 1 (data transmitted from registers SSTDR to SSTRSR) at the same time transmit data is written to the SSTDR register. Setting the TDRE bit to 0 (data not transmitted from registers SSTDR to SSTRSR) can cause an additional byte of data to be transmitted.

23.3.4 Communication Modes and Pin Functions

Synchronous serial communication unit switches the functions of the I/O pins in each communication mode according to the setting of the MSS bit in the SSCRH register and bits RE and TE in the SSER register. Table 23.4 shows the Association between Communication Modes and I/O Pins.

Table 23.4 Association between Communication Modes and I/O Pins

Communication Mode	Bit Setting					Pin State		
	SSUMS	BIDE	MSS	TE	RE	SSI	SSO	SSCK
Clock synchronous communication mode	0	Disabled	0	0	1	Input	— (1)	Input
				1	0	— (1)	Output	Input
					1	Input	Output	Input
			1	0	1	Input	— (1)	Output
				1	0	— (1)	Output	Output
					1	Input	Output	Output
4-wire bus communication mode	1	0	0	0	1	— (1)	Input	Input
				1	0	Output	— (1)	Input
					1	Output	Input	Input
			1	0	1	Input	— (1)	Output
				1	0	— (1)	Output	Output
					1	Input	Output	Output
4-wire bus (bidirectional) communication mode (2)	1	1	0	0	1	— (1)	Input	Input
				1	0	— (1)	Output	Input
			1	0	1	— (1)	Input	Output
				1	0	— (1)	Output	Output

Notes:
1. This pin can be used as a programmable I/O port.
2. Do not set both bits TE and RE to 1 in 4-wire bus (bidirectional) communication mode.

SSUMS and BIDE: Bits in SSMR2 register
MSS: Bit in SSCRH register
TE and RE: Bits in SSER register

23.4 Clock Synchronous Communication Mode

23.4.1 Initialization in Clock Synchronous Communication Mode

Figure 23.4 shows Initialization in Clock Synchronous Communication Mode. To initialize, set the TE bit in the SSER register to 0 (transmit disabled) and the RE bit to 0 (receive disabled) before data transmission or reception.
Set the TE bit to 0 and the RE bit to 0 before changing the communication mode or format.
Setting the RE bit to 0 does not change the contents of flags RDRF and ORER or the contents of the SSRDR register.

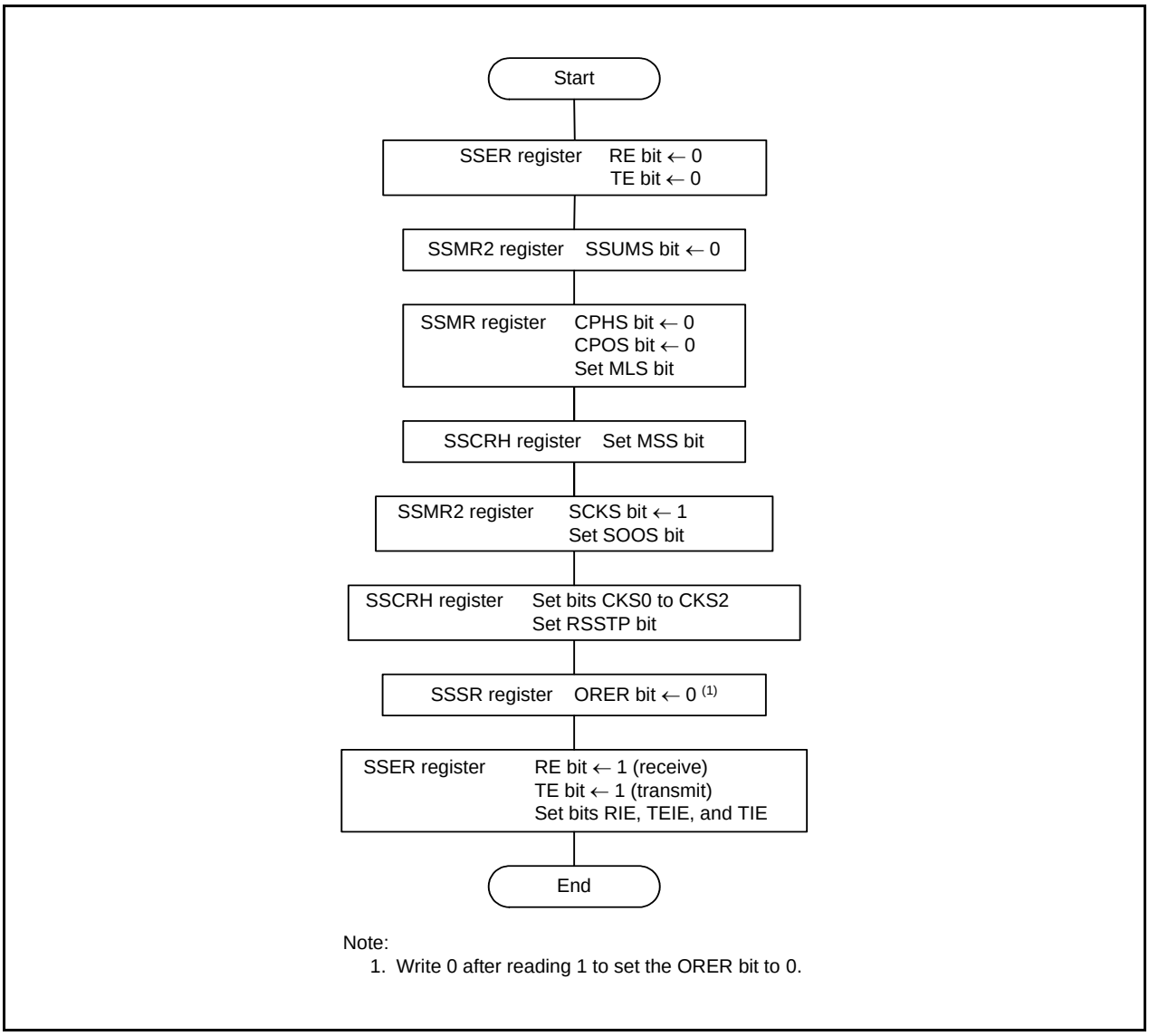


Figure 23.4 Initialization in Clock Synchronous Communication Mode

23.4.2 Data Transmission

Figure 23.5 shows an Example of Synchronous Serial Communication Unit Operation for Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data transmission, the synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)

When synchronous serial communication unit is set as a master device, it outputs a synchronous clock and data. When synchronous serial communication unit is set as a slave device, it outputs data synchronized with the input clock.

When the TE bit is set to 1 (transmit enabled) before writing the transmit data to the SSTDR register, the TDRE bit is automatically set to 0 (data not transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR.

After the TDRE bit is set to 1 (data transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1, the TXI interrupt request is generated. When one frame of data is transferred while the TDRE bit is set to 0, data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while the TDRE bit is set to 1, the TEND bit in the SSSR register is set to 1 (the TDRE bit is set to 1 when the last bit of the transmit data is transmitted) and the state is retained. The TEI interrupt request is generated when the TEIE bit in the SSER register is set to 1 (transmit-end interrupt request enabled). The SSCK pin is fixed “H” after transmit-end.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

Figure 23.6 shows a Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode).

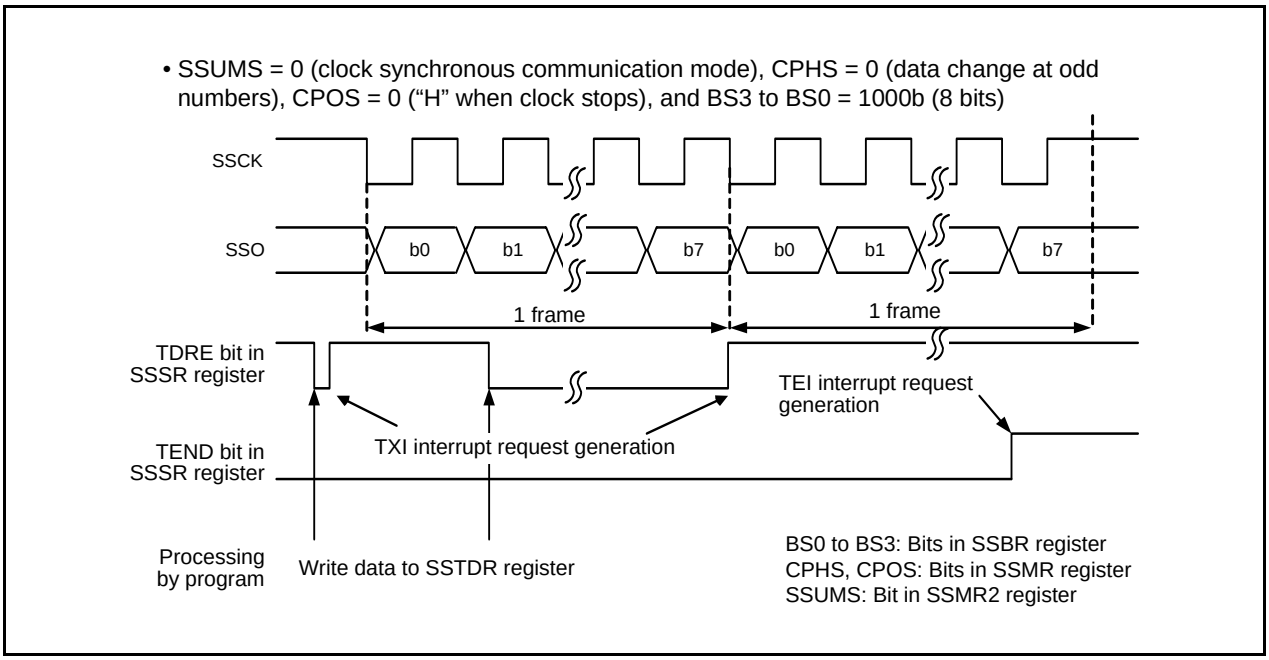


Figure 23.5 Example of Synchronous Serial Communication Unit Operation for Data Transmission (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)

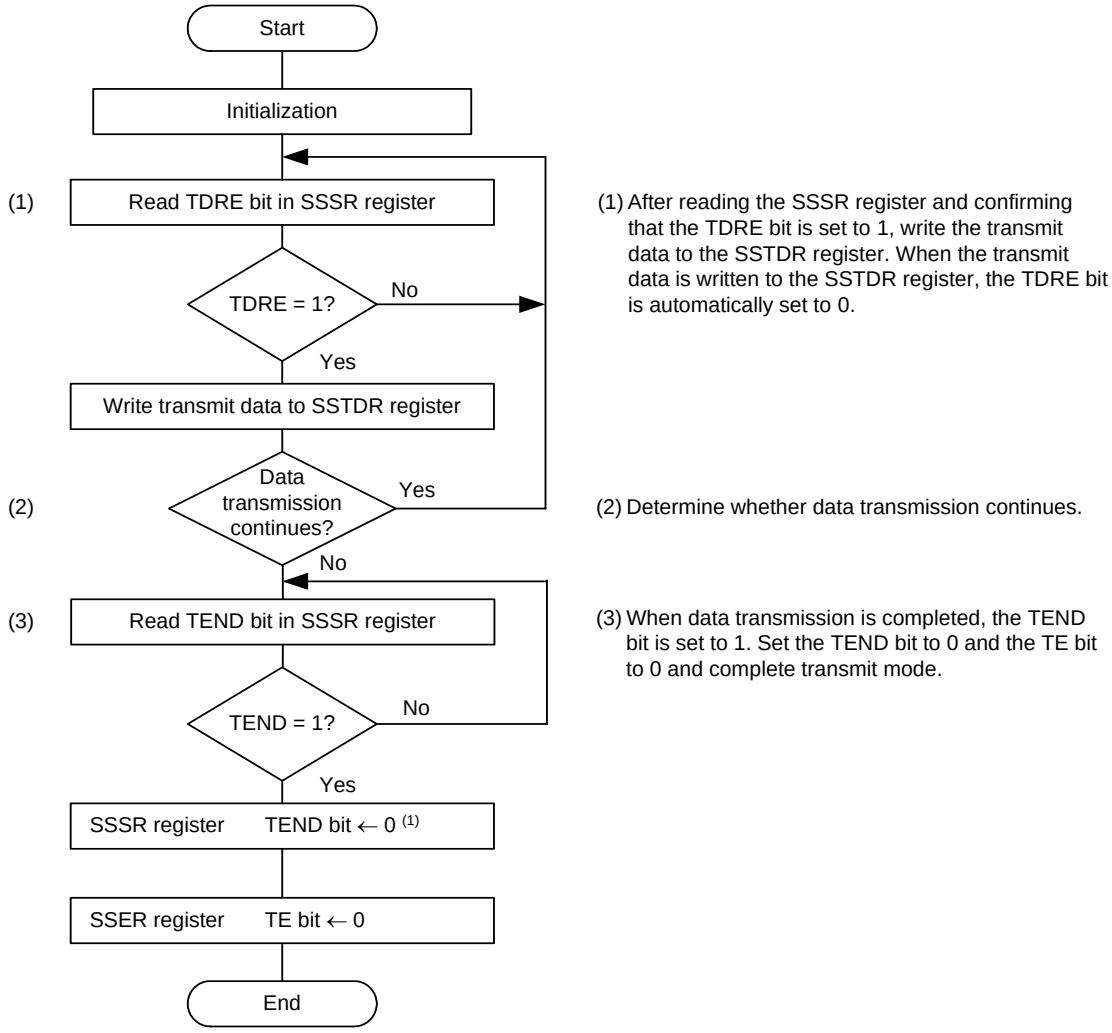


Figure 23.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)

23.4.3 Data Reception

Figure 23.7 shows an Example of Synchronous Serial Communication Unit Operation for Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and inputs data. When synchronous serial communication unit is set as a slave device, it inputs data synchronized with the input clock.

When synchronous serial communication unit is set as a master device, it outputs a receive clock and starts receiving by performing dummy read of the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled), the RXI interrupt request is generated. If the SSRDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

When the synchronous serial communication unit operates as a master device and finish the data reception, read the receive data after setting the RSSTP bit in the SSCRH register to 1 (after receiving 1 byte of data, the receive operation is completed). Synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (receive disabled) and the RSSTP bit to 0 (receive operation is continued after receiving the 1 byte of data) and read the receive data. If the SSRDR register is read while the RE bit is set to 1 (receive enabled), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, receive cannot be performed. Confirm that the ORER bit is set to 0 before restarting receive.

Figure 23.8 shows a Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode).

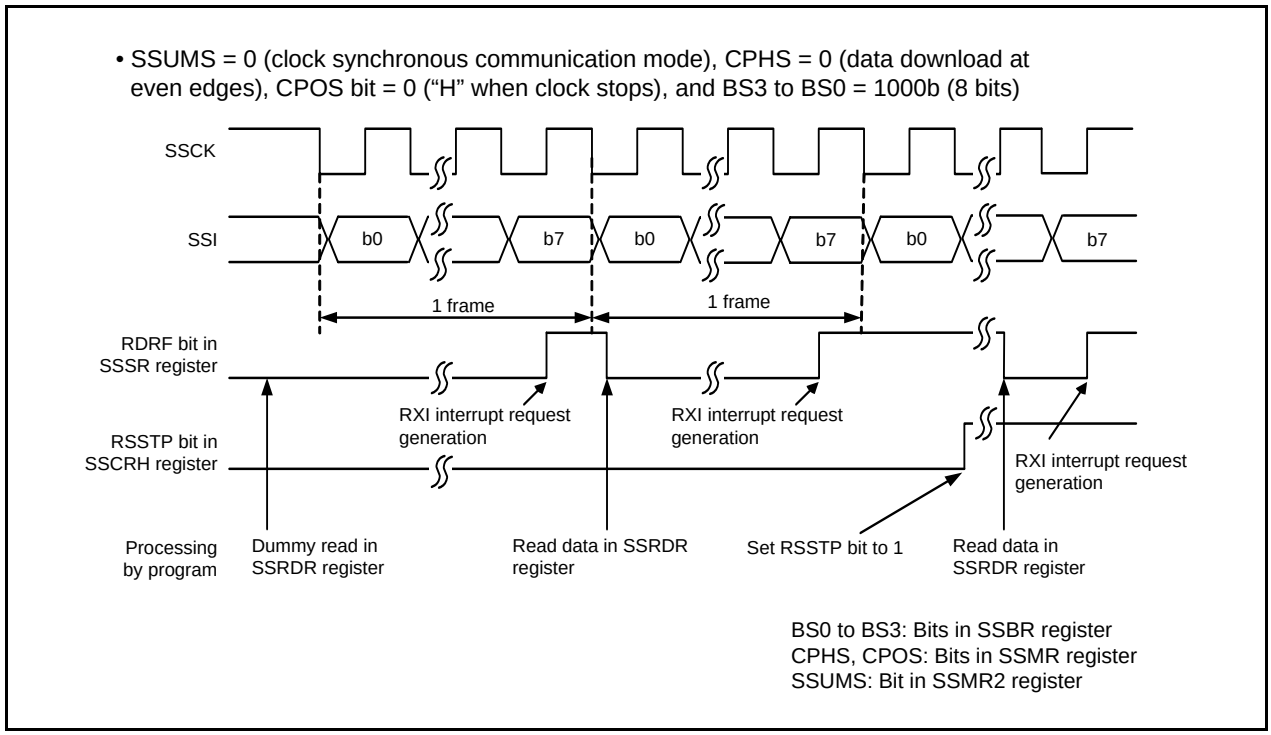


Figure 23.7 Example of Synchronous Serial Communication Unit Operation for Data Reception (Clock Synchronous Communication Mode, 8-Bit SSU Data Transfer Length)

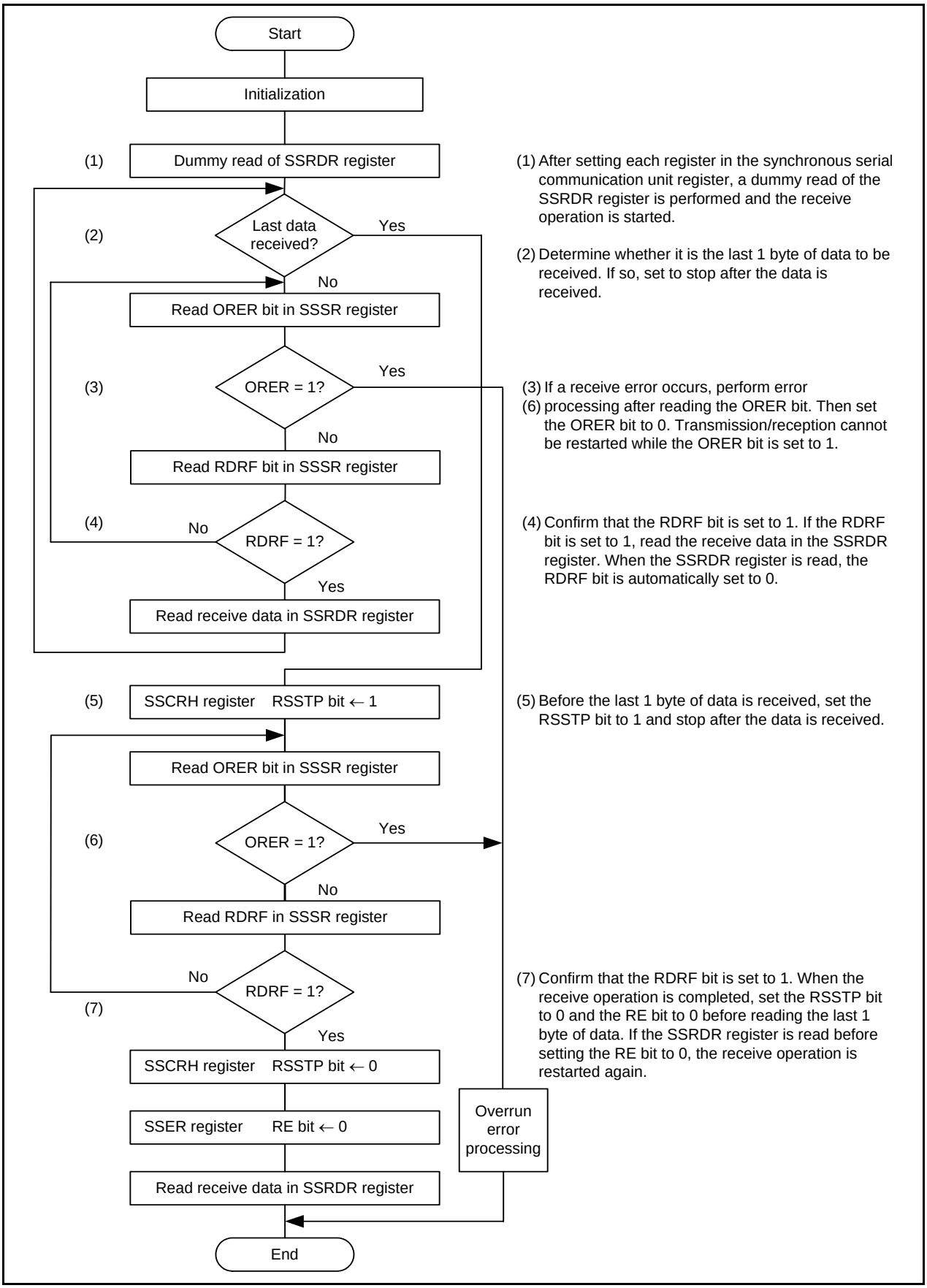


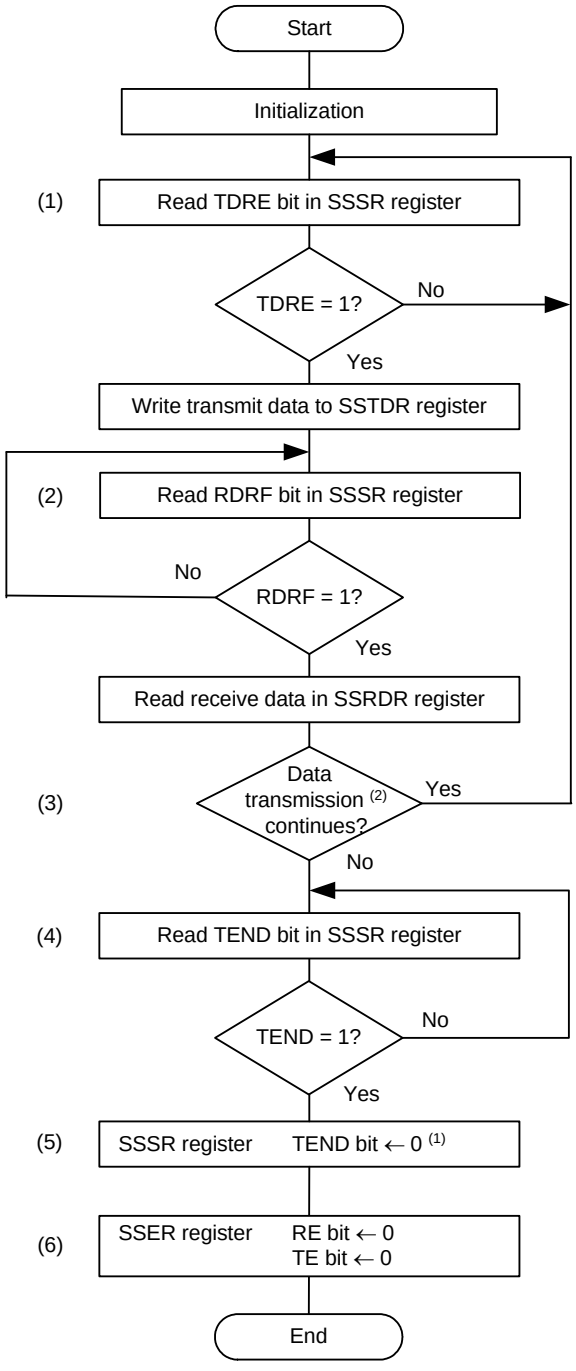
Figure 23.8 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)

23.4.3.1 Data Transmission/Reception

Data transmission/reception is an operation combining data transmission and reception which were described earlier. Transmission/reception is started by writing data to the SSTDR register.
When the last transfer clock (the data transfer length can be set from 8 to 16 bits using the SSBR register) rises or the ORER bit is set to 1 (overrun error) while the TDRE bit is set to 1 (data is transferred from registers SSTDR to SSTRSR), the transmit/receive operation is stopped.
When switching from transmit mode (TE = 1) or receive mode (RE = 1) to transmit/receive mode (TE = RE = 1), set the TE bit to 0 and RE bit to 0 before switching. After confirming that the TEND bit is set to 0 (the TDRE bit is set to 0 when the last bit of the transmit data is transmitted), the RDRF bit is set to 0 (no data in the SSRDR register), and the ORER bit is set to 0 (no overrun error), set bits TE and RE to 1.
Figure 23.9 shows a Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode).
When exiting transmit/receive mode after this mode is used (TE = RE = 1), a clock may be output if transmit/receive mode is exited after reading the SSRDR register. To avoid any clock outputs, perform either of the following:

- First set the RE bit to 0, and then set the TE bit to 0.
- Set bits TE and RE to 0 at the same time.

When subsequently switching to receive mode (TE = 0 and RE = 1), first set the SRES bit to 1, and set this bit to 0 to reset the SSU control unit and the SSTRSR register. Then, set the RE bit to 1.



(1) After reading the SSSR register and confirming that the TDRE bit is set to 1, write the transmit data to the SSTDR register. When the transmit data is written to the SSTDR register, the TDRE bit is automatically set to 0.

(2) Confirm that the RDRF bit is set to 1. If the RDRF bit is set to 1, read the receive data in the SSRDR register. When the SSRDR register is read, the RDRF bit is automatically set to 0.

(3) Determine whether the data transmission continues

(4) When the data transmission is completed, the TEND bit in the SSSR register is set to 1.

(5) Set the TEND bit to 0 and bits RE and TE in
(6) the SSER register to 0 before ending transmit/ receive mode.

Note:
1. Write 0 after reading 1 to set the TEND bit to 0.

Figure 23.9 Sample Flowchart of Data Transmission/Reception (Clock Synchronous Communication Mode)

23.5 Operation in 4-Wire Bus Communication Mode

In 4-wire bus communication mode, a 4-wire bus consisting of a clock line, a data input line, a data output line, and a chip select line is used for communication. This mode includes bidirectional mode in which the data input line and data output line function as a single pin.

The data input line and output line change according to the settings of the MSS bit in the SSCRH register and the BIDE bit in the SSMR2 register. For details, refer to **23.3.2.1 Association between Data I/O Pins and SS Shift Register**. In this mode, clock polarity, phase, and data settings are performed by bits CPOS and CPHS in the SSMR register. For details, refer to **23.3.1.1 Association between Transfer Clock Polarity, Phase, and Data**.

When this MCU is set as the master device, the chip select line controls output. When synchronous serial communication unit is set as a slave device, the chip select line controls input. When it is set as the master device, the chip select line controls output of the $\overline{\text{SCS}}$ pin or controls output of a general port according to the setting of the CSS1 bit in the SSMR2 register. When the MCU is set as a slave device, the chip select line sets the $\overline{\text{SCS}}$ pin as an input pin by setting bits CSS1 and CSS0 in the SSMR2 register to 01b.

In 4-wire bus communication mode, the MLS bit in the SSMR register is set to 0 and communication is performed MSB-first.

23.5.1 Initialization in 4-Wire Bus Communication Mode

Figure 23.10 shows Initialization in 4-Wire Bus Communication Mode. Before the data transmit/receive operation, set the TE bit in the SSER register to 0 (transmit disabled), the RE bit in the SSER register to 0 (receive disabled), and initialize the synchronous serial communication unit.
To change the communication mode or format, set the TE bit to 0 and the RE bit to 0 before making the change. Setting the RE bit to 0 does not change the settings of flags RDRF and ORER or the contents of the SSRDR register.

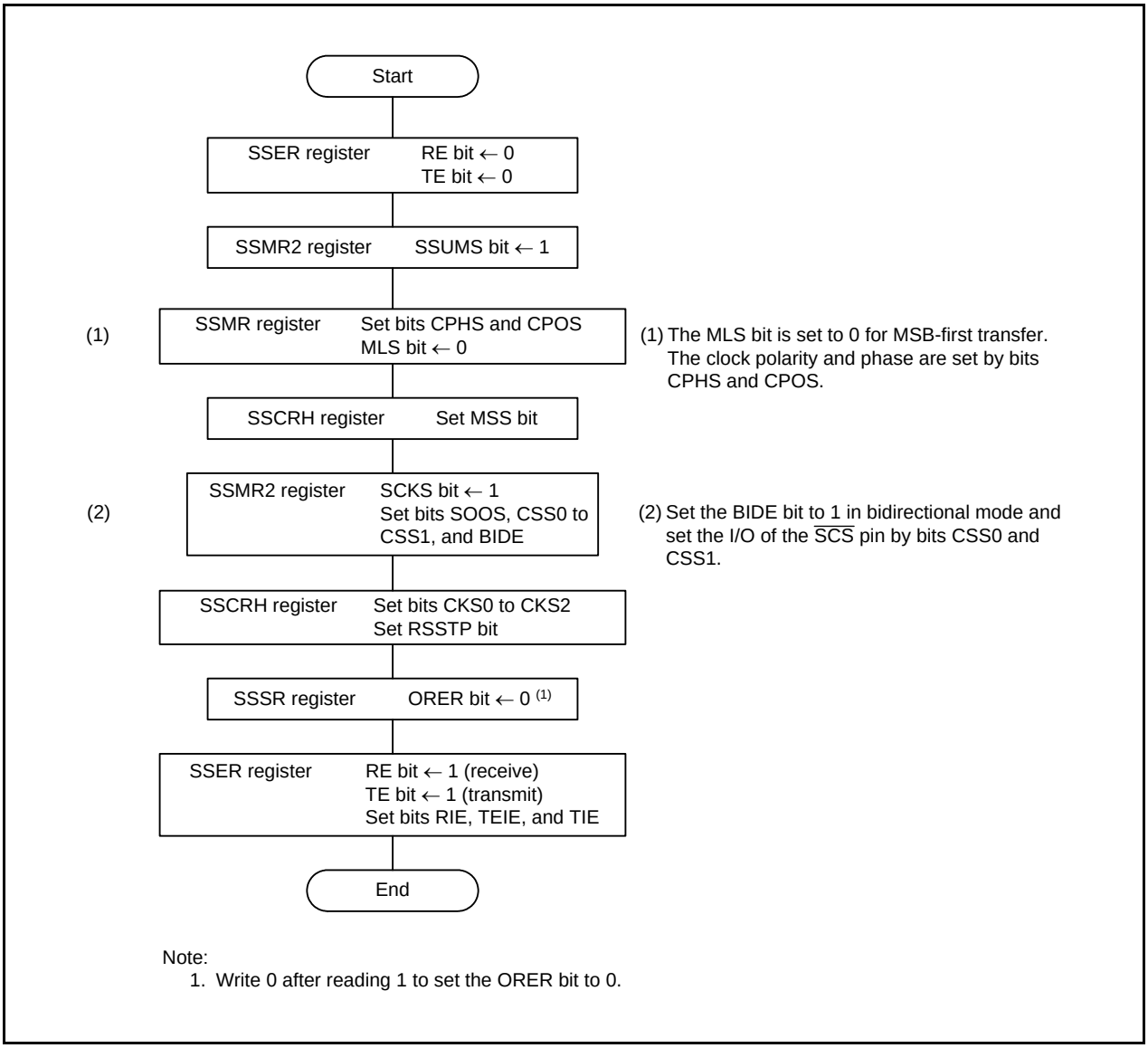


Figure 23.10 Initialization in 4-Wire Bus Communication Mode

23.5.2 Data Transmission

Figure 23.11 shows an Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During the data transmit operation, synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and data. When the synchronous serial communication unit is set as a slave device, it outputs data in synchronization with the input clock while the $\overline{SCS}$ pin is "L".

When the transmit data is written to the SSTDR register after setting the TE bit to 1 (transmit enabled), the TDRE bit is automatically set to 0 (data has not been transferred from registers SSTDR to SSTRSR) and the data is transferred from registers SSTDR to SSTRSR. After the TDRE bit is set to 1 (data is transferred from registers SSTDR to SSTRSR), transmission starts. When the TIE bit in the SSER register is set to 1, a TXI interrupt request is generated.

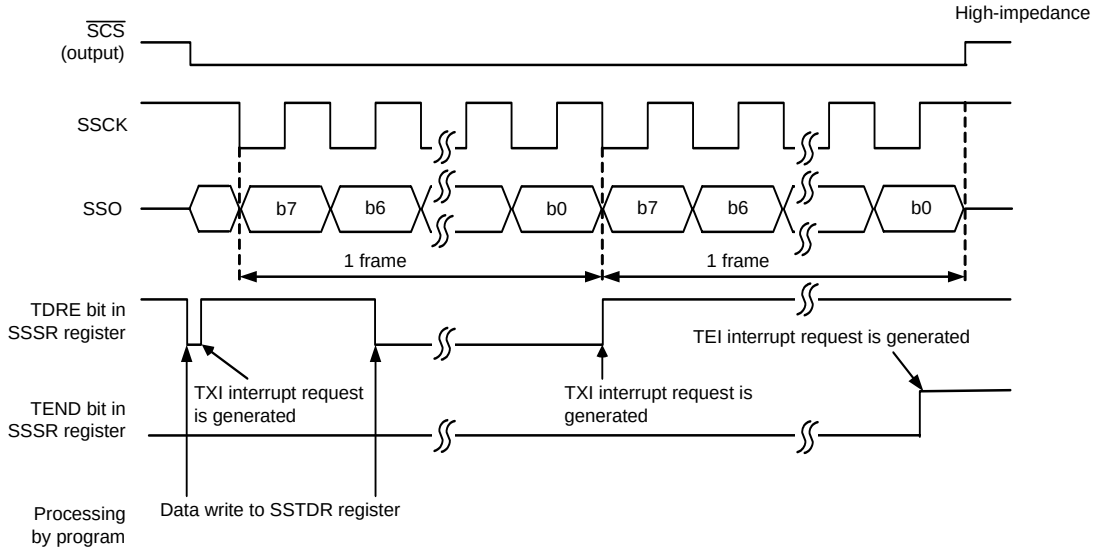
After 1 frame of data is transferred while the TDRE bit is set to 0, the data is transferred from registers SSTDR to SSTRSR and transmission of the next frame is started. If the 8th bit is transmitted while TDRE is set to 1, TEND in the SSSR register is set to 1 (when the last bit of the transmit data is transmitted, the TDRE bit is set to 1) and the state is retained. If the TEIE bit in the SSER register is set to 1 (transmit-end interrupt requests enabled), a TEI interrupt request is generated. The SSCK pin remains "H" after transmit-end and the $\overline{SCS}$ pin is held "H". When transmitting continuously while the $\overline{SCS}$ pin is held "L", write the next transmit data to the SSTDR register before transmitting the 8th bit.

Transmission cannot be performed while the ORER bit in the SSSR register is set to 1 (overrun error). Confirm that the ORER bit is set to 0 before transmission.

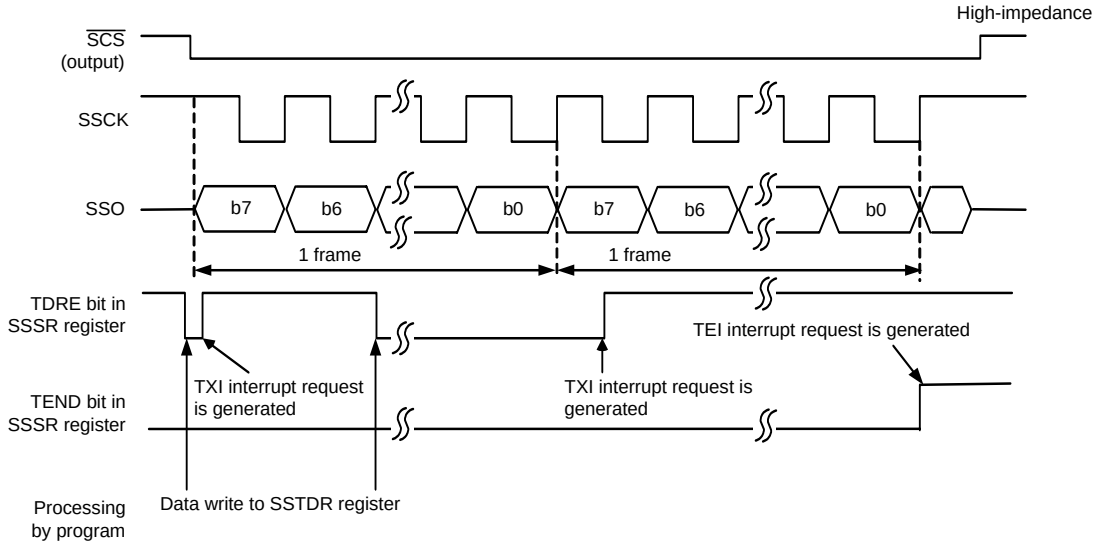
In contrast to the clock synchronous communication mode, the SSO pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in high-impedance state when operating as a master device and the SSI pin is placed in high-impedance state while the $\overline{SCS}$ pin is placed in "H" input state when operating as a slave device.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 23.6 Sample Flowchart of Data Transmission (Clock Synchronous Communication Mode)**).

• CPHS bit = 0 (data change at odd edges), CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



• CPHS bit = 1 (data change at even edges). CPOS bit = 0 (“H” when clock stops), and BS3 to BS0 = 1000b (8 bits)



BS0 to BS3: Bits in SSBR register
CPHS, CPOS: Bits in SSMR register

Figure 23.11 Example of Synchronous Serial Communication Unit Operation during Data Transmission (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

23.5.3 Data Reception

Figure 23.12 shows an Example of Synchronous Serial Communication Unit Operation during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length). During data reception, synchronous serial communication unit operates as described below. (The data transfer length can be set from 8 to 16 bits using the SSBR register.)

When the synchronous serial communication unit is set as the master device, it outputs a synchronous clock and inputs data. When the synchronous serial communication unit is set as a slave device, it outputs data synchronized with the input clock while the $\overline{SCS}$ pin receives "L" input. When the synchronous serial communication unit is set as the master device, it outputs a receive clock and starts receiving by performing a dummy read of the SSRDR register.

After 8 bits of data are received, the RDRF bit in the SSSR register is set to 1 (data in the SSRDR register) and receive data is stored in the SSRDR register. When the RIE bit in the SSER register is set to 1 (RXI and OEI interrupt requests enabled), an RXI interrupt request is generated. When the SSRDR register is read, the RDRF bit is automatically set to 0 (no data in the SSRDR register).

When the synchronous serial communication unit operates as a master device and finish the data reception, read the receive data after setting the RSSTP bit in the SSCRH register to 1 (after receiving 1-byte data, the receive operation is completed). Synchronous serial communication unit outputs a clock for receiving 8 bits of data and stops. After that, set the RE bit in the SSER register to 0 (receive disabled) and the RSSTP bit to 0 (receive operation is continued after receiving 1-byte data) and read the receive data. When the SSRDR register is read while the RE bit is set to 1 (receive enabled), a receive clock is output again.

When the 8th clock rises while the RDRF bit is set to 1, the ORER bit in the SSSR register is set to 1 (overrun error: OEI) and the operation is stopped. When the ORER bit is set to 1, reception cannot be performed. Confirm that the ORER bit is set to 0 before restarting reception.

The timing with which bits RDRF and ORER are set to 1 varies depending on the setting of the CPHS bit in the SSMR register. Figure 23.12 shows when bits RDRF and ORER are set to 1.

When the CPHS bit is set to 1 (data download at the odd edges), bits RDRF and ORER are set to 1 at some point during the frame.

The sample flowchart is the same as that for the clock synchronous communication mode (refer to **Figure 23.8 Sample Flowchart of Data Reception (MSS = 1) (Clock Synchronous Communication Mode)**).

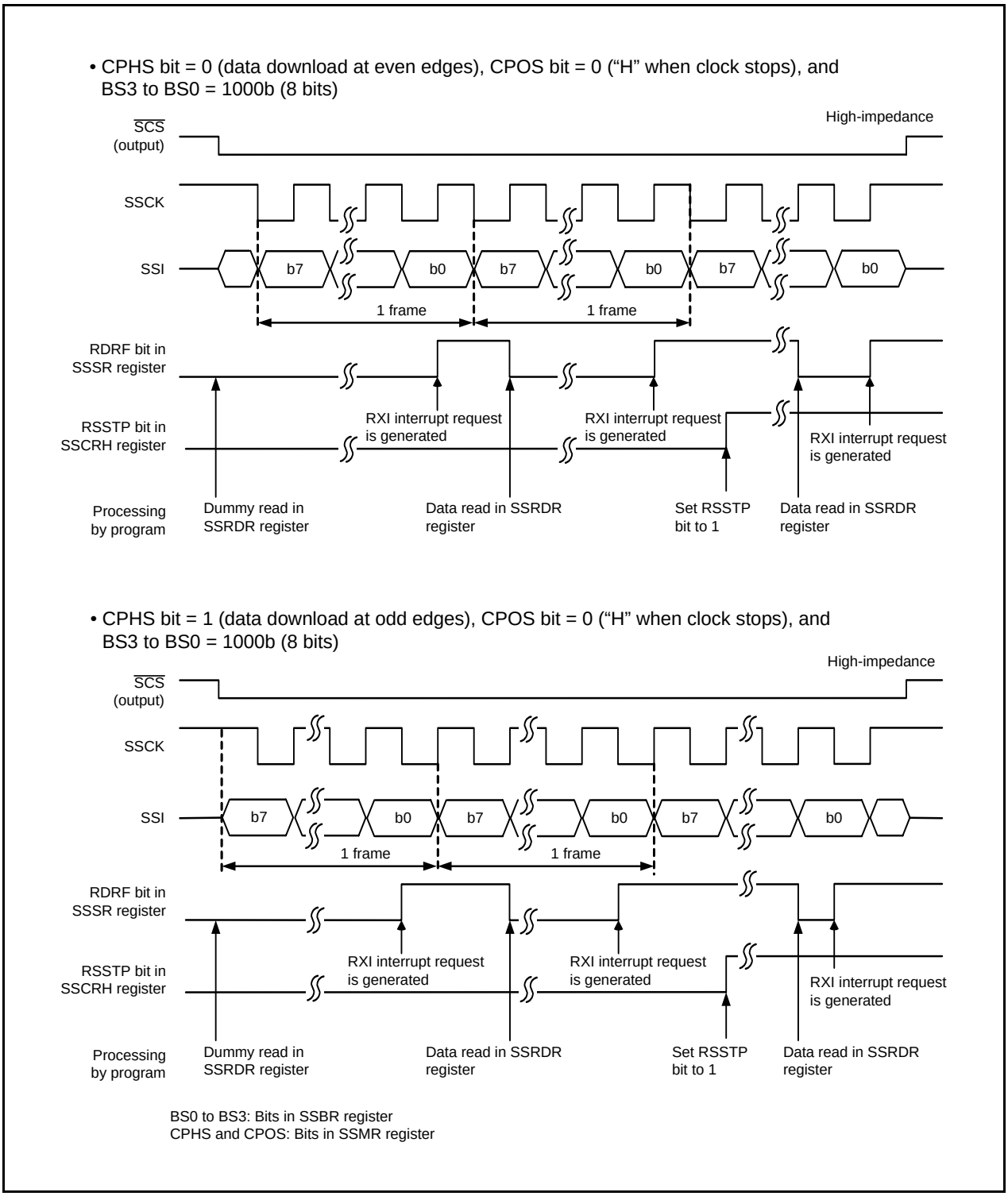


Figure 23.12 Example of Synchronous Serial Communication Unit Operation during Data Reception (4-Wire Bus Communication Mode, 8-Bit SSU Data Transfer Length)

23.5.4 $\overline{\text{SCS}}$ Pin Control and Arbitration

When setting the SSUMS bit in the SSMR2 register to 1 (4-wire bus communication mode) and the CSS1 bit in the SSMR2 register to 1 (functions as $\overline{\text{SCS}}$ output pin), set the MSS bit in the SSCRH register to 1 (operates as the master device) and check the arbitration of the $\overline{\text{SCS}}$ pin before starting serial transfer. If synchronous serial communication unit detects that the synchronized internal $\overline{\text{SCS}}$ signal is held "L" in this period, the CE bit in the SSSR register is set to 1 (conflict error) and the MSS bit is automatically set to 0 (operates as a slave device).
Figure 23.13 shows the Arbitration Check Timing.

Future transmit operations are not performed while the CE bit is set to 1. Set the CE bit to 0 (no conflict error) before starting transmission.

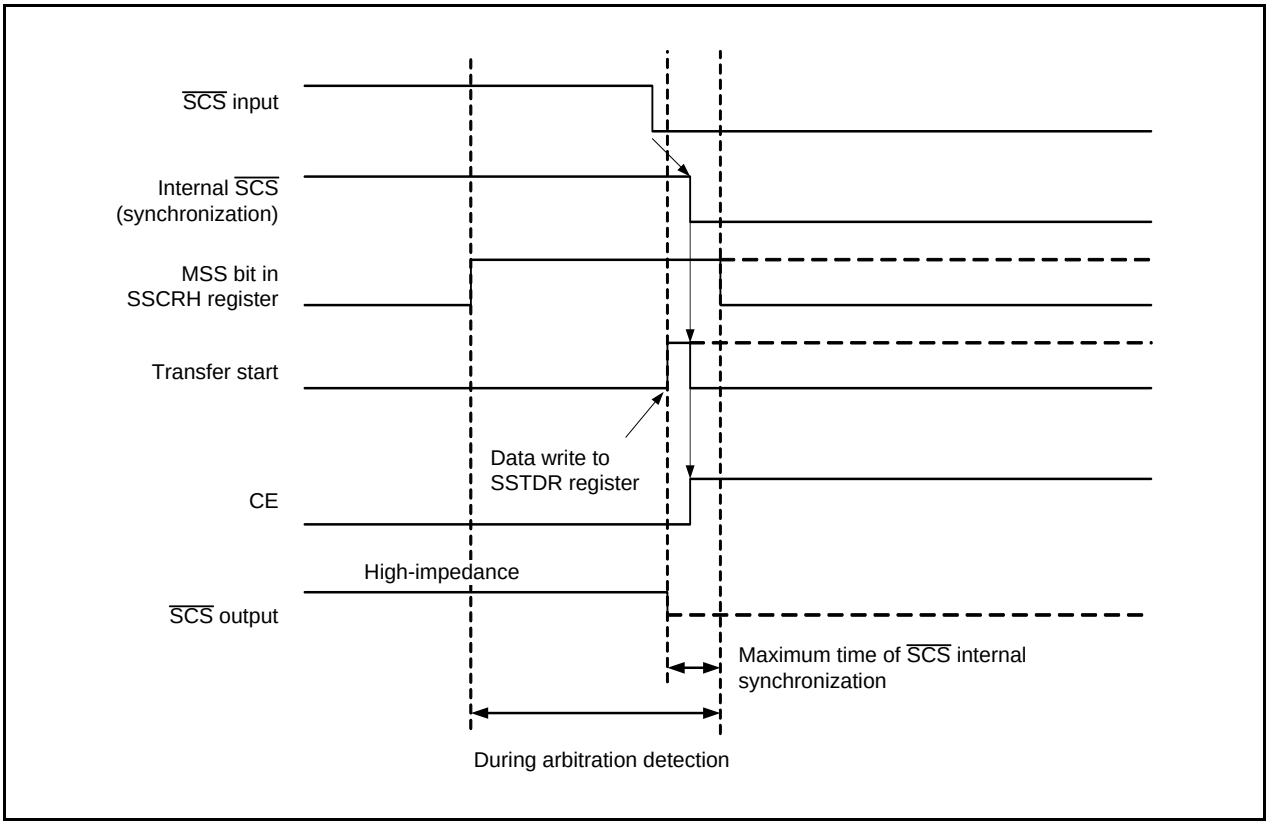


Figure 23.13 Arbitration Check Timing

23.6 Notes on Synchronous Serial Communication Unit

Set the IICSEL bit in the SSUIICSR register to 0 (select SSU function) to use the synchronous serial communication unit function.

24. I2C bus Interface

The I2C bus interface is the circuit that performs serial communication based on the data transfer format of the Philips I2C bus.

24.1 Overview

Table 24.1 lists the I2C bus Interface Specifications, Figure 24.1 shows an I2C bus interface Block Diagram, and Figure 24.2 shows the External Circuit Connection Example of Pins SCL and SDA, Table 24.2 lists the Pin Configuration of I2C bus Interface.

Table 24.1 I2C bus Interface Specifications

Item	Specification
Communication formats	• I2C bus format - Selectable as master/slave device. - Continuous transmit/receive operation (because the shift register, transmit data register, and receive data register are independent.) - Start/stop conditions are automatically generated in master mode. - Automatic loading of the acknowledge bit during transmission - Bit synchronization/wait function (In master mode, the state of the SCL signal is monitored per bit and the timing is synchronized automatically. If the transfer is not possible yet, the SCL signal goes “L” and the interface stands by.) - Support for direct drive of pins SCL and SDA (N-channel open-drain output) • Clock synchronous serial format - Continuous transmit/receive operation (because the shift register, transmit data register, and receive data register are independent.)
I/O pins	SCL (I/O): Serial clock I/O pin SDA (I/O): Serial data I/O pin
Transfer clocks	• When the MST bit in the ICCR1 register is set to 0. External clock (input from the SCL pin) • When the MST bit in the ICCR1 register is set to 1. Internal clock selected by bits CKS0 to CKS3 in the ICCR1 register and bits IICTCTWI and IICTCHALF in the PINSR register (output from the SCL pin)
Receive error detection	• Overrun error detection (clock synchronous serial format) Indicates an overrun error during reception. When the last bit of the next unit of data is received while the RDRF bit in the ICSR register is set to 1 (data in the ICDRR register), the AL bit is set to 1.
Interrupt sources	• I2C bus format ..... 6 sources (1) Transmit data empty (including when slave address matches), end of transmission, receive data full (including when slave address matches), arbitration lost, NACK detection, and stop condition detection • Clock synchronous serial format ..... 4 sources (1) Transmit data empty, end of transmission, receive data full, and overrun error
Selectable functions	• I2C bus format - Selectable output level for the acknowledge signal during reception. • Clock synchronous serial format - MSB-first or LSB-first selectable as the data transfer direction. • SDA digital delay - Digital delay value for the SDA pin selectable by bits SDADLY0 to SDADLY1 in the PINSR register.

Note:
1. All sources use one interrupt vector for I2C bus interface.

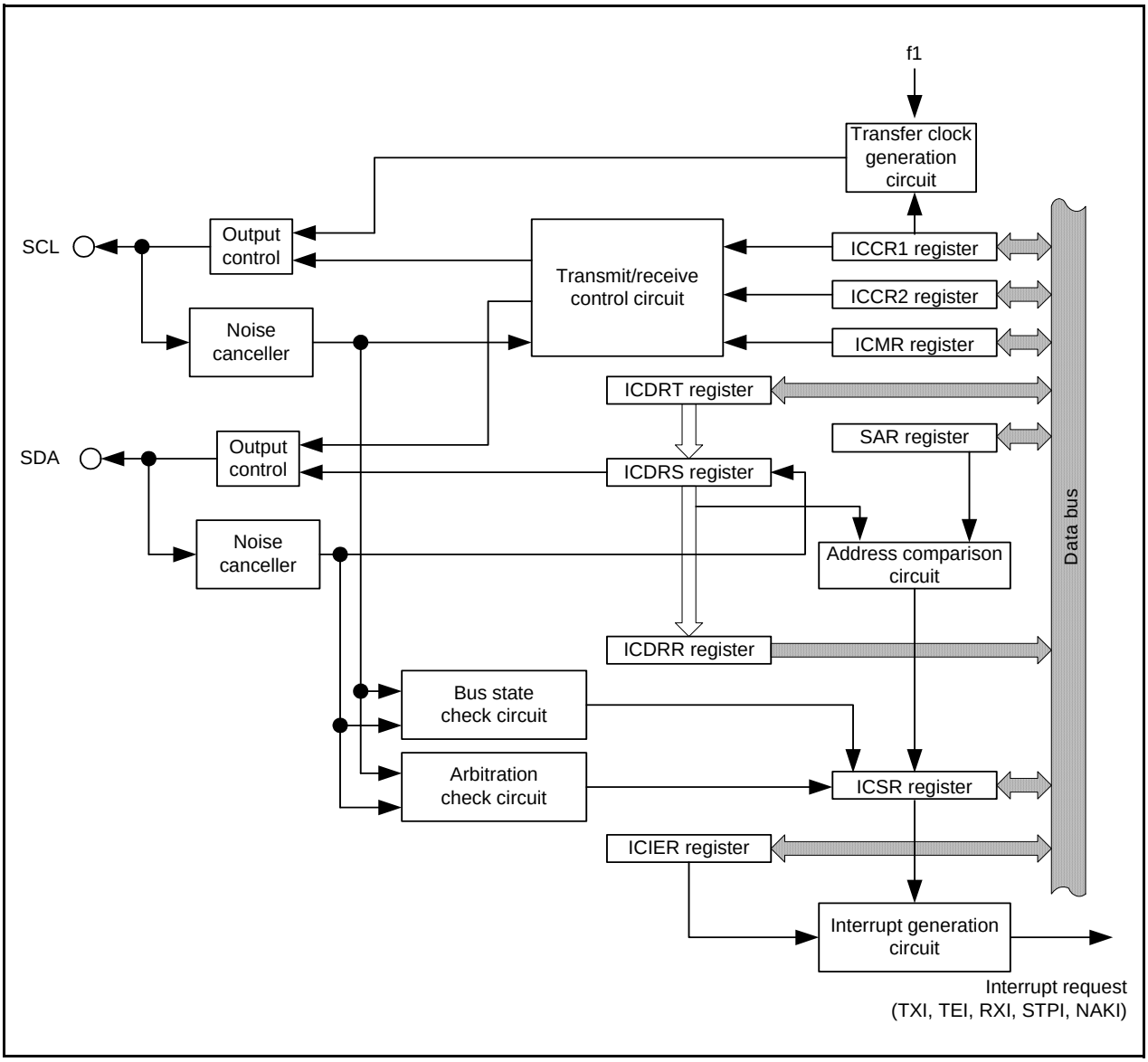


Figure 24.1 I2C bus interface Block Diagram

Table 24.2 Pin Configuration of I2C bus Interface

Pin Name	Assigned Pin	Function
SCL	P3_5	Clock I/O pin
SDA	P3_7	Data I/O pin

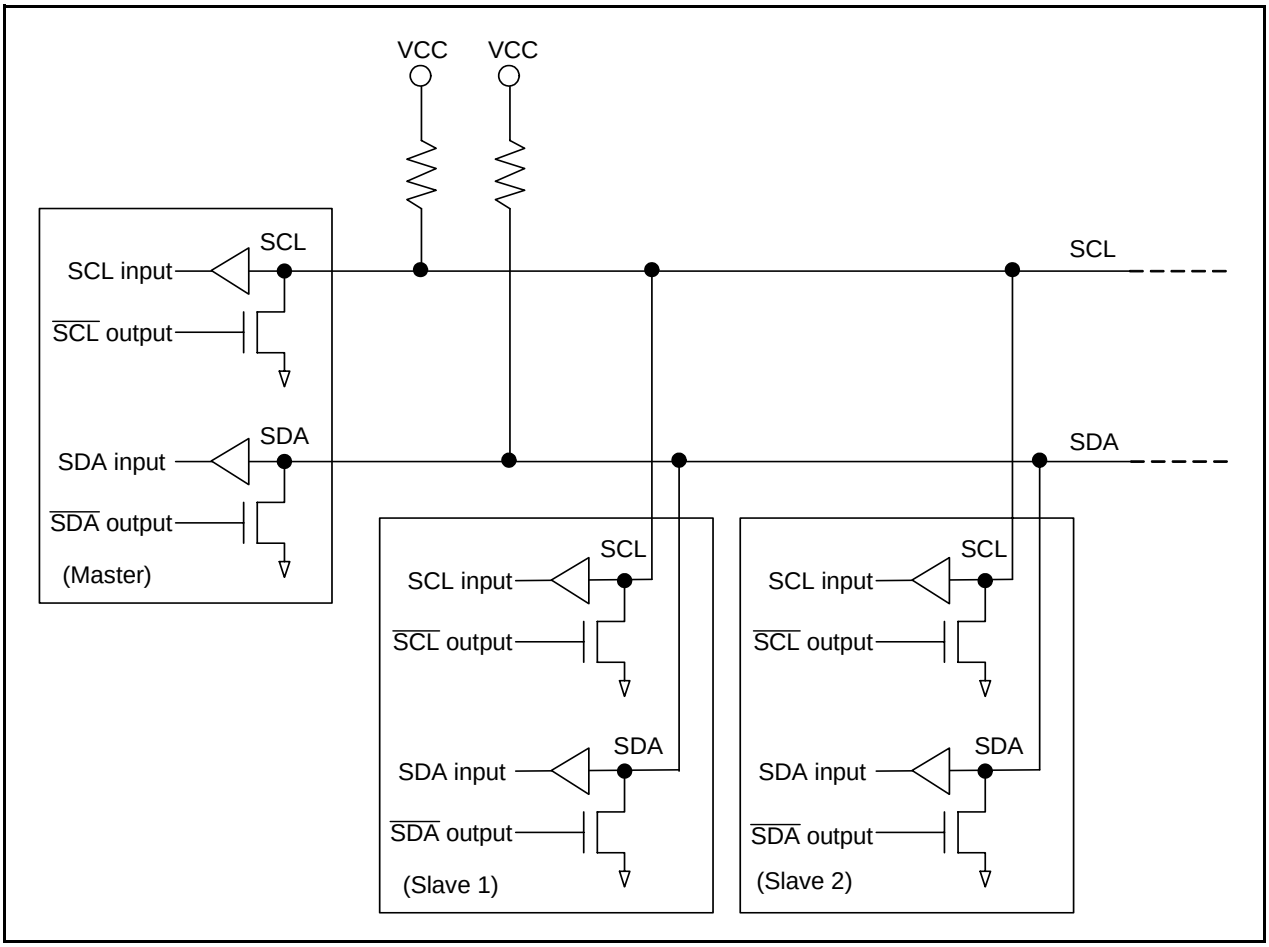


Figure 24.2 External Circuit Connection Example of Pins SCL and SDA

24.2 Registers

24.2.1 Module Standby Control Register (MSTCR)

Address 0008h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	MSTTRC	—	MSTIIC	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	MSTIIC	SSU, I2C bus standby bit	0: Active 1: Standby (1)	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	MSTTRC	Timer RC standby bit	0: Active 1: Standby (2)	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Notes:
1. Stop the SSU and the I2C bus functions before setting to standby. When the MSTIIC bit is set to 1 (standby), any access to the SSU or the I2C bus associated registers (addresses 0193h to 019Dh) is disabled.
2. Stop the timer RC function before setting to standby. When the MSTTRC bit is set to 1 (standby), any access to the timer RC associated registers (addresses 0120h to 0132h) is disabled.

24.2.2 SSU/IIC Pin Select Register (SSUIICSR)

Address 018Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	IICSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	IICSEL	SSU/I2C bus switch bit	0: SSU function selected 1: I2C bus function selected	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	—			

24.2.3 I/O Function Pin Select Register (PINSR)

Address 018Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SDADLY1	SDADLY0	IICTCHALF	IICTCTWI	IOINSEL	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bits	Set to 0.	R/W
b1	—			R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	IOINSEL	I/O port input function select bit	0: The I/O port input function depends on the PDi (i =0, 1, 3, 4) register. When the PDi_j (j = 0 to 7) bit in the PDi register is set to 0 (input mode), the pin input level is read. When the PDi_j bit in the PDi register is set to 1 (output mode), the port latch is read. 1: The I/O port input function reads the pin input level regardless of the PDi register	R/W
b4	IICTCTWI	I2C double transfer rate select bit (1)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is twice the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b5	IICTCHALF	I2C half transfer rate select bit (1)	0: Transfer rate is the same as the value set with bits CKS0 to CKS3 in the ICCR1 register 1: Transfer rate is half the value set with bits CKS0 to CKS3 in the ICCR1 register	R/W
b6	SDADLY0	SDA digital delay select bit	b7 b6 0 0: Digital delay of 3 × f1 cycles 0 1: Digital delay of 11 × f1 cycles 1 0: Digital delay of 19 × f1 cycles 1 1: Do not set.	R/W
b7	SDADLY1			R/W

Note:
1. Do not set both the IICTCTWI and IICTCHALF bits to 1 when the I2C bus function is used. Set these bits to 0 when the SSU function is used.

IOINSEL Bit (I/O port input function select bit)

The IOINSEL bit is used to select the pin level of an I/O port when the PDi_j (j = 0 to 7) bit in the PDi (i = 0, 1, 3, 4) register is set to 1 (output mode). When this bit is set to 1, the I/O port input function reads the pin input level regardless of the PDi register.

Table 24.3 lists I/O Port Values Read by Using IOINSEL Bit. The IOINSEL bit can be used to change the input function of all I/O ports.

Table 24.3 I/O Port Values Read by Using IOINSEL Bit

PDi_j bit in PDi register	0 (input mode)		1 (output mode)	
IOINSEL bit	0	1	0	1
I/O port values read	Pin input level		Port latch value	Pin input level

24.2.4 IIC bus Transmit Data Register (ICDRT)

Address 0194h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b7 to b0	This register stores transmit data. When the ICDRS register is detected as empty, the stored transmit data item is transferred to the ICDRS register and data transmission starts. When the next unit of transmit data is written to the ICDRT register while data is transmitted from the ICDRS register, continuous transmission is enabled. When the MLS bit in the ICMR register is set to 1 (data transfer with LSB-first), the MSB-LSB inverted data is read after the data is written to the ICDRT register.	R/W

24.2.5 IIC bus Receive Data Register (ICDRR)

Address 0196h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	1	1	1	1	1	1	1	1

Bit	Function	R/W
b7 to b0	This register stores receive data. When the ICDRS register receives 1 byte of data, the receive data is transferred to the ICDRR register and the next receive operation is enabled.	R

24.2.6 IIC bus Control Register 1 (ICCR1)

Address 0198h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CKS0	Transmit clock select bits 3 to 0 (1)	b3 b2 b1 b0 0 0 0 0: f1/28 0 0 0 1: f1/40 0 0 1 0: f1/48 0 0 1 1: f1/64 0 1 0 0: f1/80 0 1 0 1: f1/100 0 1 1 0: f1/112 0 1 1 1: f1/128 1 0 0 0: f1/56 1 0 0 1: f1/80 1 0 1 0: f1/96 1 0 1 1: f1/128 1 1 0 0: f1/160 1 1 0 1: f1/200 1 1 1 0: f1/224 1 1 1 1: f1/256	R/W
b1	CKS1			R/W
b2	CKS2			R/W
b3	CKS3			R/W
b4	TRS	Transfer/receive select bit (2, 3, 6)	b5 b4 0 0: Slave Receive Mode (4) 0 1: Slave Transmit Mode 1 0: Master Receive Mode 1 1: Master Transmit Mode	R/W
b5	MST	Master/slave select bit (5, 6)		R/W
b6	RCVD	Receive disable bit	After reading the ICDRR register while the TRS bit is set to 0 0: Next receive operation continues 1: Next receive operation disabled	R/W
b7	ICE	I2C bus interface enable bit (7)	0: This module is halted (Pins SCL and SDA are set to a port function) 1: This module is enabled for transfer operations (Pins SCL and SDA are in a bus drive state)	R/W

Notes:

1. Set according to the necessary transfer rate in master mode. Refer to **Tables 24.4 and 24.5 Transfer Rate Examples** for the transfer rate. This bit is used for maintaining the setup time in transmit mode of slave mode. The time is 10Tcyc when the CKS3 bit is set to 0 and 20Tcyc when the CKS3 bit is set to 1. (1Tcyc = 1/f1(s))
2. Rewrite the TRS bit between transfer frames.
3. When the first 7 bits after the start condition in slave receive mode match the slave address set in the SAR register and the 8th bit is set to 1, the TRS bit is set to 1.
4. In master mode with the I2C bus format, if arbitration is lost, bits MST and TRS are set to 0 and the IIC enters slave receive mode.
5. When an overrun error occurs in master receive mode with the clock synchronous serial format, the MST bit is set to 0 and the I2C bus enters slave receive mode.
6. In multimaster operation, use the MOV instruction to set bits TRS and MST.
7. When writing 0 to the ICE bit or 1 to the IICRST bit in the ICCR2 register during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined. Refer to **24.9 Notes on I2C bus Interface**.

24.2.7 IIC bus Control Register 2 (ICCR2)

Address 0199h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BBSY	SCP	SDAO	SDAOP	SCLO	—	IICRST	—
After Reset	0	1	1	1	1	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b1	IICRST	I2C bus control block reset bit (5)	When hang-up occurs due to communication failure during I2C bus interface operation, writing 1 resets the control block of the I2C bus interface without setting ports or initializing registers.	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b3	SCLO	SCL monitor flag	0: SCL pin is set to “L” 1: SCL pin is set to “H”	R
b4	SDAOP	SDAO write protect bit	When rewriting the SDAO bit, write 0 simultaneously. (1) When read, the content is 1.	R/W
b5	SDAO	SDA output value control bit	When read 0: SDA pin output is held “L” 1: SDA pin output is held “H” When written (1, 2) 0: SDA pin output is changed to “L” 1: SDA pin output is changed to high-impedance (“H” output via external pull-up resistor)	R/W
b6	SCP	Start/stop condition generation disable bit	When writing to the to BBSY bit, write 0 simultaneously. (3) When read, the content is 1. Writing 1 is invalid.	R/W
b7	BBSY	Bus busy bit (4, 5)	When read: 0: Bus is released (SDA signal changes from “L” to “H” while SCL signal is held “H”) 1: Bus is occupied (SDA signal changes from “H” to “L” while SCL signal is held “H”) When written (3): 0: Stop condition generated 1: Start condition generated	R/W

Notes:
1. When rewriting the SDAO bit, write 0 to the SDAOP bit simultaneously using the MOV instruction.
2. Do not write to the SDAO bit during a transfer operation.
3. Enabled in master mode. When writing to the BBSY bit, write 0 to the SCP bit simultaneously using the MOV instruction. Execute the same way when a start condition is regenerated.
4. Disabled when the clock synchronous serial format is used.
5. When writing 0 to the ICE bit in the ICCR1 register or 1 to the IICRST bit during an I2C bus interface operation, the BBSY bit and the STOP bit in the ICSR register may become undefined. Refer to **24.9 Notes on I2C bus Interface**.

24.2.8 IIC bus Mode Register (ICMR)

Address 019Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	MLS	WAIT	—	—	BCWP	BC2	BC1	BC0
After Reset	0	0	0	1	1	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BC0	Bit counters 2 to 0	I2C bus format (Read: Number of remaining transfer bits; Write: Number of next transfer data bits) (1, 2) b2 b1 b0 0 0 0: 9 bits (3) 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits Clock synchronous serial format (Read: Number of remaining transfer bits; Write: Always 000b) b2 b1 b0 0 0 0: 8 bits 0 0 1: 1 bit 0 1 0: 2 bits 0 1 1: 3 bits 1 0 0: 4 bits 1 0 1: 5 bits 1 1 0: 6 bits 1 1 1: 7 bits	R/W
b1	BC1			R/W
b2	BC2			R/W
b3	BCWP	BC write protect bit	When rewriting bits BC0 to BC2, write 0 simultaneously. (2, 4) When read, the content is 1.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
b5	—	Reserved bit	Set to 0.	R/W
b6	WAIT	Wait insertion bit (5)	0: No wait states (Data and the acknowledge bit are transferred consecutively) 1: Wait state (After the clock of the last data bit falls, a “L” period is extended for two transfer clocks)	R/W
b7	MLS	MSB-first/LSB-first select bit	0: Data transfer with MSB-first (6) 1: Data transfer with LSB-first	R/W

Notes:
1. Rewrite between transfer frames. When writing values other than 000b, write when the SCL signal is “L”.
2. When writing to bits BC0 to BC2, write 0 to the BCWP bit simultaneously using the MOV instruction.
3. After data including the acknowledge bit is transferred, these bits are automatically set to 000b. When a start condition is detected, these bits are automatically set to 000b.
4. Do not rewrite when the clock synchronous serial format is used.
5. The setting value is valid in master mode with the I2C bus format. It is invalid in slave mode with the I2C bus format or when the clock synchronous serial format is used.
6. Set to 0 when the I2C bus format is used.

24.2.9 IIC bus Interrupt Enable Register (ICIER)

Address 019Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TIE	TEIE	RIE	NAKIE	STIE	ACKE	ACKBR	ACKBT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ACKBT	Transmit acknowledge select bit	0: In receive mode, 0 is transmitted as the acknowledge bit. 1: In receive mode, 1 is transmitted as the acknowledge bit.	R/W
b1	ACKBR	Receive acknowledge bit	0: In transmit mode, the acknowledge bit received from receive device is set to 0. 1: In transmit mode, the acknowledge bit received from receive device is set to 1.	R
b2	ACKE	Acknowledge bit detection select bit	0: Content of the receive acknowledge bit is ignored and continuous transfer is performed. 1: When the receive acknowledge bit is set to 1, continuous transfer is halted.	R/W
b3	STIE	Stop condition detection interrupt enable bit	0: Stop condition detection interrupt request disabled 1: Stop condition detection interrupt request enabled (2)	R/W
b4	NAKIE	NACK receive interrupt enable bit	0: NACK receive interrupt request and arbitration lost/overrun error interrupt request disabled 1: NACK receive interrupt request and arbitration lost/overrun error interrupt request (1)	R/W
b5	RIE	Receive interrupt enable bit	0: Receive data full and overrun error interrupt request disabled 1: Receive data full and overrun error interrupt request enabled (1)	R/W
b6	TEIE	Transmit end interrupt enable bit	0: Transmit end interrupt request disabled 1: Transmit end interrupt request enabled	R/W
b7	TIE	Transmit interrupt enable bit	0: Transmit data empty interrupt request disabled 1: Transmit data empty interrupt request enabled	R/W

Notes:
1. An overrun error interrupt request is generated when the clock synchronous format is used.
2. Set the STIE bit to 1 (stop condition detection interrupt request enabled) when the STOP bit in the ICSR register is set to 0.

24.2.10 IIC bus Status Register (ICSR)

Address 019Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	TDRE	TEND	RDRF	NACKF	STOP	AL	AAS	ADZ
After Reset	0	0	0	0	X	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADZ	General call address recognition flag (1, 2)	This flag is set to 1 when a general call address is detected.	R/W
b1	AAS	Slave address recognition flag (1)	This flag is set to 1 when the first frame immediately after the start condition matches bits SVA0 to SVA6 in the SAR register in slave receive mode (slave address detection and general call address detection)	R/W
b2	AL	Arbitration lost flag/overrun error flag (1)	I2C bus format: This flag indicates that arbitration has been lost in master mode. This flag is set to 1 (3) when: • The internal SDA signal and SDA pin level do not match at the rising edge of the SCL signal in master transmit mode • The SDA pin is held “H” at start condition detection in master transmit/receive mode Clock synchronous format: This flag indicates an overrun error. This flag is set to 1 when: • The last bit of the next unit of data is received while the RDRF bit is set to 1	R/W
b3	STOP	Stop condition detection flag (1, 7)	This flag is set to 1 when a stop condition is detected after the frame is transferred.	R/W
b4	NACKF	No acknowledge detection flag (1, 4)	This flag is set to 1 when no ACKnowledge is detected from the receive device after transmission.	R/W
b5	RDRF	Receive data register full flag (1, 5)	This flag is set to 1 when receive data is transferred from registers ICDRS to ICDRR.	R/W
b6	TEND	Transmit end flag (1, 6)	I2C bus format: This flag is set to 1 at the rising edge of the 9th clock cycle of the SCL signal while the TDRE bit is set to 1. Clock synchronous format: This flag is set to 1 when the last bit of the transmit frame is transmitted.	R/W
b7	TDRE	Transmit data empty flag (1, 6)	This flag is set to 1 when: • Data is transferred from registers ICDRT to ICDRS and the ICDRT register is empty • The TRS bit in the ICCR1 register is set to 1 (transmit mode) • A start condition is generated (including retransmission) • Slave receive mode is changed to slave transmit mode	R/W

Notes:

1. Each bit is set to 0 by reading 1 before writing 0.
2. This flag is enabled in slave receive mode with the I2C bus format.
3. When two or more master devices attempt to occupy the bus at nearly the same time, if the I2C bus Interface monitors the SDA pin and the data which the I2C bus Interface transmits is different, the AL flag is set to 1 and the bus is occupied by another master.
4. The NACKF bit is enabled when the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted).
5. The RDRF bit is set to 0 when data is read from the ICDRR register.
6. Bits TEND and TDRE are set to 0 when data is written to the ICDRT register.
   When reading these bits immediately after writing to the SSTDR register, insert three or more NOP instructions between the instructions used for writing and reading.
7. When writing 0 to the ICE bit in the ICCR1 register or 1 to the IICRST bit in the ICCR2 register during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit may become undefined. Refer to **24.9 Notes on I2C bus Interface**.

When accessing the ICSR register continuously, insert one or more NOP instructions between the instructions to access it.

24.2.11 Slave Address Register (SAR)

Address 019Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FS	Format select bit	0: I2C bus format 1: Clock synchronous serial format	R/W
b1	SVA0	Slave addresses 6 to 0	Set an address different from that of the other slave devices connected to the I2C bus. When the 7 high-order bits of the first frame transmitted after the start condition match bits SVA0 to SVA6 in slave mode of the I2C bus format, the MCU operates as a slave device.	R/W
b2	SVA1			R/W
b3	SVA2			R/W
b4	SVA3			R/W
b5	SVA4			R/W
b6	SVA5			R/W
b7	SVA6			R/W

24.2.12 IIC bus Shift Register (ICDRS)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—

Bit	Function	R/W
b7 to b0	This register transmits and receives data. During transmission, data is transferred from registers ICRDT to ICDRS and transmitted from the SDA pin. During reception, data is transferred from registers ICDRS to the ICDRR after 1 byte of data reception ends.	—

24.3 Common Items for Multiple Modes

24.3.1 Transfer Clock

When the MST bit in the ICCR1 register is set to 0, the transfer clock is the external clock input from the SCL pin.
When the MST bit in the ICCR1 register is set to 1, the transfer clock is the internal clock selected by bits CKS0 to CKS3 in the ICCR1 register and bits IICTCTWI and IICTCHALF in the PINSR register and the transfer clock is output from the SCL pin. Tables 24.4 and 24.5 list the Transfer Rate Examples.

Table 24.4 Transfer Rate Examples (1)

PINSR Register		ICCR1 Register				Transfer Clock	Transfer Rate
IICTCHALF	IICTCTWI	CKS3	CKS2	CKS1	CKS0		f1 = 16 MHz
0	0	0	0	0	0	f1/28	571 kHz
					1	f1/40	400 kHz
				1	0	f1/48	333 kHz
					1	f1/64	250 kHz
			1	0	0	f1/80	200 kHz
					1	f1/100	160 kHz
				1	0	f1/112	143 kHz
					1	f1/128	125 kHz
		1	0	0	0	f1/56	286 kHz
					1	f1/80	200 kHz
				1	0	f1/96	167 kHz
					1	f1/128	125 kHz
			1	0	0	f1/160	100 kHz
					1	f1/200	80.0 kHz
				1	0	f1/224	71.4 kHz
					1	f1/256	62.5 kHz

Table 24.5 Transfer Rate Examples (2)

PINSR Register		ICCR1 Register				Transfer Clock	Transfer Rate
IICTCHALF	IICTCTWI	CKS3	CKS2	CKS1	CKS0		f1 = 16 MHz
0	1	0	0	0	0	f1/28	1142 kHz
					1	f1/40	800 kHz
				1	0	f1/48	666 kHz
					1	f1/64	500 kHz
			1	0	0	f1/80	400 kHz
					1	f1/100	320 kHz
				1	0	f1/112	286 kHz
					1	f1/128	250 kHz
		1	0	0	0	f1/56	572 kHz
					1	f1/80	400 kHz
				1	0	f1/96	334 kHz
					1	f1/128	250 kHz
			1	0	0	f1/160	200 kHz
					1	f1/200	160 kHz
				1	0	f1/224	143 kHz
					1	f1/256	125 kHz
1	0	0	0	0	0	f1/28	286 kHz
					1	f1/40	200 kHz
				1	0	f1/48	167 kHz
					1	f1/64	125 kHz
			1	0	0	f1/80	100 kHz
					1	f1/100	80 kHz
				1	0	f1/112	72 kHz
					1	f1/128	63 kHz
		1	0	0	0	f1/56	143 kHz
					1	f1/80	100 kHz
				1	0	f1/96	84 kHz
					1	f1/128	63 kHz
			1	0	0	f1/160	50 kHz
					1	f1/200	40 kHz
				1	0	f1/224	36 kHz
					1	f1/256	31 kHz

24.3.2 SDA Pin Digital Delay Selection

The digital delay value for the SDA pin can be selected by bits SDADLY0 to SDADLY1 in the PINSR register. Figure 24.3 shows the Operating Example of Digital Delay for SDA Pin.

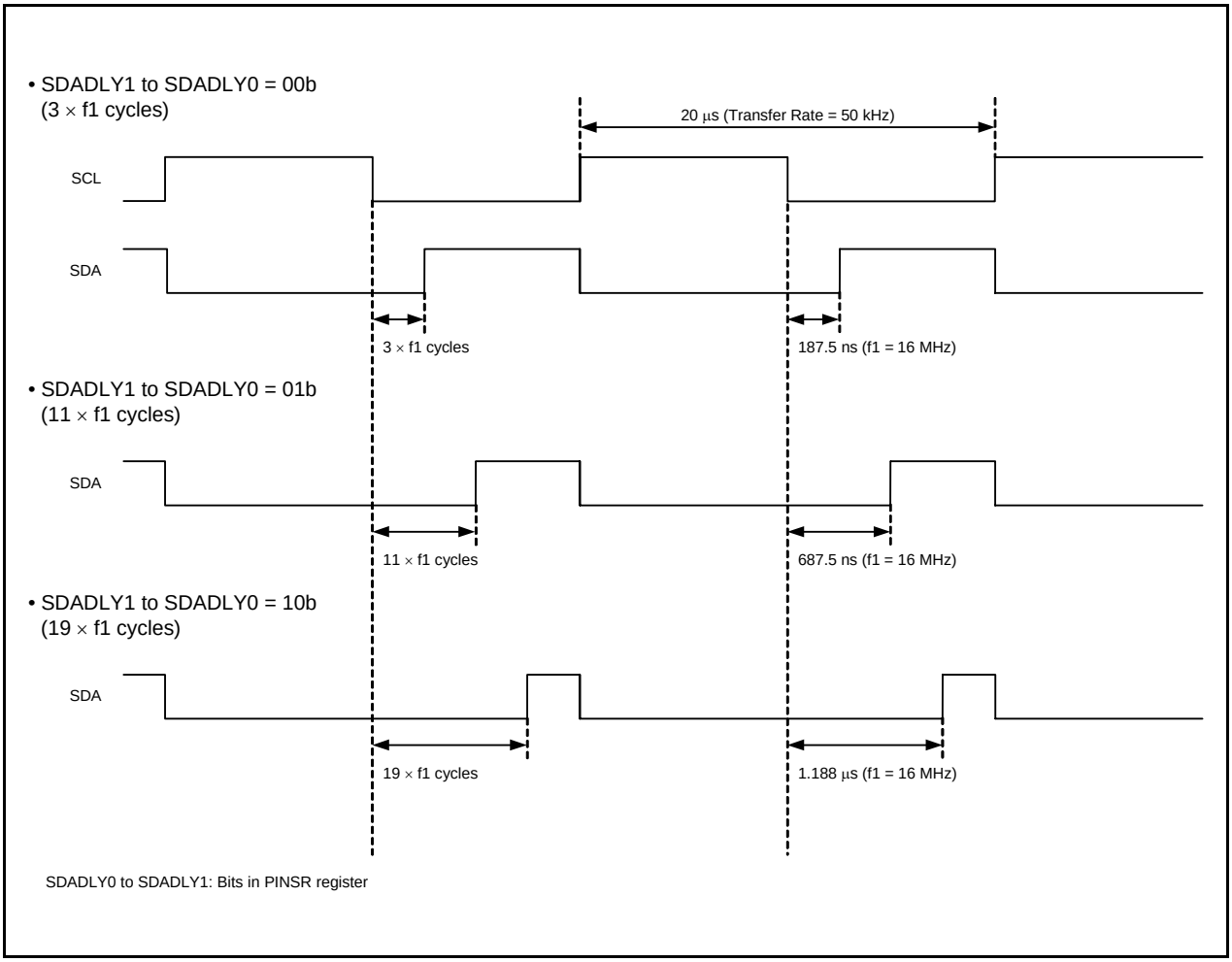


Figure 24.3 Operating Example of Digital Delay for SDA Pin

24.3.3 Interrupt Requests

The I2C bus interface has six interrupt requests when the I2C bus format is used and four interrupt requests when the clock synchronous serial format is used. Table 24.6 lists the Interrupt Requests of I2C bus Interface. Because these interrupt requests are allocated at the I2C bus interface interrupt vector table, the source must be determined bit by bit.

Table 24.6 Interrupt Requests of I2C bus Interface

Interrupt Request		Generation Condition	Format	
			I2C bus	Clock Synchronous Serial
Transmit data empty	TXI	TIE = 1 and TDRE = 1	Enabled	Enabled
Transmit ends	TEI	TEIE = 1 and TEND = 1	Enabled	Enabled
Receive data full	RXI	RIE = 1 and RDRF = 1	Enabled	Enabled
Stop condition detection	STPI	STIE = 1 and STOP = 1	Enabled	Disabled
NACK detection	NAKI	NAKIE = 1 and AL = 1 (or NAKIE = 1 and NACKF = 1)	Enabled	Disabled
Arbitration lost/overrun error			Enabled	Enabled

STIE, NAKIE, RIE, TEIE, TIE: Bits in ICIER register
AL, STOP, NACKF, RDRF, TEND, TDRE: Bits in ICSR register

When generation conditions listed in Table 24.6 are met, an I2C bus interface interrupt request is generated. Set the interrupt generation conditions to 0 by the I2C bus interface interrupt routine.
Note that bits TDRE and TEND are automatically set to 0 by writing transmit data to the ICDRT register and that the RDRF bit is automatically set to 0 by reading the ICDRR register. Especially, the TDRE bit is set to 0 when writing transmit data to the ICDRT register and set to 1 when transferring data from the ICDRT register to the ICDRS register. If the TDRE bit is further set to 0, additional 1 byte may be transmitted.
Also, set the STIE bit to 1 (stop condition detection interrupt request enabled) when the STOP bit is set to 0.

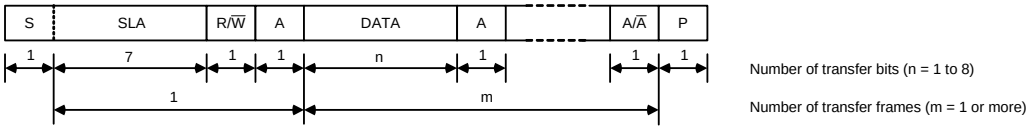
24.4 I2C bus Interface Mode

24.4.1 I2C bus Format

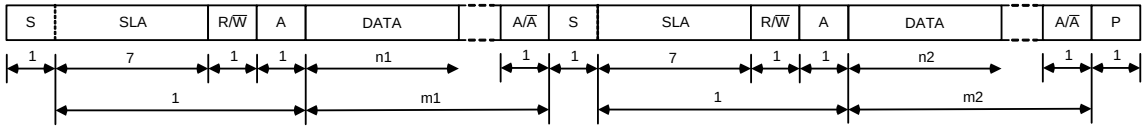
When the FS bit in the SAR register is set to 0, the I2C bus format is used for communication.
Figure 24.4 shows the I2C bus Format and Bus Timing. The first frame following the start condition consists of 8 bits.

(1) I2C bus format

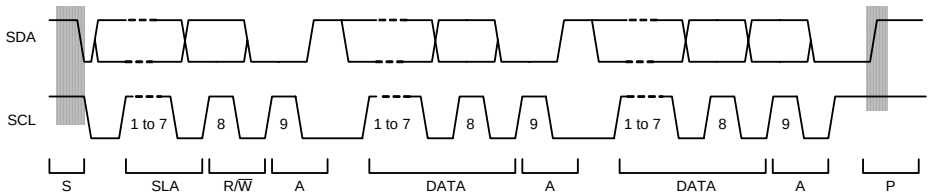
(a) I2C bus format (FS = 0)



(b) I2C bus format when start condition is retransmitted (FS = 0)



(2) I2C bus timing



Legend:
S : Start condition
The master device changes the SDA signal from “H” to “L” while the SCL signal is held “H”.
SLA : Slave address
R/W : Indicates the direction of data transmission/reception
Data is transmitted when:
R/W value is 1: From the slave device to the master device
R/W value is 0: From the master device to the slave device
A : Acknowledge
The receive device sets the SDA signal to “L”.
DATA : Transmit/receive data
P : Stop condition
The master device changes the SDA signal from “L” to “H” while the SCL signal is held “H”.

Figure 24.4 I2C bus Format and Bus Timing

24.4.2 Master Transmit Operation

In master transmit mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal. Figures 24.5 and 24.6 show the Operating Timing in Master Transmit Mode (I2C bus Interface Mode).

The transmit procedure and operation in master transmit mode are as follows.

(1) Set the STOP bit in the ICSR register to 0 for initialization, and set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then, set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting).
(2) After confirming that the bus is released by reading the BBSY bit in the ICCR2 register, set bits TRS and MST in the ICCR1 register to master transmit mode. Then, write 1 to the BBSY bit and 0 to the SCP bit with the MOV instruction (start condition generated). This will generate a start condition.
(3) After confirming that the TDRE bit in the ICSR register is set to 1 (data is transferred from registers ICDRT to ICDRS), write transmit data to the ICDRT register (data in which a slave address and R/$\overline{W}$ are indicated in the 1st byte). At this time, the TDRE bit is automatically set to 0. When data is transferred from registers ICDRT to ICDRS, the TDRE bit is set to 1 again.
(4) When 1 byte of data transmission is completed while the TDRE bit is set to 1, the TEND bit in the ICSR register is set to 1 at the rising edge of the 9th clock cycle of the transmit clock. After confirming that the slave device is selected by reading the ACKBR bit in the ICIER register, write the 2nd byte of data to the ICDRT register. Since the slave device is not acknowledged when the ACKBR bit is set to 1, generate a stop condition. Stop condition generation is enabled by writing 0 to the BBSY bit and 0 to the SCP bit with the MOV instruction. The SCL signal is fixed “L” until data is ready or a stop condition is generated.
(5) Write the transmit data after the 2nd byte to the ICDRT register every time the TDRE bit is set to 1.
(6) When the number of bytes to be transmitted is written to the ICDRT register, wait until the TEND bit is set to 1 while the TDRE bit is set to 1. Or wait for NACK (NACKF bit in ICSR register = 1) from the receive device while the ACKE bit in the ICIER register is set to 1 (when the receive acknowledge bit is set to 1, transfer is halted). Then, generate a stop condition before setting the TEND bit or the NACKF bit to 0.
(7) When the STOP bit in the ICSR register is set to 1, return to slave receive mode.

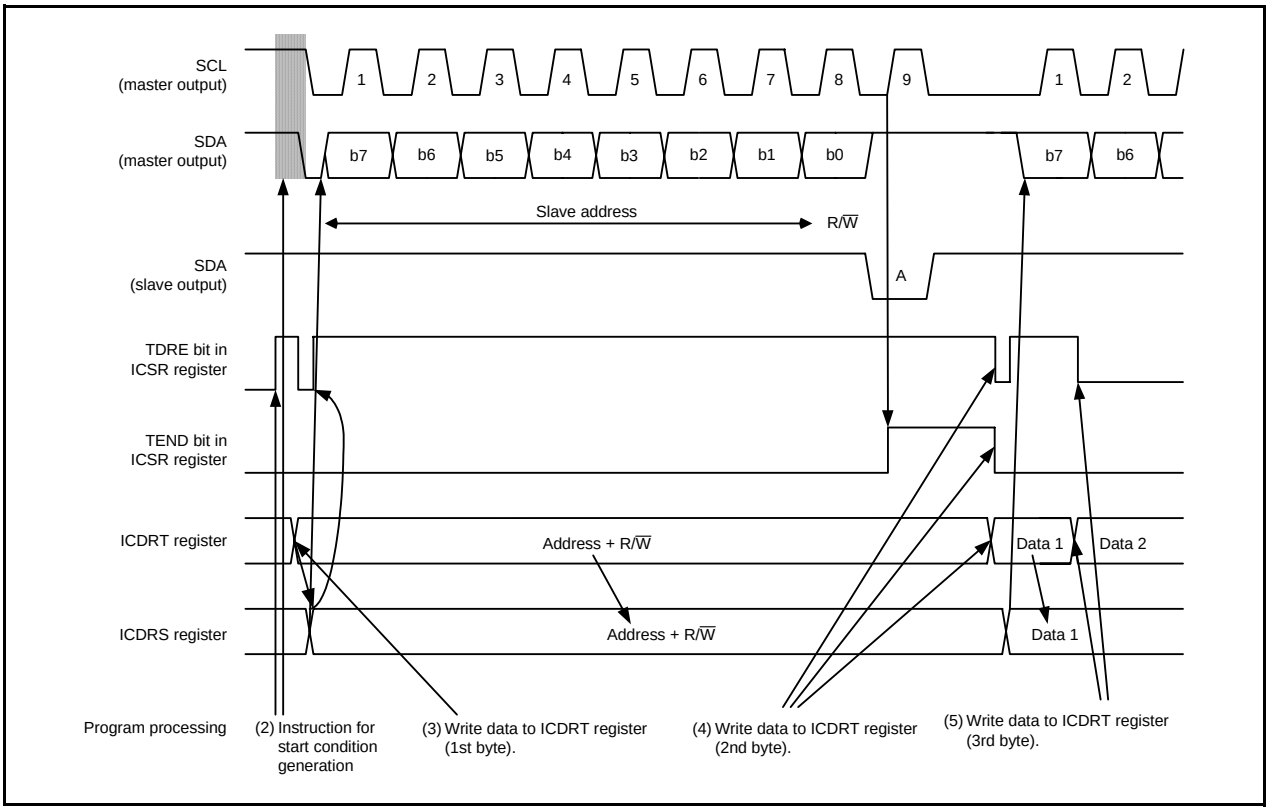


Figure 24.5 Operating Timing in Master Transmit Mode (I2C bus Interface Mode) (1)

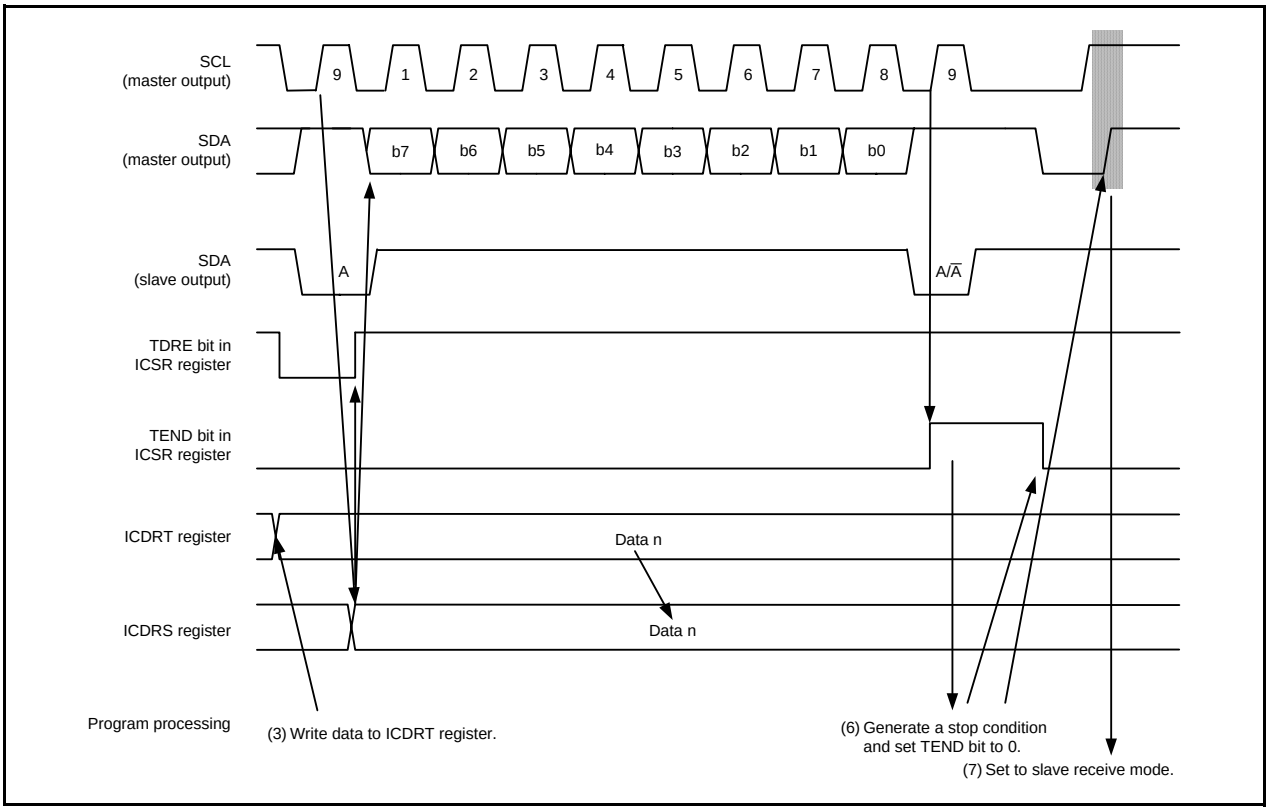


Figure 24.6 Operating Timing in Master Transmit Mode (I2C bus Interface Mode) (2)

24.4.3 Master Receive Operation

In master receive mode, the master device outputs the receive clock, receives data from the slave device, and returns an acknowledge signal. Figures 24.7 and 24.8 show the Operating Timing in Master Receive Mode (I2C bus Interface Mode).

The receive procedure and operation in master receive mode are shown below.

(1) After setting the TEND bit in the ICSR register to 0, set the TRS bit in the ICCR1 register to 0 to switch from master transmit mode to master receive mode. Then set the TDRE bit in the ICSR register to 0.
(2) Dummy reading the ICDRR register starts receive operation. The receive clock is output in synchronization with the internal clock and data is received. The master device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle of the receive clock.
(3) When 1-frame of data reception is completed, the RDRF bit in the ICSR register is set to 1 at the rising edge of the 9th clock cycle of the receive clock. At this time, if the ICDRR register is read, the received data can be read and the RDRF bit is set to 0 simultaneously.
(4) Continuous receive operation is enabled by reading the ICDRR register every time the RDRF bit is set to 1. If reading the ICDRR register is delayed by another process and the 8th clock cycle falls while the RDRF bit is set to 1, the SCL signal is fixed “L” until the ICDRR register is read.
(5) If the next frame is the last receive frame and the RCVD bit in the ICCR1 register is set to 1 (next receive operation disabled) before reading the ICDRR register, stop condition generation is enabled after the next receive operation.
(6) When the RDRF bit is set to 1 at the rising edge of the 9th clock cycle of the receive clock, generate a stop condition. When a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle. Refer to **24.9 Notes on I2C bus Interface**.
(7) When the STOP bit in the ICSR register is set to 1, read the ICDRR register and set the RCVD bit to 0 (next receive operation continues).
(8) Return to slave receive mode.

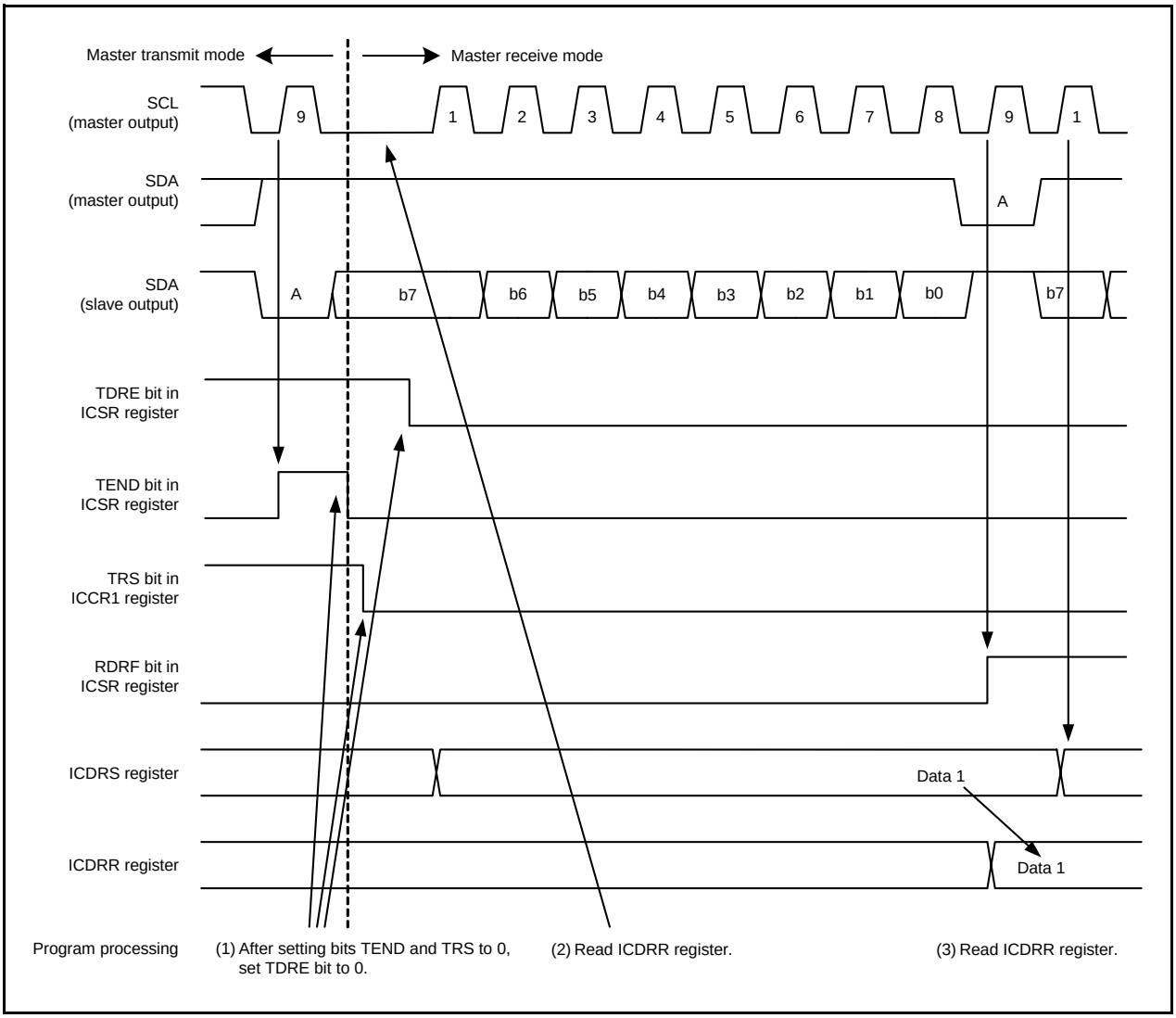


Figure 24.7 Operating Timing in Master Receive Mode (I2C bus Interface Mode) (1)

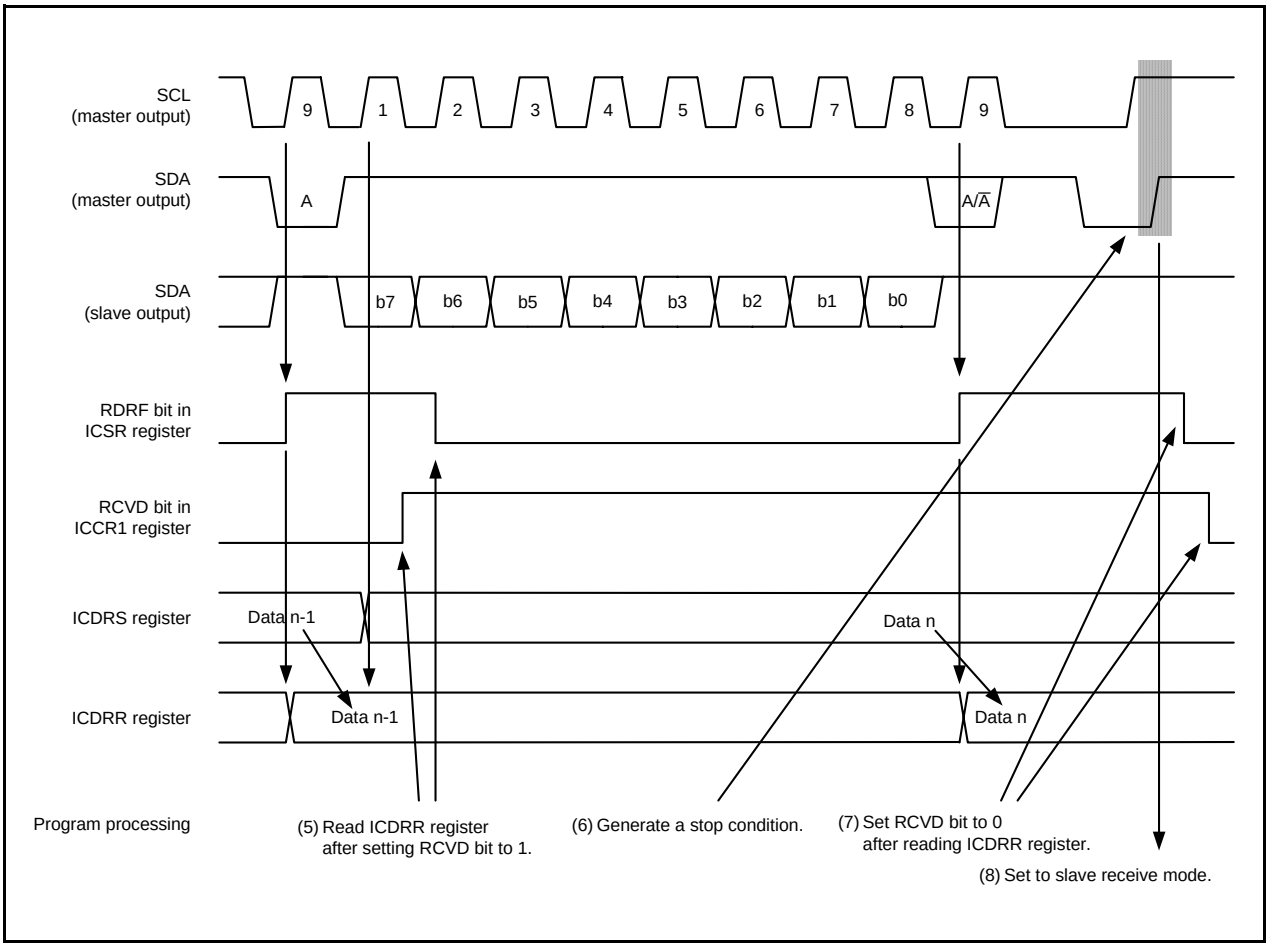


Figure 24.8 Operating Timing in Master Receive Mode (I2C bus Interface Mode) (2)

24.4.4 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data while the master device outputs the receive clock and returns an acknowledge signal. Figures 24.9 and 24.10 show the Operating Timing in Slave Transmit Mode (I2C bus Interface Mode).

The transmit procedure and operation in slave transmit mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled), and set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting). Then, set bits TRS and MST in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set by the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle. At this time, if the 8th bit of data (R/$\overline{W}$) is 1, bits TRS and TDRE in the ICSR register are set to 1, and the mode is switched to slave transmit mode automatically. Continuous transmission is enabled by writing transmit data to the ICDRT register every time the TDRE bit is set to 1.

(3) When the TDRE bit in the ICDRT register is set to 1 after the last transmit data is written to the ICDRT register, wait until the TEND bit in the ICSR register is set to 1 while the TDRE bit is set to 1. When the TEND bit is set to 1, set the TEND bit to 0.

(4) Set the TRS bit to 0 and dummy read the ICDRR register to end the process. This will release the SCL signal.

(5) Set the TDRE bit to 0.

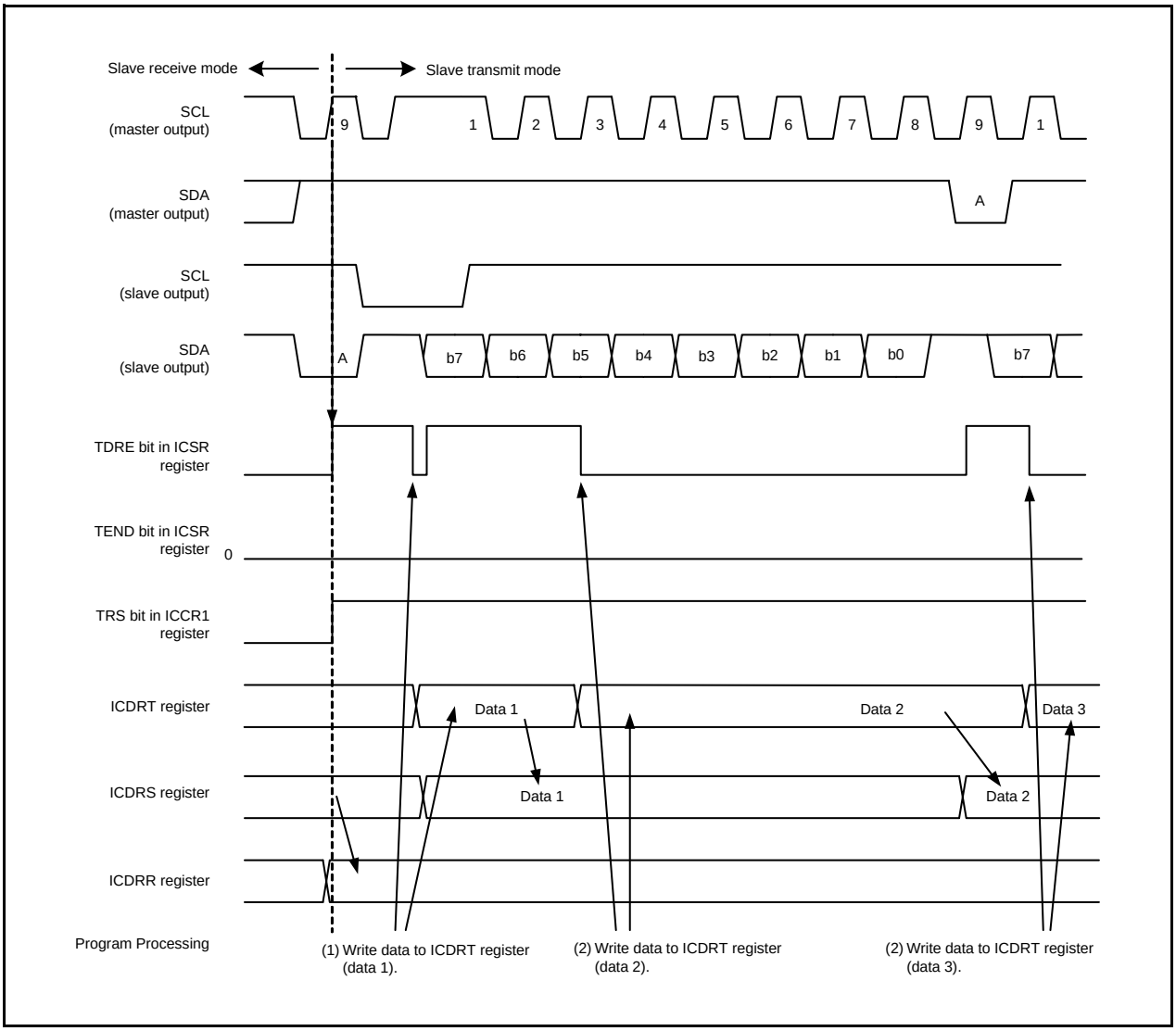


Figure 24.9 Operating Timing in Slave Transmit Mode (I2C bus Interface Mode) (1)

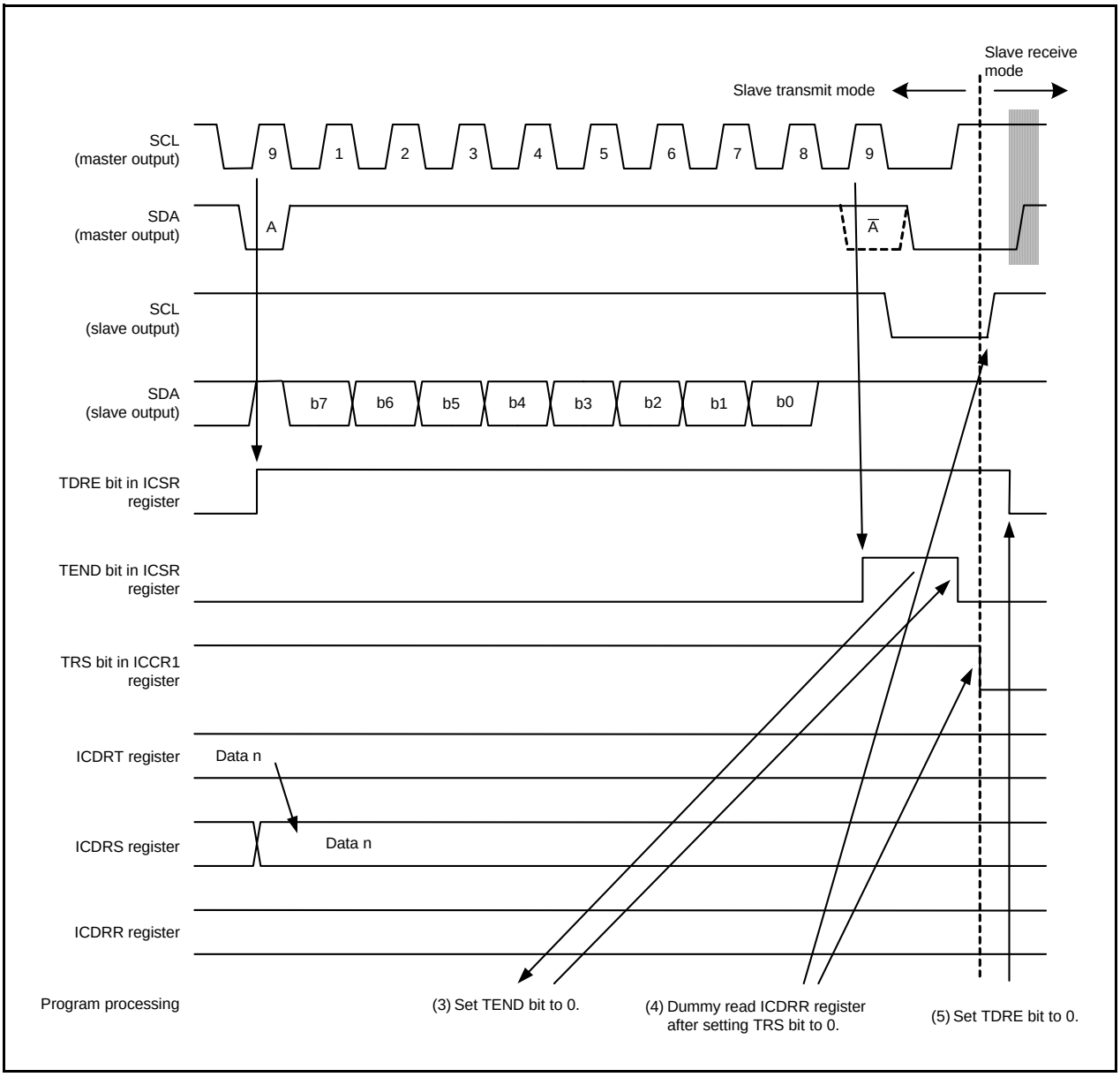


Figure 24.10 Operating Timing in Slave Transmit Mode (I2C bus Interface Mode) (2)

24.4.5 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and data, and the slave device returns an acknowledge signal. Figures 24.11 and 24.12 show the Operating Timing in Slave Receive Mode (I2C bus Interface Mode).

The receive procedure and operation in slave receive mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled), and set bits WAIT and MLS in the ICMR register and bits CKS0 to CKS3 in the ICCR1 register (initial setting). Then, set bits TRS and MST in the ICCR1 register to 0 and wait until the slave address matches in slave receive mode.

(2) When the slave address matches at the first frame after detecting the start condition, the slave device outputs the level set in the ACKBT bit in the ICIER register to the SDA pin at the rising edge of the 9th clock cycle. Since the RDRF bit in the ICSR register is set to 1 simultaneously, dummy read the ICDRR register (the read data is unnecessary because it indicates the slave address and R/$\overline{W}$).

(3) Read the ICDRR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is set to 1, the SCL signal is fixed “L” until the ICDRR register is read. The setting change of the acknowledge signal returned to the master device before reading the ICDRR register takes affect from the following transfer frame.

(4) Reading the last byte is also performed by reading the ICDRR register.

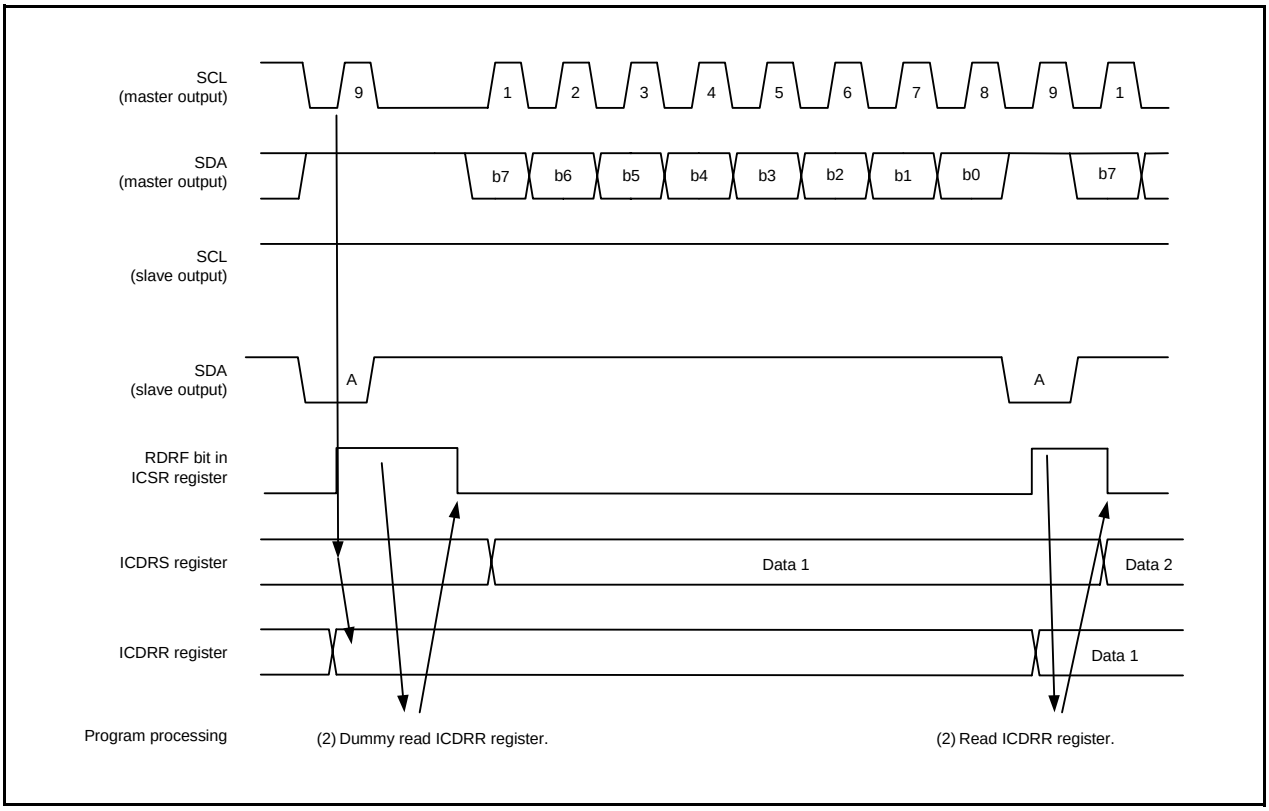


Figure 24.11 Operating Timing in Slave Receive Mode (I2C bus Interface Mode) (1)

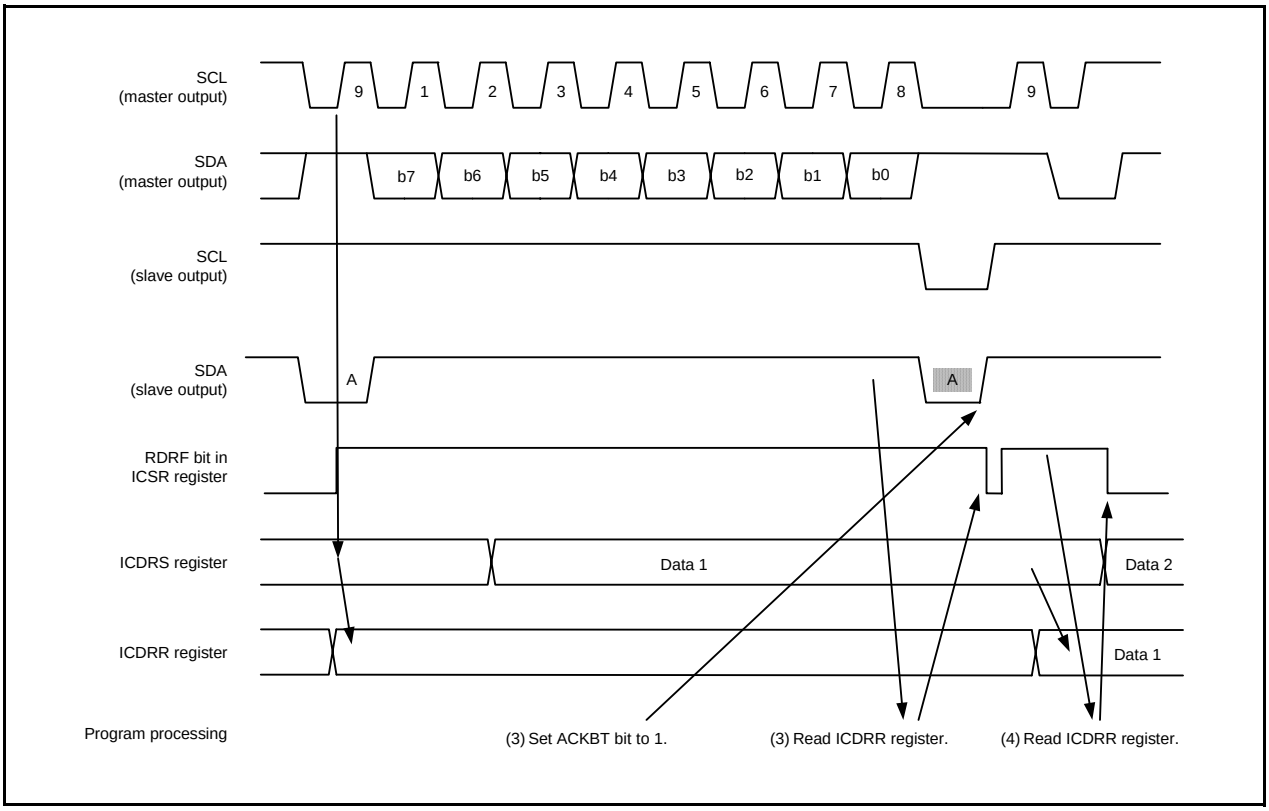


Figure 24.12 Operating Timing in Slave Receive Mode (I2C bus Interface Mode) (2)

24.5 Clock Synchronous Serial Mode

24.5.1 Clock Synchronous Serial Format

When the FS bit in the SAR register is set to 1, the clock synchronous serial format is used for communication. Figure 24.13 shows the Transfer Format of Clock Synchronous Serial Format.

When the MST bit in the ICCR1 register is set to 1, the transfer clock is output from the SCL pin. When the MST bit is set to 0, the external clock is input.

The transfer data is output between successive falling edges of the SCL clock, and data is determined at the rising edge of the SCL clock. MSB-first or LSB-first can be selected as the order of the data transfer by setting the MLS bit in the ICMR register. The SDA output level can be changed by the SDAO bit in the ICCR2 register during transfer standby.

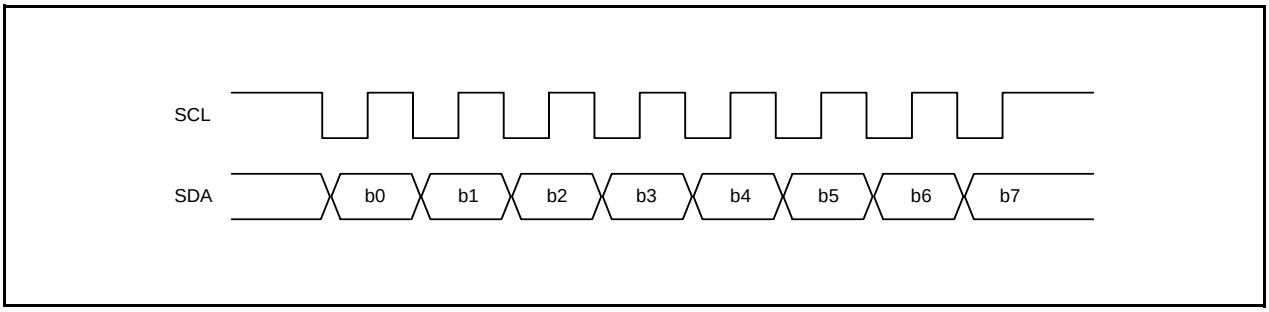


Figure 24.13 Transfer Format of Clock Synchronous Serial Format

24.5.2 Transmit Operation

In transmit mode, transmit data is output from the SDA pin in synchronization with the falling edge of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 and input when the MST bit is set to 0.
Figure 24.14 shows the Operating Timing in Transmit Mode (Clock Synchronous Serial Mode).

The transmit procedure and operation in transmit mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then set bits CKS0 to CKS3 in the ICCR1 register and the MST bit (initial setting).
(2) Set the TRS bit in the ICCR1 register to 1 to select transmit mode. This will set the TDRE bit in the ICSR register to 1.
(3) After confirming that the TDRE bit is set to 1, write transmit data to the ICDRT register. Data is transferred from registers ICDRT to ICDRS and the TDRE bit is automatically set to 1. Continuous transmission is enabled by writing data to the ICDRT register every time the TDRE bit is set to 1. To switch from transmit to receive mode, set the TRS bit to 0 while the TDRE bit is set to 1.

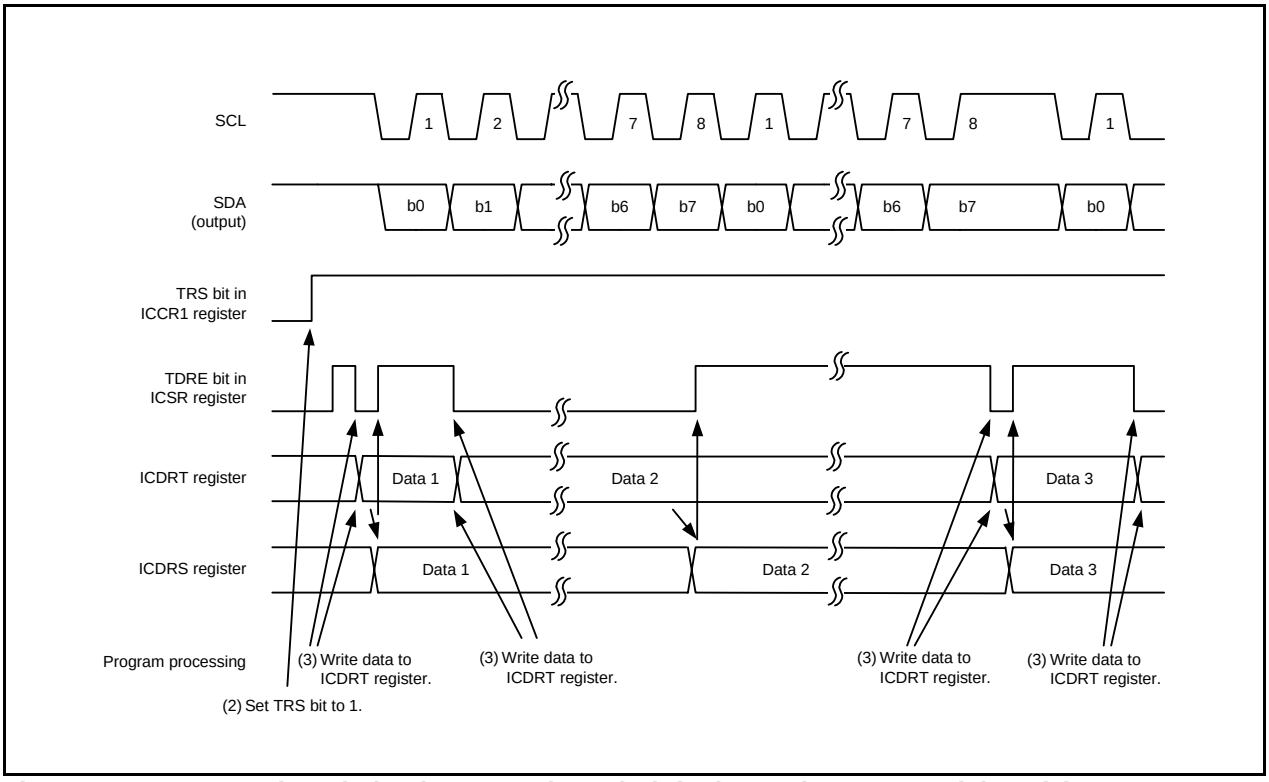


Figure 24.14 Operating Timing in Transmit Mode (Clock Synchronous Serial Mode)

24.5.3 Receive Operation

In receive mode, data is latched at the rising edge of the transfer clock. The transfer clock is output when the MST bit in the ICCR1 register is set to 1 and input when the MST bit is set to 0.
Figure 24.15 shows the Operating Timing in Receive Mode (Clock Synchronous Serial Mode).

The receive procedure and operation in receive mode are as follows.

(1) Set the ICE bit in the ICCR1 register to 1 (transfer operation enabled). Then set bits CKS0 to CKS3 in the ICCR1 register and the MST bit (initial setting).
(2) Set the MST bit to 1 while the transfer clock is being output. This will start the output of the receive clock.
(3) When the receive operation is completed, data is transferred from registers ICDRS to ICDRR and the RDRF bit in the ICSR register is set to 1. When the MST bit is set to 1, the clock is output continuously since the next byte of data is enabled for reception. Continuous reception is enabled by reading the ICDRR register every time the RDRF bit is set to 1. If the 8th clock cycle falls while the RDRF bit is set to 1, an overrun is detected and the AL bit in the ICSR register is set to 1. At this time, the last receive data is retained in the ICDRR register.
(4) When the MST bit is set to 1, set the RCVD bit in the ICCR1 register to 1 (next receive operation disabled) and read the ICDRR register. The SCL signal is fixed “H” after the following byte of data reception is completed.

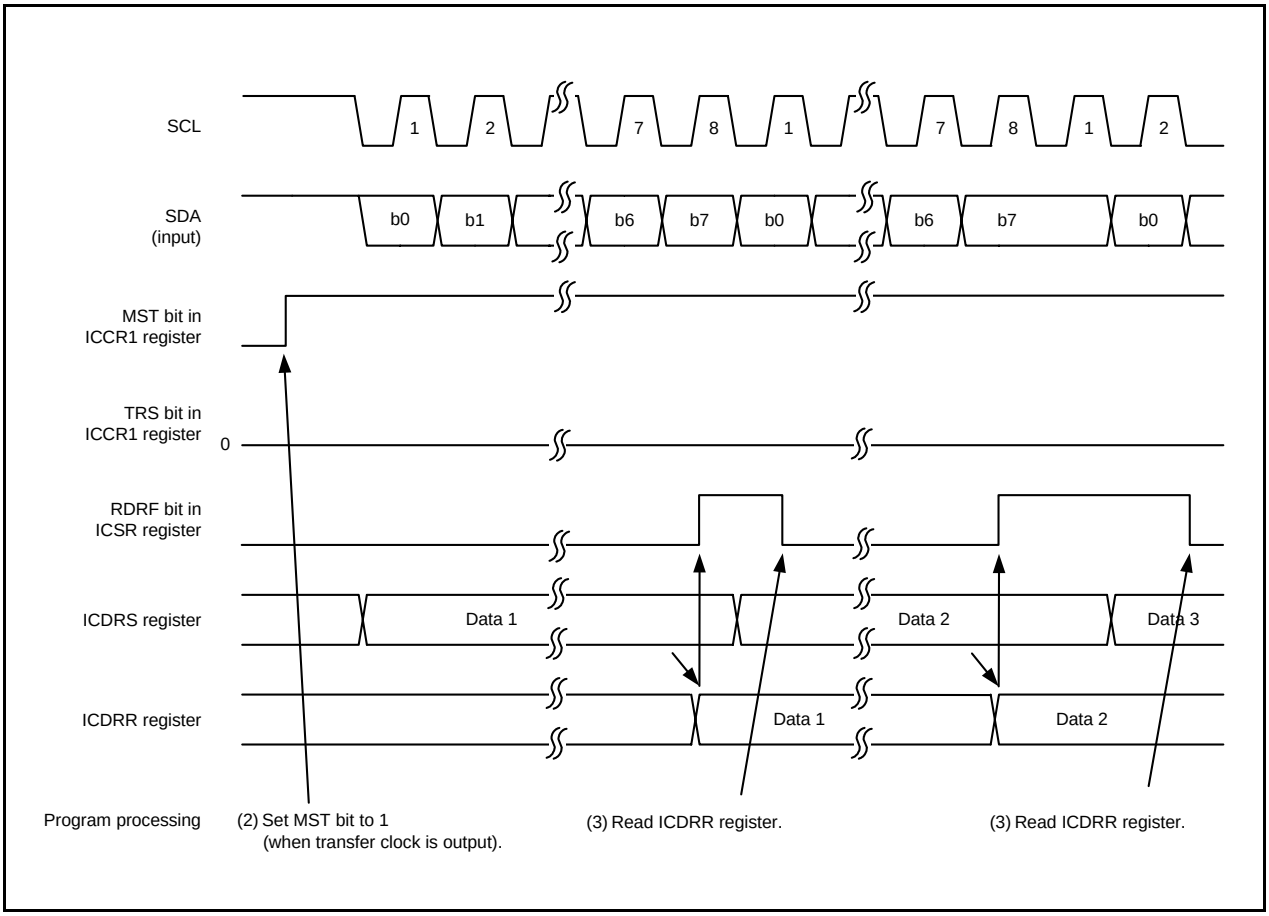


Figure 24.15 Operating Timing in Receive Mode (Clock Synchronous Serial Mode)

24.6 Examples of Register Setting

Figures 24.16 to 24.19 show Examples of Register Setting When Using I2C bus interface.

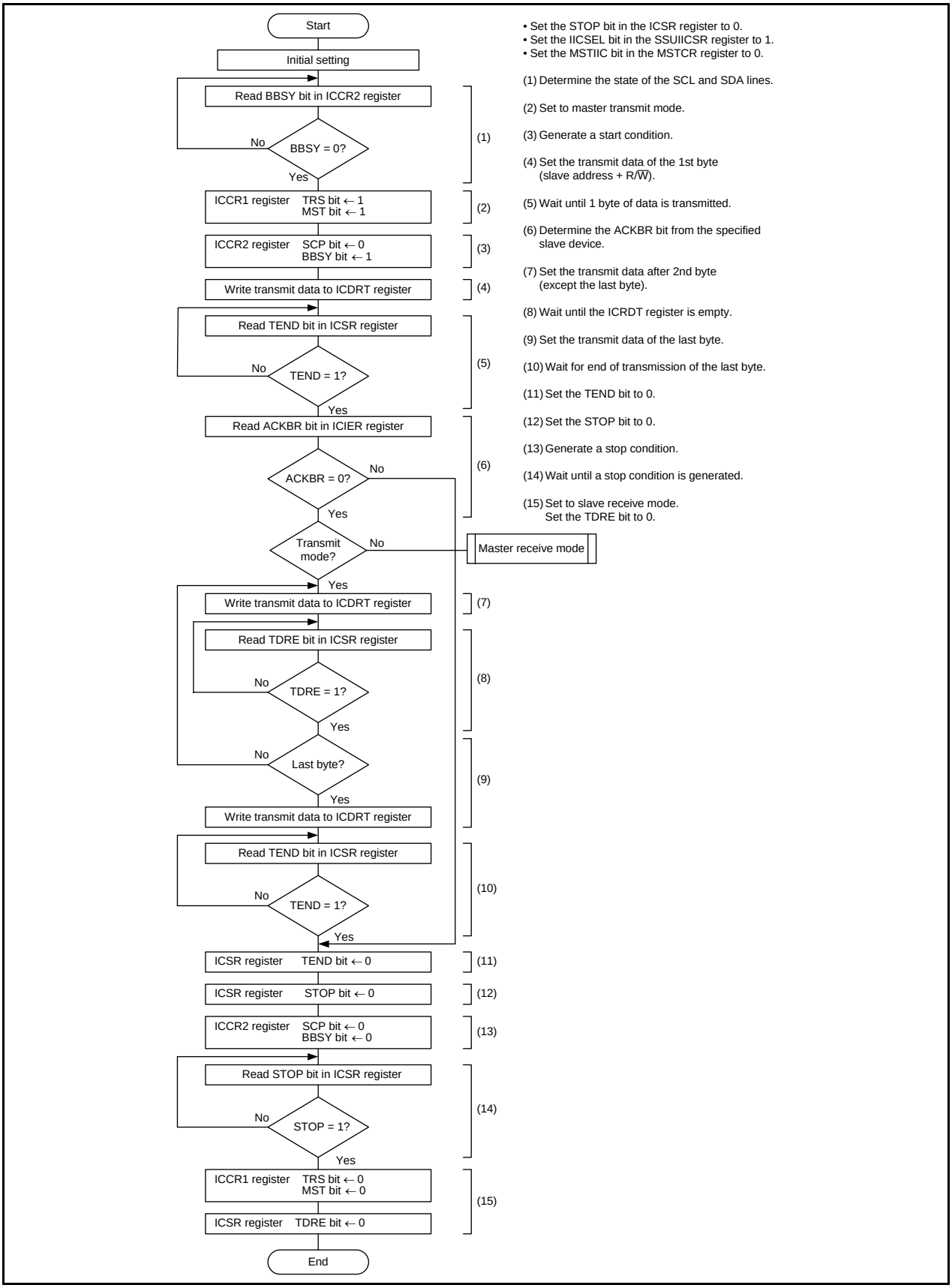
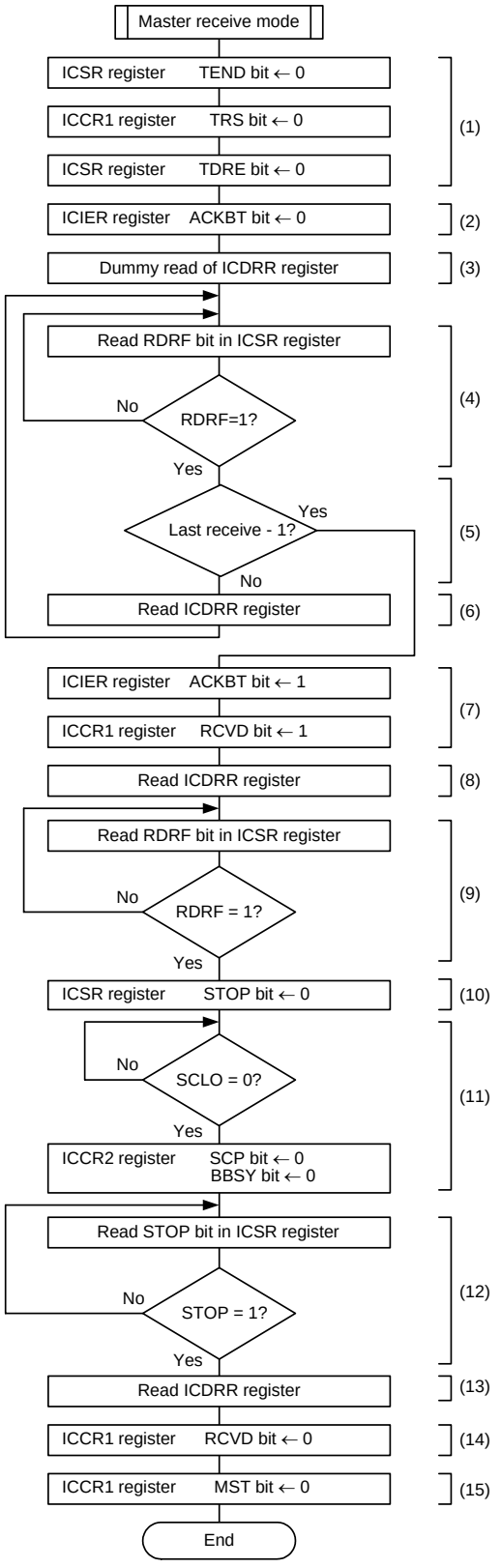


Figure 24.16 Register Setting Example in Master Transmit Mode (I2C bus Interface Mode)



(1) Set the TEND bit to 0 and set to master receive mode. Then set the TDRE bit to 0. (1, 2)

(2) Set the ACKBT bit to the transmit device. (1)

(3) Dummy read the ICDRR register. (1)

(4) Wait until 1 byte is received.

(5) Determine (last receive – 1).

(6) Read the receive data.

(7) Set the ACKBT bit of the last byte and set continuous receive operation to disable (RCVD = 1). (2)

(8) Read the receive data of (last byte – 1).

(9) Wait until the last byte is received.

(10) Set the STOP bit to 0.

(11) Generate a stop condition. (3)

(12) Wait until a stop condition is generated.

(13) Read the receive data of the last byte.

(14) Set the RCVD bit to 0.

(15) Set to slave receive mode.

Notes:
1. Do not generate interrupts during process steps (1) to (3).
2. For 1 byte of data reception, skip steps (2) to (6) after step (1) and jump to process step (7). Process step (8) is a dummy read of the ICDRR register.
3. Confirm the rising edge of the 9th clock cycle of the SCL signal before generating a stop condition. Refer to **24.9.1 Master Receive Mode**.

Figure 24.17 Register Setting Example in Master Receive Mode (I2C bus Interface Mode)

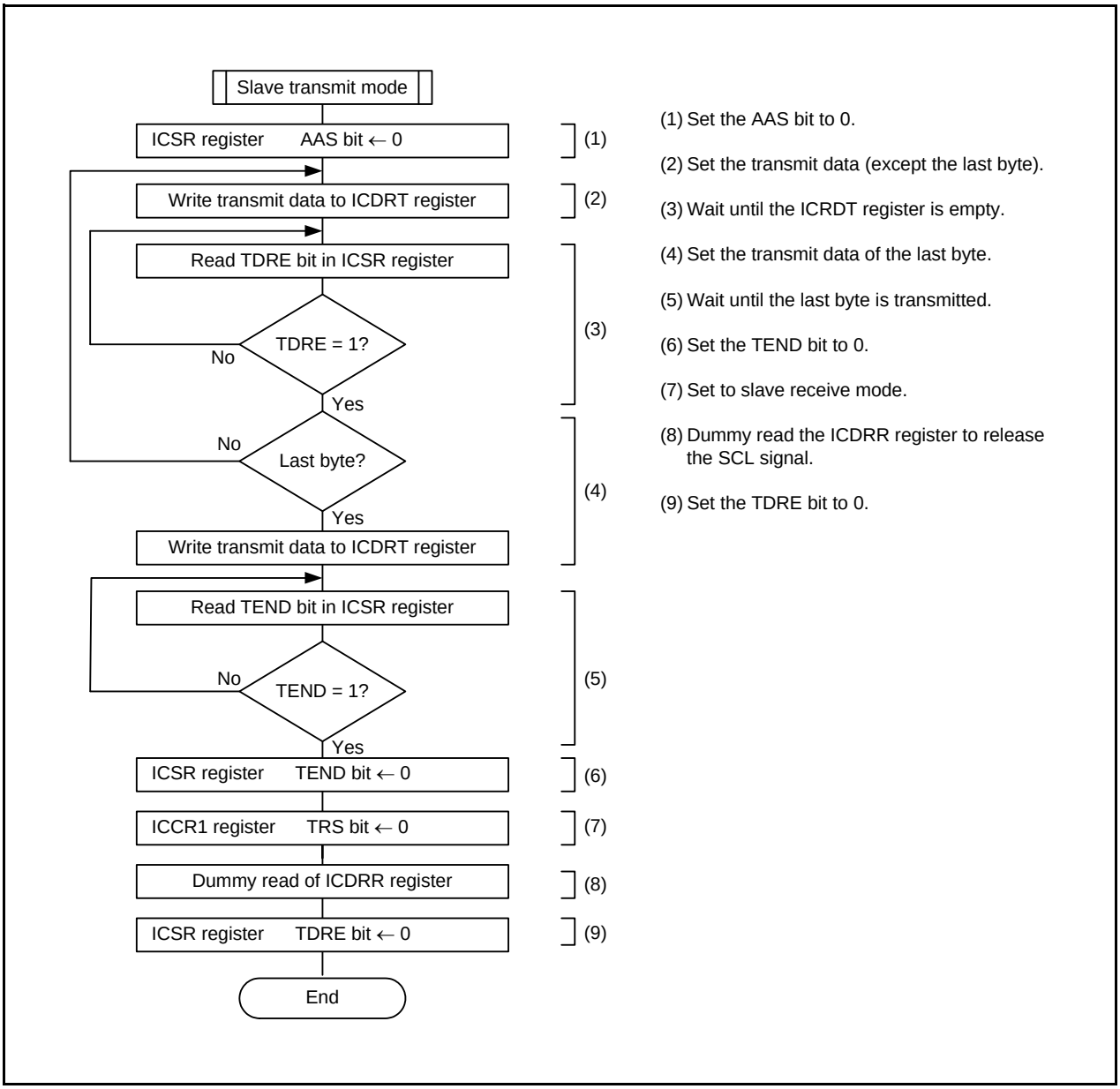
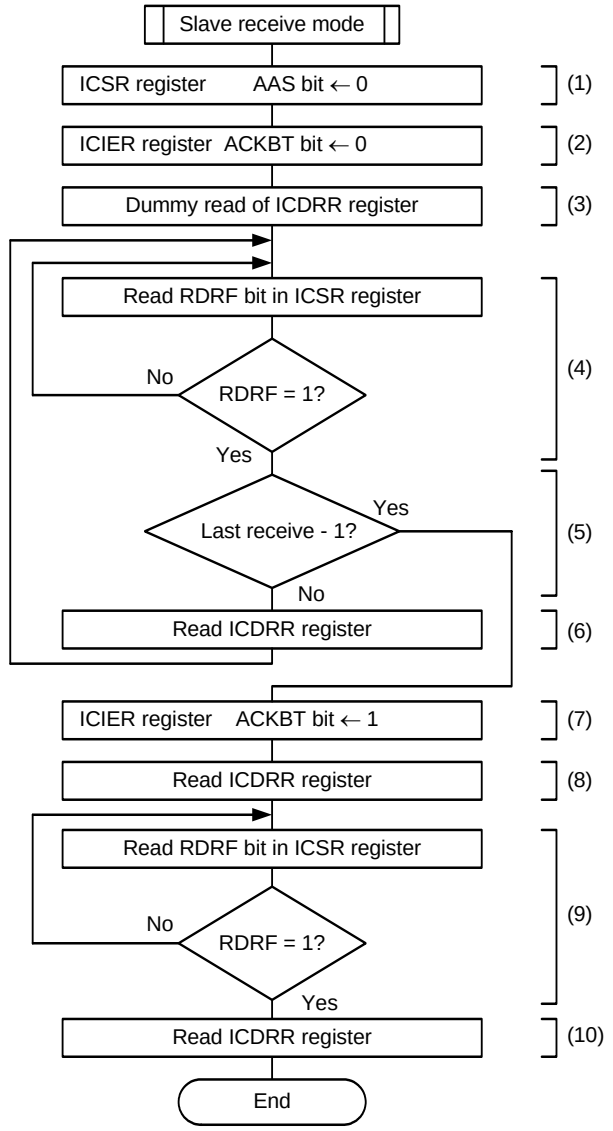


Figure 24.18 Register Setting Example in Slave Transmit Mode (I2C bus Interface Mode)



(1) Set the AAS bit to 0. (1)

(2) Set the ACKBT bit to the transmit device.

(3) Dummy read the ICDRR register.

(4) Wait until 1 byte is received.

(5) Determine (last receive - 1).

(6) Read the receive data.

(7) Set the ACKBT bit of the last byte. (1)

(8) Read the receive data of (last byte - 1).

(9) Wait until the last byte is received.

(10) Read the receive data of the last byte.

Note:
1. For 1 byte of data reception, skip steps (2) to (6) after (1) and jump to process step (7). Process step (8) is a dummy read of the ICDRR register.

Figure 24.19 Register Setting Example in Slave Receive Mode (I2C bus Interface Mode)

24.7 Noise Canceller

The states of pins SCL and SDA are routed through the noise canceller before being latched internally. Figure 24.20 shows a Noise Canceller Block Diagram.

The noise canceller consists of two cascaded latch and match detector circuits. When the SCL pin input signal (or SDA pin input signal) is sampled on f1 and two latch outputs match, the level is passed forward to the next circuit. When they do not match, the former value is retained.

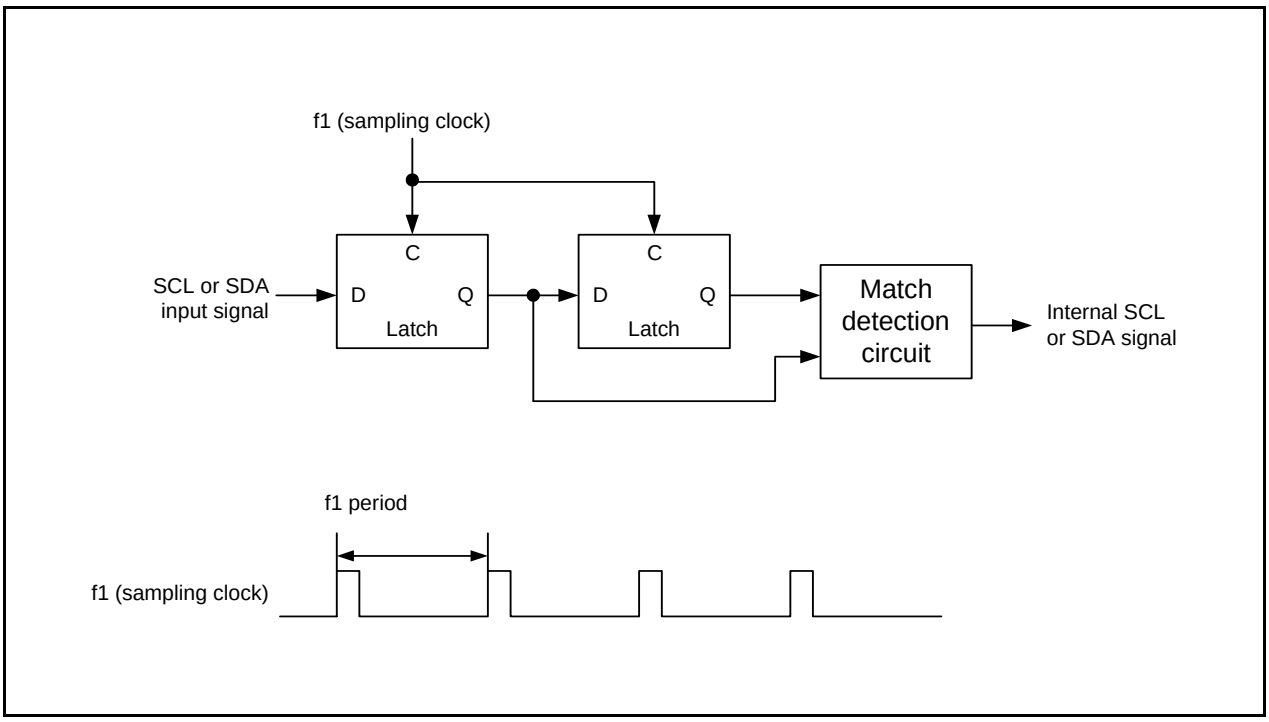


Figure 24.20 Noise Canceller Block Diagram

24.8 Bit Synchronization Circuit

When the I2C bus interface is set to master mode, the high-level period may become shorter if:
- The SCL signal is driven L level by a slave device
- The rise speed of the SCL signal is reduced by a load (load capacity or pull-up resistor) on the SCL line.

Therefore, the SCL signal is monitored and communication is synchronized bit by bit.
Figure 24.21 shows the Bit Synchronization Circuit Timing and Table 24.7 lists the Time between Changing SCL Signal from “L” Output to High-Impedance and Monitoring SCL Signal.

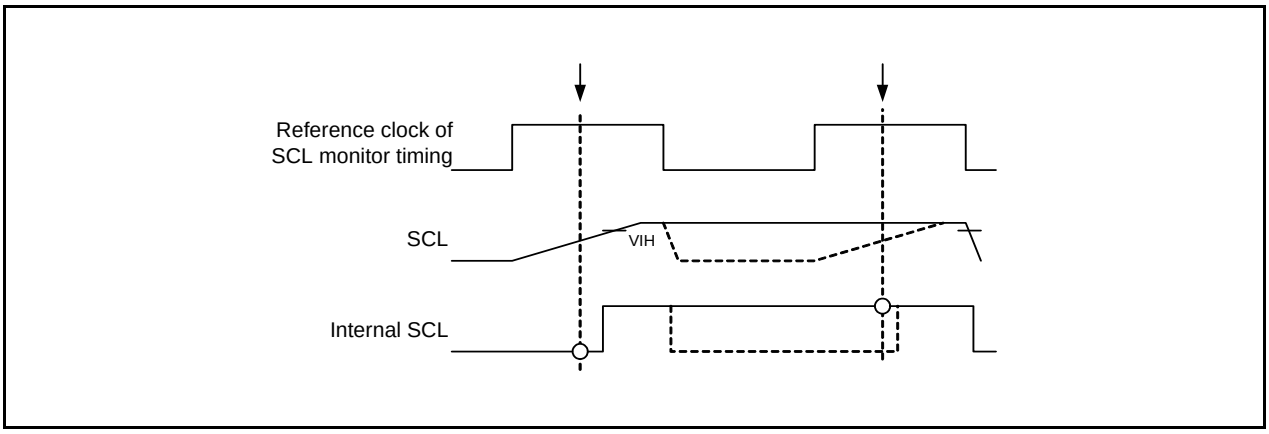


Figure 24.21 Bit Synchronization Circuit Timing

Table 24.7 Time between Changing SCL Signal from “L” Output to High-Impedance and Monitoring SCL Signal

ICCR1 Register		SCL Monitoring Time
CKS3	CKS2	
0	0	7.5Tcyc
	1	19.5Tcyc
1	0	17.5Tcyc
	1	41.5Tcyc

1Tcyc = 1/f1(s)

24.9 Notes on I2C bus Interface

To use the I2C bus interface, set the IICSEL bit in the SSUIICSR register to 1 (I2C bus interface function selected).

24.9.1 Master Receive Mode

After a master receive operation is completed, when a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle.

24.9.1.1 Countermeasure

After a master receive operation is completed, confirm the falling edge of the ninth clock cycle of SCL and generate a stop condition or regenerate a start condition.
Confirm the falling edge of the ninth clock cycle of SCL as follows: Confirm the SCLO bit in the ICCR2 register (SCL monitor flag) becomes 0 (SCL pin is low) after confirming the RDRF bit in the ICSR register (receive data register full flag) becomes 1.

24.9.2 ICE Bit in ICCR1 Register and IICRST Bit in ICCR2 Register

When writing 0 to the ICE bit or 1 to the IICRST bit during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined.

24.9.2.1 Conditions When Bits Become Undefined

- When this module occupies the bus in master transmit mode (bits MST and TRS in the ICCR1 register are 1).
- When this module occupies the bus in master receive mode (the MST bit is 1 and the TRS bit is 0).
- When this module transmits data in slave transmit mode (the MST bit is 0 and the TRS bit is 1).
- When this module transmits an acknowledge in slave receive mode (bits MST and TRS are 0).

24.9.2.2 Countermeasures

- When the start condition (the SDA falling edge when SCL is high) is input, the BBSY bit becomes 1.
- When the stop condition (the SDA rising edge when SCL is high) is input, the BBSY bit becomes 0.
- When writing 1 to the BBSY bit, 0 to the SCP bit, and the start condition (the SDA falling edge when SCL is high) is output while SCL and SDA are high in master transmit mode, the BBSY bit becomes 1.
- When writing 0 to bits BBSY and SCP, the stop condition (the SDA rising edge when SCL is high) is output while SDA is low, and this is the only module that holds SCL low in master transmit mode or master receive mode, the BBSY bit becomes 0.
- When writing 1 to the FS bit in the SAR register, the BBSY bit becomes 0.

24.9.2.3 Additional Descriptions Regarding IICRST Bit

- When writing 1 to the IICRST bit, bits SDAO and SCLO in the ICCR2 register become 1.
- When writing 1 to the IICRST bit in master transmit mode and slave transmit mode, the TDRE bit in the ICSR register becomes 1.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, writing to bits BBSY, SCP, and SDAO is disabled. Write 0 to the IICRST bit before writing to the BBSY bit, SCP bit, or SDAO bit.
- Even when writing 1 to the IICRST bit, the BBSY bit does not become 0. However, the stop condition (the SDA rising edge when SCL is high) may be generated depending on the states of SCL and SDA and the BBSY bit may become 0. There may also be a similar effect on other bits.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, data transmission/reception is stopped. However, the function to detect the start condition, stop condition, or arbitration lost operates. The values in the ICCR1 register, ICCR2 register, or ICSR register may be updated depending on the signals applied to pins SCL and SDA.

25. Baseband Functionality

The contents described in this chapter are supported by the application program interface (API) of the Renesas RF driver. Thus, the settings in this chapter are not necessary when using the Renesas RF driver.

25.1 Baseband Functional Description

The following baseband functions are implemented in hardware:

(1) 26-bit timer
(2) Transmit RAM
(3) Receive RAM
(4) Transmit frame generator
(5) Filter function
(6) Interrupts
(7) CRC circuit
(8) Automatic ACK response function
(9) Automatic ACK reception function
(10) Automatic reception switching function
(11) ANTSW output switching function
(12) Automatic CSMA-CA function
(13) State transitions
(14) Baseband associated registers
(15) Control sequence
(16) Examples of automatic transmit and receive operations

25.1.1 Baseband Block Diagram

Figure 25.1 shows the Baseband Block Diagram.

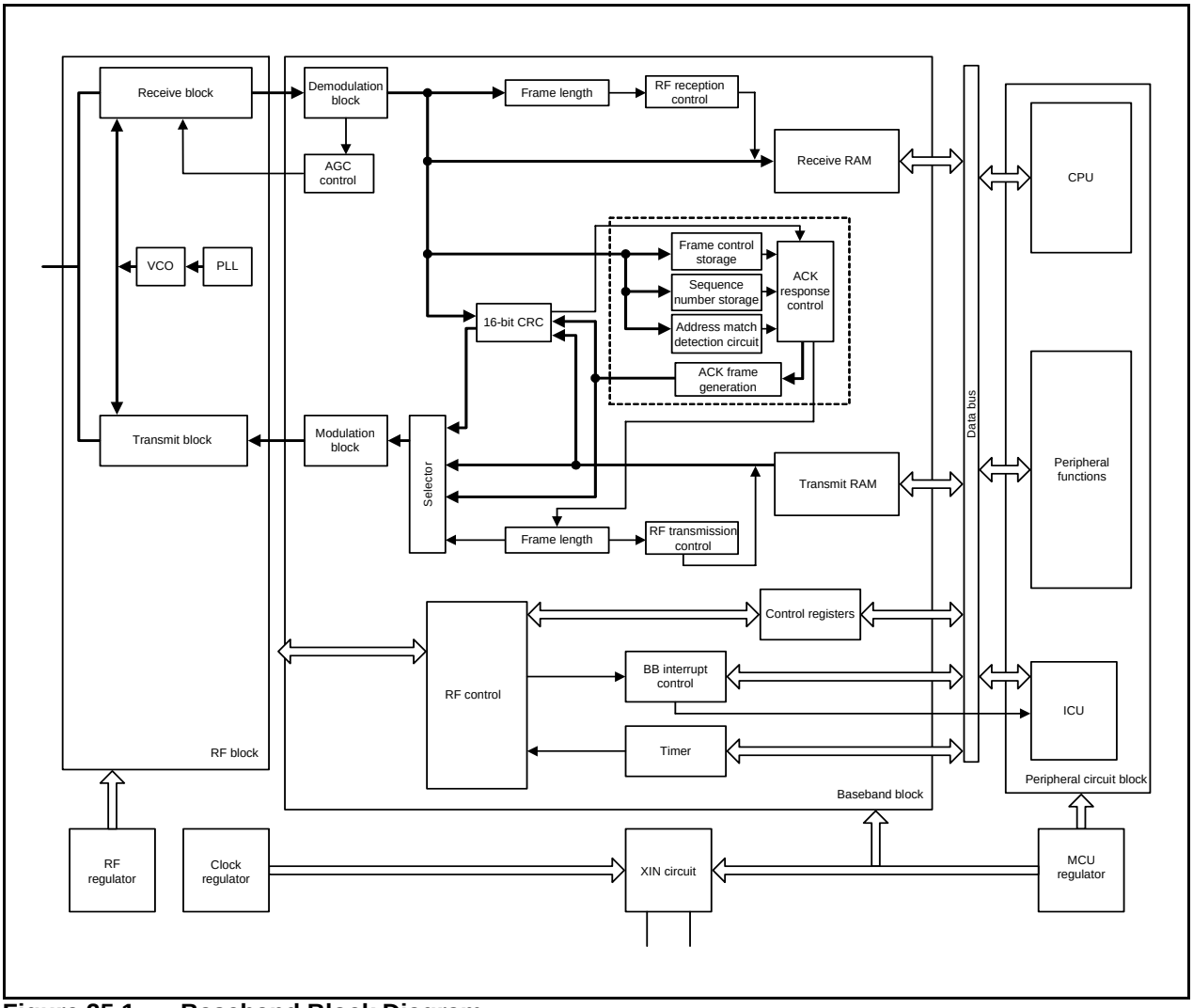


Figure 25.1 Baseband Block Diagram

25.1.2 Baseband Terminological Description

Terms used in this chapter are shown below:

- IDLE status: Status where the RF regulator, which is supplied to the internal RF block, has started up stably
- RF regulator: Dedicated on-chip regulator for the RF block
- Clock regulator: Dedicated on-chip regulator for the XIN circuit to stabilize the reference 16-MHz CLK. The power supply for the clock regulator is applied from the VCCRF pin.

25.1.3 26-Bit Timer

Three timer compare functions are implemented in the 26-bit timer. When the timer value and the timer compare i (i = 0 to 2) value match, a BB timer compare i (i = 0 to 2) interrupt can be generated.
The clock which is the count source 16 MHz divided by 256 by using the prescaler is input to the timer.
Figure 25.2 shows the 26-Bit Timer Configuration.

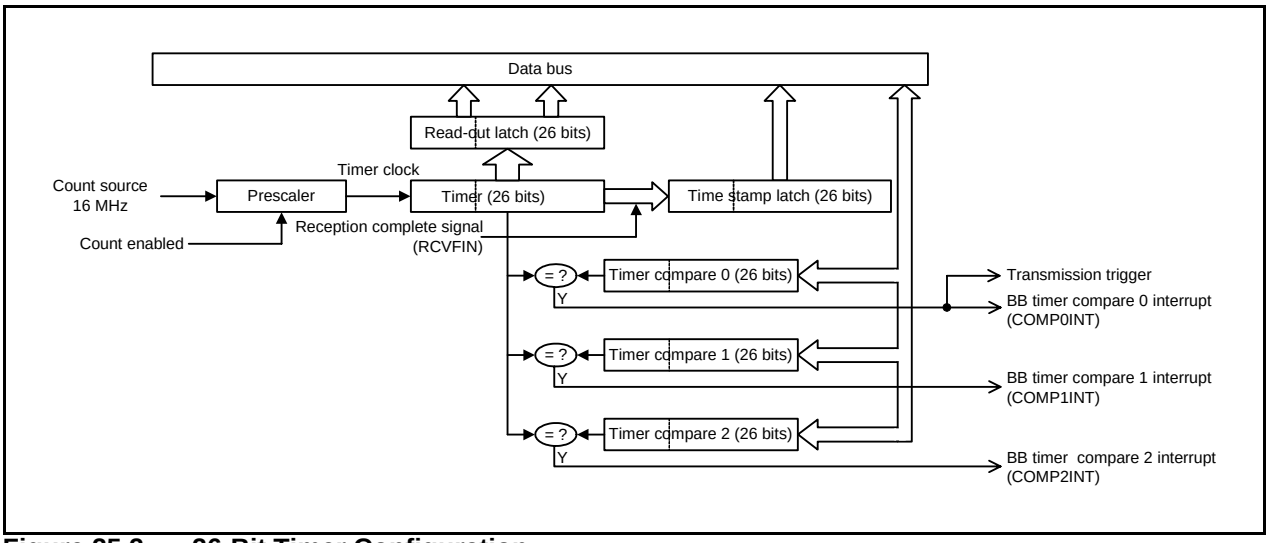


Figure 25.2 26-Bit Timer Configuration

25.1.3.1 BB Timer Compare i Interrupt

A timer compare i interrupt is generated when the timer value and the BB timer compare i value match.
Timer compare 0 also functions as a transmission start signal.
Transmission automatically starts 144 μs after a transmission start signal is generated.

25.1.3.2 Time Stamp

The timer value when frame reception is completed is stored in registers BBTSTAMP0 and BBTSTAMP1.
These registers are retained until the next frame reception is completed.

25.1.3.3 Reading Timer Values

Timer values can be read from registers BBTIMEREAD0 and BBTIMEREAD1. When reading timer values, read the BBTIMEREAD0 register (lower byte) first.
When either bits 7 to 0 or bits 15 to 8 in the BBTIMEREAD0 register (or both) are read, the count value of all bits is latched. The latched value is discarded when bits 25 and 24 in the BBTIMEREAD1 register (highest byte) are read.
If the BBTIMEREAD1 register is read first, note the BBTIMEREAD0 register is not latched.
After reading the BBTIMEREAD0 register, its value is not updated even if this register is read again without reading the BBTIMEREAD1 register, and the previously read value is read.

25.1.4 Transmit RAM

127 bytes of transmit RAM is implemented exclusively for the baseband block.
The addresses are 2E00h to 2E7Eh.
Frames are transmitted each 1 byte of transmit RAM data, beginning with the start address.
As the next frame transmission always begins with the start address even if transmit RAM data is less than 127 bytes, write transmit RAM data from the start address.
If the internal transmit counter value is equal to or greater than the written address, a transmit overrun interrupt request is generated, and transmit processing is cancelled simultaneously.
The data written to transmit RAM can be read.

25.1.5 Receive RAM

127 × 2 bytes (banks 0 and 1) of receive RAM is implemented exclusively for the baseband block.
The addresses are 2E80h to 2EFEh and read-only.
After the baseband functions are enabled, the storage of frames begins with receive RAM bank 0, and frames are stored in bank 0 or 1 alternately for each reception. The reception complete interrupt request corresponding to the bank is generated each time frame reception is completed. When reading receive RAM, the receive RAM data of the bank set by the RCVBANKSEL bit in the BBTXRXMODE3 register is read.
Received frames are stored each 1 byte, beginning with the start address.
Even if a received frame is less than 127 bytes, the next frame is stored beginning with the start address of receive RAM when the next frame reception starts.
The data in receive RAM can be read during reception. In that case, the address of the currently receiving data can be confirmed by reading the value of the BBRXCOUNT register.
Bits ADRSFILEN and LVLFILEN in the BBTXRXMODE3 register can be used to enable or disable the filter for frames to be captured. Refer to **25.1.7 Filter Function** for details.
Bits RCVBANK0 and RCVBANK1 in the BBTXRXST0 register can be used as the flags for transferring data in receive RAM. These bits are automatically set to 1 (received data present) when reception starts. After received data has been read by a program, these bits are cleared to 0 (reception enabled). If frame reception restarts while these bits are set to 1 (received data present), a receive overrun interrupt is generated.
The RCVBANKST bit in the BBTXRXST0 register can be used to confirm whether the last received frame is in bank 0 or bank 1.

25.1.6 Transmit Frame Generator

This function automatically generates and outputs transmit frames.
Figure 25.3 shows the Transmit Frame Structure.

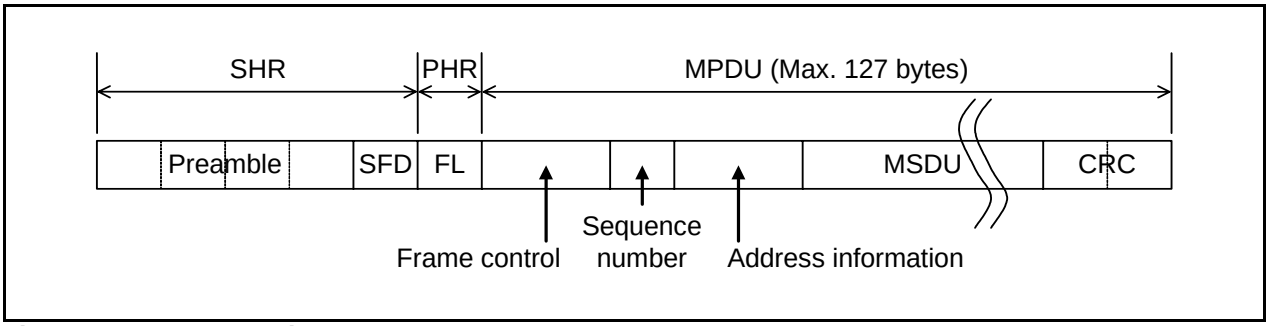


Figure 25.3 Transmit Frame Structure

SHR: Synchronization Header
PHR: PHY Header
MPDU: MAC Protocol Data Unit
SFD: Start of Frame Delimiter
FL: Frame Length
MSDU: MAC Service Data Unit
CRC: Cyclic Redundancy Check

(1) Preamble: 4 bytes (8 symbols), 00000000h
(2) SFD: 1 byte (2 symbols), A7h
(3) FL: 1 byte (2 symbols), MPDU length, value written to the BBTXFLEN register
(4) MPDU: Maximum 127-byte data. Data written to transmit RAM is sequentially output.
When the NOCRC bit in the BBTXRXMODE2 register is set to 0 (automatic CRC enabled), CRC data generated in the CRC circuit is automatically added to the last 2 bytes.

- Frame control: 2 bytes (4 symbols)
  - Frame types (bits 2 to 0)
    000b: Beacon frame, 001b: Data frame, 010b: ACK frame
    011b: MAC command frame, 100b-111b: Reserved
  - Security enabled or disabled (bit 3), transmit pending bit (bit 4)
  - ACK request (bit 5), transmission within a PAN (bit 6)
  - Source address mode (bits 10 and 11), destination address mode (bits 14 and 15)
- Sequence number: 1 byte (2 symbols)
- Address information: PANID and addresses of the destination and source
- MSDU (MAC payload): Frame payload
- CRC: Frame CRC queue

25.1.7 Filter Function

25.1.7.1 Address Filter

The ADRSFILEN bit in the BBTXRXMODE3 register can be used to enable or disable the address filter for frames to be captured.
While the address filter is enabled, frames other than those under the following address filter requirements are not stored in receive RAM. Also, no bank 0 or 1 reception complete interrupt request is generated.
While the address filter is disabled, all receive frames are captured. When reception of all frames is completed, a bank 0 or 1 reception complete interrupt request is generated.

25.1.7.2 Address Filter Requirements

If a destination PAN identifier is included in the frame, it should match the BBPANID register or FFFFh.
If a destination short address is included in the frame, it should match the BBSHORTAD register or FFFFh.
If a destination extended address is included in the frame, it should match registers BBENXTENDAD0 to BBENXTENDAD3.
If the frame type is a beacon frame and the BBPANID register is not set to FFFFh, the source PAN identifier should match the BBPANID register. When this register is set to FFFFh, all receive frames are captured.
If the frame type is a data frame or MAC command frame and only the source addressing field is included, the source PAN identifier should match the BBPANID register when the PANCORD bit in the BBTXRXMODE3 register is set to 1 (PAN coordinator).
If the addressing fields and PAN identifier fields of the source and destination are not included, only an ACK frame can be received (ACK frame requirements: frame type = ACK, encrypt bit = 0, and receive frame length = 05h). However, when the address filter is enabled, an ACK frame can be received only within 54 symbols after a frame with an ACK request is transmitted. When an ACK frame is received outside this period, data is discarded and transmission is awaited again.

25.1.7.3 Receive Level Filter

The LVLFILEN bit in the BBTXRXMODE3 register is used to enable or disable the filter for frames to be captured.
While the receive level filter is enabled, only frames with the receive level set in the BBLVLVTH register or higher level can be received.
The value set in the receive level threshold set register or CCA level threshold set register is compared with the value to be stored in the RSSI/CCA result register (the value added with the offset value set in the RSSI offset register).

25.1.8 Interrupts

Table 25.1 lists the interrupt signals from the baseband block.

Table 25.1 Baseband Interrupt List

Interrupt No.	Interrupt Name	Interrupt Generation Conditions
31	BB timer compare 0	An interrupt request is generated when the timer value and the timer compare 0 value match.
28	BB timer compare 1	An interrupt request is generated when the timer value and the timer compare 1 value match.
2	BB timer compare 2	An interrupt request is generated when the timer value and the timer compare 2 value match.
46	Transmission complete	An interrupt request is generated when frame transmission is completed. However, while automatic ACK receive mode is enabled, if an ACK is requested for the transmit frame, no interrupt request is generated when reception is completed; an interrupt request is generated when ACK reception is completed or timed out.
20 (1)	Bank 0 reception complete	An interrupt request is generated when the frame reception at bank 0 is completed. However, while automatic ACK response mode is enabled, if an ACK is requested for the receive frame, no interrupt request is generated when reception is completed; an interrupt request is generated when ACK response is completed.
51 (2)	Bank 1 reception complete	An interrupt request is generated when the frame reception at bank 1 is completed. However, while automatic ACK response mode is enabled, if an ACK is requested for the receive frame, no interrupt request is generated when reception is completed; and an interrupt request is generated when ACK response is completed.
44	Address filter	An interrupt request is generated when an address match is recognized.
30	CCA complete	An interrupt request is generated when a CCA sequence is completed or a CSMA-CA sequence is completed.
48	PLL lock detection	An interrupt request is generated when a PLL lock or unlock is detected. A lock or unlock can be switched by using the PLLINTSEL bit in the BBTXRXMODE4 register. An unlock interrupt is also generated when transmit or receive operation becomes ready while the PLL is not locked.
45	Transmit overrun	A transmit overrun interrupt is generated when the internal transmit counter value is equal to or greater than the write address after transmission starts.
49 (3)	Receive overrun 0	A receive overrun 0 interrupt is generated when data reception restarts at bank 0 while the RCVBANK0 bit in the BBTXRXST0 register is set to 1 (received data present).
47	Receive overrun 1	A receive overrun 1 interrupt is generated when data reception restarts at bank 1 while the RCVBANK1 bit in the BBTXRXST0 register is set to 1 (received data present).
20 (1)	IDLE	An interrupt request is generated after the IDLE startup time has elapsed.
51 (2)	Clock regulator	An interrupt request is generated after the clock regulator startup time has elapsed.
49 (3)	Calibration complete	An interrupt request is generated when calibration is completed.

Notes:
1. Switchable by using the BANK0INTSEL bit in the BBTXRXMODE4 register.
2. Switchable by using the BANK1INTSEL bit in the BBTXRXMODE4 register.
3. Switchable by using the ROR0INTSEL bit in the BBTXRXMODE4 register.

25.1.9 CRC Circuit

The CRC circuit automatically performs operations for transmit frames and receive frames.
A generator polynomial $X^{16} + X^{12} + X^5 + 1$ is used to generate CRC code.
Data is input in 8-bit units, beginning with the start of the payload data, and a 16-bit code is generated.
For transmission, the CRC circuit starts CRC operation from the start address of transmit RAM, and transmits a frame after automatically adding the result which operated up to the (BBTXFLEN register value – 2) address to the last 2 bytes of the transmit frame.
By setting the NOCRC bit in the BBTXRXMODE2 register to 1 (automatic CRC disabled), data in transmit RAM can be transmitted as CRC data instead of the CRC result.
For reception, the CRC circuit starts CRC operation from the start address of receive RAM, and stores the result which operated up to the (BBRXFLEN register value – 2) address and the result which compared with the CRC data of the last 2 bytes of the received frame in the CRC bit in the BBTXRXST0 register. The CRC data of the received frame is stored in receive RAM.

25.1.10 Automatic ACK Response Function

After frame reception is completed, an ACK can be automatically responded by using the AUTOACKEN bit in the BBTXRXMODE0 register.

The conditions for automatic ACK response is automatically resolved in hardware by using received frame control bits.

- CRC result Received frame and the CRC result match
- Address filter enabled
- Frame control bits b2-b0
  Frame types 001b or 011b (data frame or MAC command frame)
- Frame control bit b5
  ACK request 1: Requested
- Frame control bits b11, b10, b15, and b14 (refer to **Table 25.2**)

Table 25.2 Automatic ACK Response Conditions

Frame Control				PAN Coordinator Bit (PANCORD Bit in BBTXRXMODE3 Register)	PANID (BBPANID)	Short Address (BBSHORTAD)	Extended Address (BBEXTENDAD3-0)
b11	b10	b15	b14				
1	0	–	–	–	Match with destination PANID	Match with destination address	×
1	1	–	–	–	Match with destination PANID (1)	×	Match with destination address
0	0	1	0	1	Match with destination PANID	×	×
0	0	1	1	1	Match with destination PANID	×	×

Note:
1. An ACK is responded regardless of the value of BBPANID when the destination PANID = FFFFh.

An ACK frame to be responded is shown in the following figure.

- Frame length (FL): The length is set to 05h regardless of the setting value.
- Sequence number: The received sequence number is transmitted without changes.

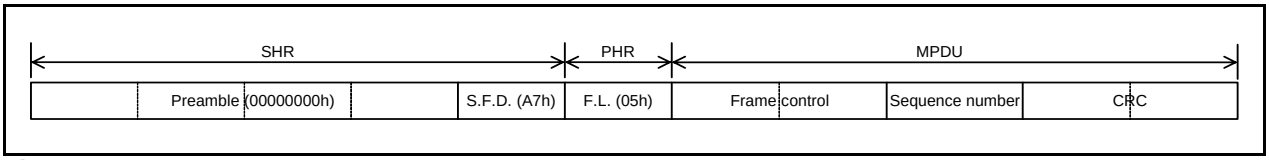


Figure 25.4 ACK Frame

The timing for ACK response varies with nonbeacon mode and beacon mode.
Nonbeacon and beacon modes are selected by using the BEACON bit in the BBTXRXMODE0 register.
In nonbeacn mode, an ACK frame is transmitted 192 µs after frame reception is completed.
In beacon mode, period check begins for a 320µs backoff period after frame reception starts. If reception complete timing takes 192 µs or more before the boundary of a backoff period, an ACK frame is transmitted after the boundary is located (case 1). If the reception complete timing takes 192 µs or less before the boundary of a backoff period, transmission does not start even after the boundary is located, but transmission starts after a delay for the boundary of the next backoff period (case 2).

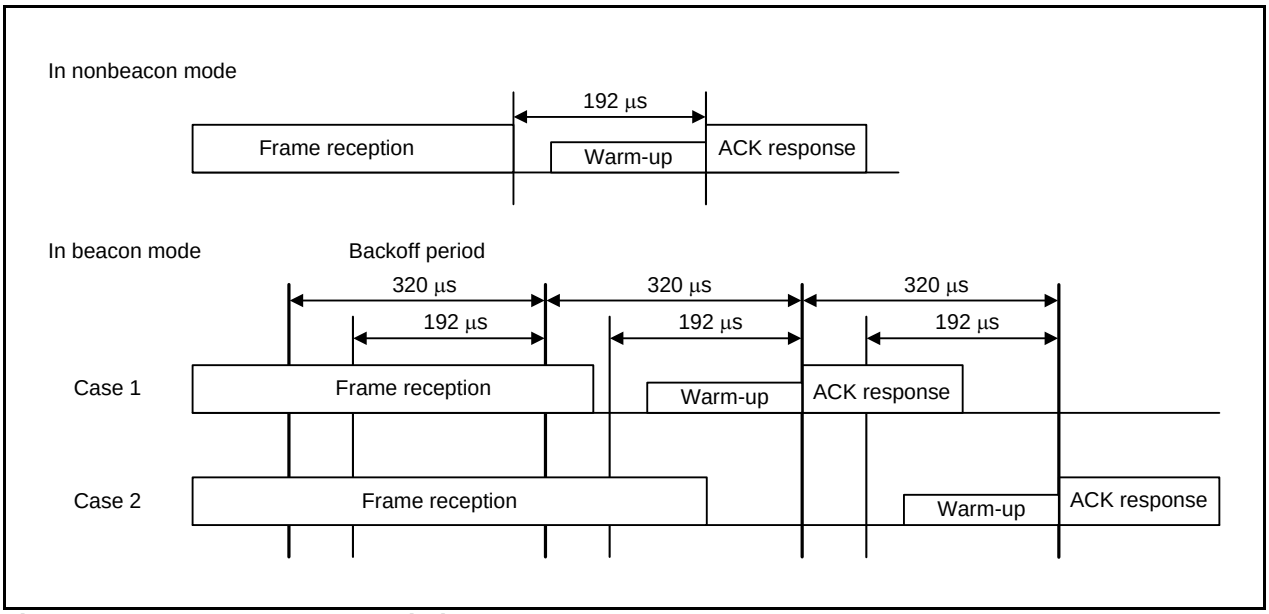


Figure 25.5 ACK Response Timing

Notes:

1. Ongoing ACK response processing is not cancelled even if the AUTOACKEN bit in the BBTXRXMODE0 register is set to 0 (automatic ACK disabled).
2. When performing frame transmission (including automatic ACK reception), disable the automatic ACK response function until the frame transmission is completed.
3. A transmission complete interrupt is generated when ACK response is completed.

25.1.11 Automatic ACK Reception Function

After frame transmission is completed, ACK receive processing can be automatically performed by using the ACKRCVEN bit in the BBTXRXMODE1 register. Frames other than ACK are not received.
The conditions for automatic ACK reception are:

- Frame is transmitted with an ACK request
- Received frame is an ACK frame
- The sequence number of the transmitted frame and the one of the received frame match
- CRC match
- Within 54 symbols after transmission is completed

When all the above conditions are met, a transmission complete interrupt request is generated when ACK reception is completed. Regardless of the address filter enabled or disabled, receive RAM, the BBRXFLEN register, and the CRC bit in the BBTXRXST0 register are not updated.

After transmission is completed, retransmit processing can be performed again from CSMA-CA operation if ACK reception is not confirmed within 54 symbols.
After retransmit processing, the same operation is performed again.
Repeat transmit processing for the number of times set in the RETRN bit in the BBTXRXMODE1 register (default: 3 times). If transmit processing is not required, set 000b in the RETRN bit in the BBTXRXMODE1 register.
To perform retransmit processing, make sure to set the CSMATRNST bit in the BBCSMACON0 register to 1 (transmit processing after CSMA-CA) and the CSMAST bit in the BBCSMACON0 register to 1 (automatic CSMA-CA start) before starting transmit operation.
When ACK reception is completed, or when ACK reception is not confirmed and no ACK is received after retransmit processing is performed for the set number of times (time out), a transmission complete interrupt request is generated.
The TRNRCVSQC bit in the BBTXRXST0 register can be used to confirm whether an ACK has been successfully received or no ACK has been received even after repeating retransmission.

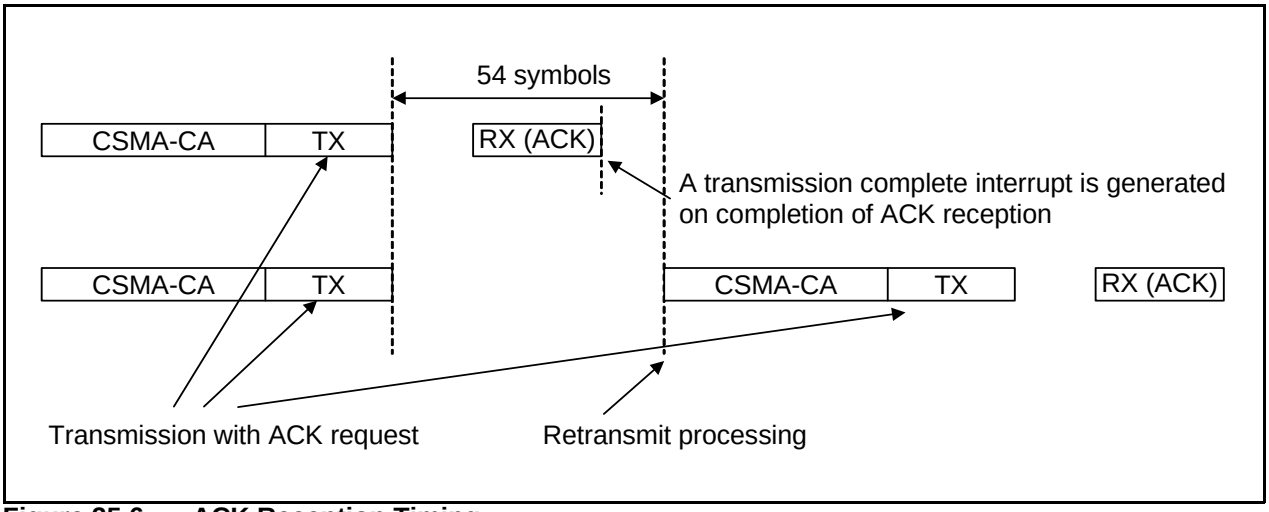


Figure 25.6 ACK Reception Timing

25.1.12 Automatic Reception Switching Function

25.1.12.1 From Transmission to Reception

By setting the AUTORCV0 bit in the BBTXRXMODE0 register to 1 (automatic reception switching function enabled), reception status is automatically selected after frame transmission is completed.
Reception status is enabled 184 μs after transmission is completed.
However, reception status is not entered but IDLE status is entered if CSMA-CA is in busy status during CSMA-CA transmission or if no ACK has been received during transmission with an ACK request.

25.1.12.2 From Reception to Reception

By setting the AUTORCV1 bit in the BBTXRXMODE0 register to 1 (automatic reception switching enabled), reception status is automatically selected after frame reception is completed.
Reception status is enabled 184 μs after reception is completed.
However, ACK response takes priority when ACK response conditions are met while the AUTOACKEN bit in the BBTXRXMODE0 register is 1 (automatic ACK enabled).

Note:

1. After reception is switched while automatic reception switching mode is enabled, reception status remains the same until receive operation is completed (frame reception is completed) even if bits AUTORCV0 and AUTORCV1 in the BBTXRXMODE0 register are set to 0 (automatic reception switching disabled).

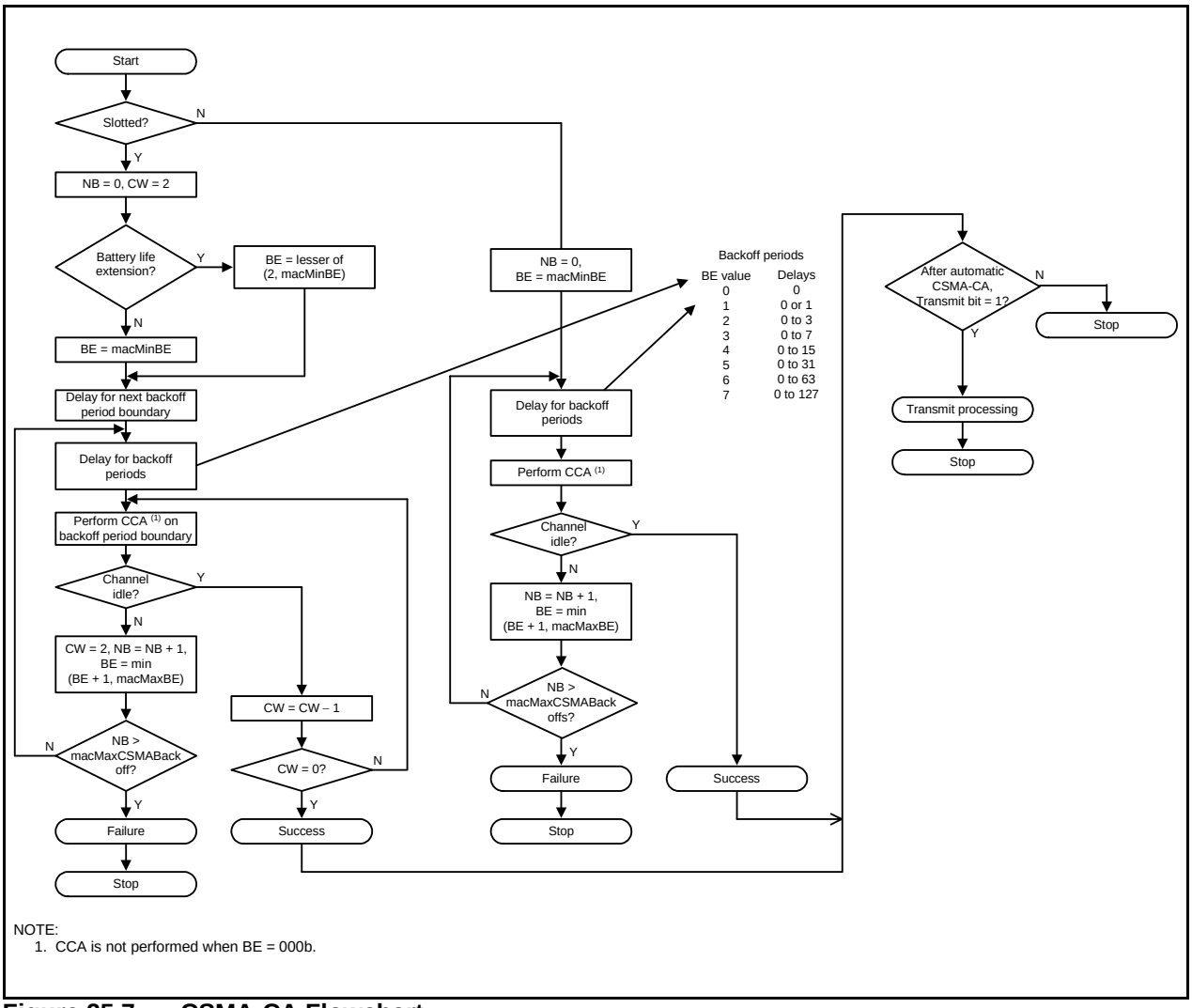
25.1.13 ANTSW Output Switching Function

To control the external power amplifier and others, this function enables the output of the signal which is set to high output when transmitted from the P0_4/ASW pin. Switching to the ASW output can be set by the BBANTSWCON register.

The timing can be set by using the BBANTSWTIMG register.

25.1.14 Automatic CSMA-CA Function

By setting CSMAST bit in the BBCSMACON0 register 1 (automatic CSMA-CA start), the CSMA-CA flowchart can be automatically performed.
Set the CCA threshold level in the BBCCAVTH register.
Registers BBCSMACON1 and BBCSMACON2 can be used to set each variable.
Upon completion of CSMA-CA operation, the result can be simultaneously stored in the CSMACA bit in the BBTXRXST0 register, and a CSMA-CA interrupt can be generated.
By having set the CSMATRNST bit in the BBCSMACON0 register to 1 (transmit processing after CSMA-CA), transmit processing can be automatically proceeded if the CSMA-CA check result is TRUE.
Before performing an automatic CSMA-CA start, make sure to allow the wait time set in the BBIDLEWAIT register to elapse after setting to IDLE status.
When the CSMAST bit in the BBCSMACON0 register is set to 1 (automatic CSMA-CA start) while the BEMIN bit in the BBCSMACON1 register is set to 000b, processing starts from transmission without performing CSMA-CA operation. When the automation ACK reception function is enabled, if ACK reception is not confirmed within 54 symbols after transmission is completed, retransmit processing is performed from transmit operation for the number of times set in the RETRN bit in the BBBBTXRXMODE1 register. When the RETRN bit in the BBTXRXMODE1 register is set to 000b, retransmit processing is not performed.



NOTE:
1. CCA is not performed when BE = 000b.

Figure 25.7 CSMA-CA Flowchart

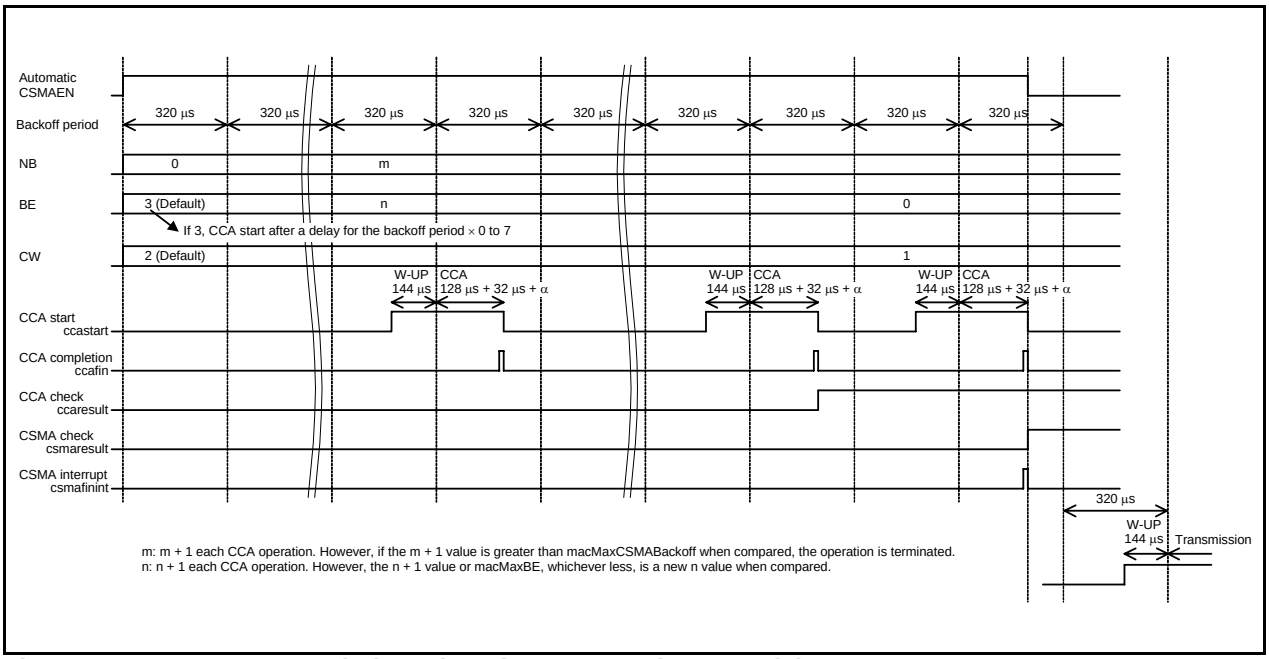


Figure 25.8 CSMA-CA Timing Chart (Beacon Mode Example)

25.1.15 State Transitions

Figure 25.9 shows State Transitions.

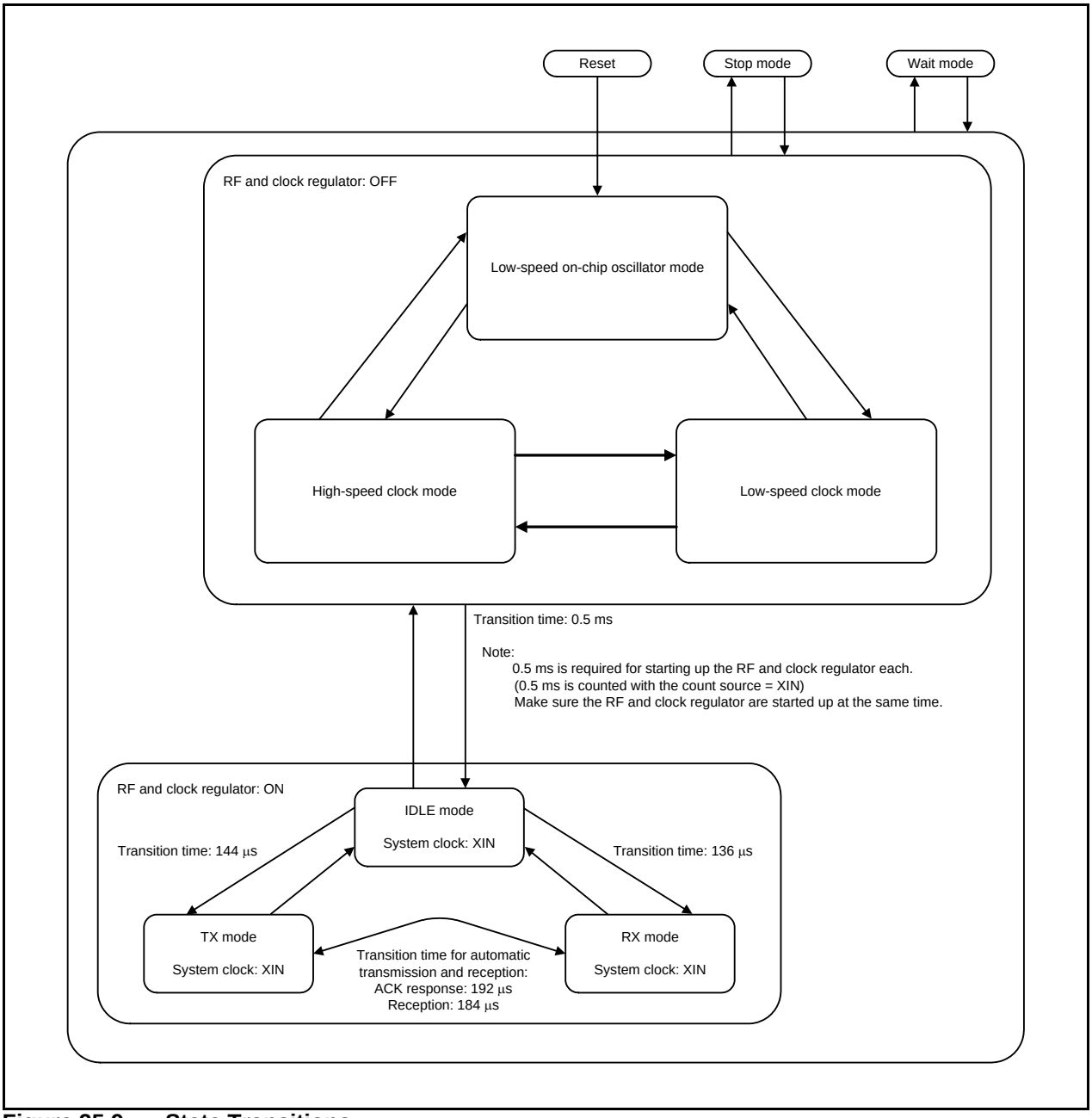


Figure 25.9 State Transitions

25.2 Baseband Associated Registers

Baseband associated registers are shown below.

25.2.1 Baseband Control Register (BBCON)

Address 2D00h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	BBEN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BBEN	Baseband enable bit	0: Baseband functions disabled (stop) 1: Baseband functions enabled	R/W
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

BBEN Bit (Baseband Enable Bit)

This register controls enabling or disabling of the baseband functions. Setting the BBEN bit to 1 enables the baseband functions.

Access to the baseband associated registers when this bit is 1.

Setting the BBEN bit to 0 initializes any processing during communication, but the setting value of each register is retained. Other processing such as the automatic ACK response and automatic reception switching functions are also cancelled.

Make sure to set the RFPWRON bit in the BBRFCON register to 0 (RF power OFF) before setting the BBEN bit to 0.

25.2.2 Transmit/Receive Reset Register (BBTXRXRST)

Address 2D01h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	RFRESET	RFSTOP
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RFSTOP	RF communication stop bit	0: RF communication enabled 1: RF communication stopped	R/W
b1	RFRESET	RF reset bit	0: Baseband function registers retain values 1: Baseband associated registers are reset	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

RFSTOP Bit (RF Communication Stop Bit)

Setting the RFSTOP bit to 1 enables the cancellation of processing during transmission, reception, CCA, or calibration (IDLE status after cancellation). Processing such as the automatic ACK response and automatic reception switching mode functions are also cancelled. The RFSTOP bit is automatically cleared to 0. However, the setting value of each register is retained.

RFRESET Bit (RF Reset Bit)

Setting the RFRESET bit to 1 initializes all baseband associated registers. As all control signals are initialized, communication is also cancelled as with the RFSTOP bit. The RFRESET bit is automatically cleared to 0. This bit can also be set regardless of the value of the BBEN bit in the baseband control register.

25.2.3 Transmit/Receive Mode Register 0 (BBTXRXMODE0)

Address 2D02h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	BEACON	BATLIFEEXT	AUTORCV1	AUTORCV0	AUTOACKEN	—	CCACOND
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CCACOND	CCA type bit	0: Normal 1: CCA/ED	R/W
b1	—	Reserved bit	Set to 0.	R/W
b2	AUTOACKEN	Auto ACK mode enable bit	0: Automatic ACK disabled 1: Automatic ACK enabled	R/W
b3	AUTORCV0	Auto receive switch mode 0 enable bit (TX → RX)	0: Automatic reception switching disabled 1: Automatic reception switching enabled	R/W
b4	AUTORCV1	Auto receive switch mode 1 enable bit (RX → RX)	0: Automatic reception switching disabled 1: Automatic reception switching enabled	R/W
b5	BATLIFEEXT	Battery life extension mode bit	0: Disabled 1: Enabled	R/W
b6	BEACON	Beacon mode bit	0: Nonbeacon mode 1: Beacon mode	R/W
b7	—	Reserved bit	Set to 0.	R/W

CCACOND Bit (CCA Type Bit)

To execute CCA or ED, set the CCACOND bit to 1.

AUTOACKEN Bit (Auto ACK Mode Enable Bit)

The AUTOACKEN bit can be used to select whether to perform automatic ACK response operation after reception is completed.

AUTORCV0 Bit (Auto Receive Switch Mode 0 Enable Bit)

The AUTORCV0 bit can be used to automatically transit to reception status after transmission is completed.

AUTORCV1 Bit (Auto Receive Switch Mode 1 Enable Bit)

The AUTORCV1 bit can be used to automatically transit to reception status after reception is completed. However, ACK response takes priority when ACK response conditions are met while the AUTOACKEN bit is 1 (automatic ACK enabled).

BATLIFEEXT Bit (Battery Life Extension Mode Bit)

The BATLIFEEXT bit can be used to enable the battery life extension mode for the branch conditions used in CSMA-CA processing shown in Figure 25.7.

BEACON Bit (Beacon Mode Bit)

The BEACON bit can be used to specify the operating mode for ACK frame response or CSMA-CA timing.

25.2.4 Transmit/Receive Mode Register 1 (BBTXRXMODE1)

Address 2D03h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	CCASEL	—	—	—	ACKRCVEN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ACKRCVEN	Auto ACK receive mode bit	0: Automatic ACK reception disabled 1: Automatic ACK reception enabled	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	CCASEL	CCA result select bit	0: CCA/ED 1: RSSI	R/W
b5	—	Reserved bits	Set to 0.	R/W
b6	—			
b7	—			

ACKRCVEN Bit (Auto ACK Receive Mode Bit)

The ACKRCVEN bit can be used to select whether to perform automatic receive operation.

CCASEL Bit (CCA Result Select Bit)

The CCASEL bit can be used to select the CCA/ED or RSSI value when reading the RSSI/CCA result register.

25.2.5 Receive Frame Length Register (BBRXFLEN)

Address 2D04h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RXFLEN	RXFLEN	RXFLEN	RXFLEN	RXFLEN	RXFLEN	RXFLEN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RXFLEN	Receive frame length (1)	Indicates the frame length value for reception.	R
b1	RXFLEN			
b2	RXFLEN			
b3	RXFLEN			
b4	RXFLEN			
b5	RXFLEN			
b6	RXFLEN			
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Note:
1. These bits correspond to the receive RAM bank.

RXFLEN Bit (Receive Frame Length)

This register stores the frame length value for reception. When reading this register, the frame length value corresponding to the receive RAM bank specified with the RCVBANKSEL bit in the BBTXRXMODE3 register is read.

The frame length value is stored when frame reception starts, and it is retained until the next frame reception starts. However, the value is updated when an address match is recognized while the address filter is enabled.

If the receive frame length is less than or equal to 04h, the frame reception is not accepted. In this case, the receive frame length value is not updated. Also, no reception complete interrupt is generated.

25.2.6 Receive Data Counter Register (BBRXCOUNT)

Address 2D05h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	RXCOUNT	RXCOUNT	RXCOUNT	RXCOUNT	RXCOUNT	RXCOUNT	RXCOUNT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RXCOUNT	Receive data counter	Indicates the data counter value for reception.	R
b1	RXCOUNT			
b2	RXCOUNT			
b3	RXCOUNT			
b4	RXCOUNT			
b5	RXCOUNT			
b6	RXCOUNT			
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

RXCOUNT Bit (Receive Data Counter)

This register indicates the receive data counter value for reception. It can be used to confirm what bytes of data has been received. The value is cleared to 00h when frame reception stops.

25.2.7 RSSI/CCA Result Register (BBRSSICCARSLT)

Address 2D06h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RSSICCARSLT	RSSICCARSLT	RSSICCARSLT	RSSICCARSLT	RSSICCARSLT	RSSICCARSLT	RSSICCARSLT	RSSICCARSLT
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RSSICCARSLT	RSSI/CCA result data (1)	Indicates the result data of RSSI/CCA.	R
b1	RSSICCARSLT			
b2	RSSICCARSLT			
b3	RSSICCARSLT			
b4	RSSICCARSLT			
b5	RSSICCARSLT			
b6	RSSICCARSLT			
b7	RSSICCARSLT			

Note:
1. These bits correspond to the receive RAM bank.

RSSICCARSLT Bit (RSSI/CCA Result Data)

This register stores the result data of CCA/ED or RSSI.
The CCA/ED or RSSI value can be switched by using the CCASEL bit in the BBTXRXMODE1 register. When reading the RSSI value, the result corresponding the receive RAM bank specified with the RCVBANKSEL bit in the BBTXRXMODE3 register is read.
The read data is indicated by two's complement in dBm units (example: 9Eh is indicated as –98 dBm).
Also, refer to **25.2.31 RSSI Offset Register (BBRSSIOFS)**.

25.2.8 Transmit/Receive Status Register 0 (BBTXRXST0)

Address 2D07h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RCVBANKST	RCVPEND	RCVBANK1	RCVBANK0	TRNRCVSQC	CSMACA	CRC	CCA
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CCA	CCA check result bit	0: Channel clear 1: Channel busy	R
b1	CRC	CRC check result bit (1)	0: TRUE 1: FALSE	R
b2	CSMACA	CSMA-CA check result bit	0: TRUE 1: FALSE	R
b3	TRNRCVSQC	Transmit/receive operation complete check result bit	0: TRUE 1: FALSE	R
b4	RCVBANK0	Receive bank 0 status bit	0: Reception enabled 1: Received data present	R/W
b5	RCVBANK1	Receive bank 1 status bit	0: Reception enabled 1: Received data present	R/W
b6	RCVPEND	Receive pending bit	0: No pending 1: Pending	R
b7	RCVBANKST	Receive bank pointer bit	0: Bank 0 1: Bank 1	R

Note:
1. This bit corresponds to the receive RAM bank.

CCA Bit (CCA Check Result Bit)

This register stores the CCA check result in the CCA bit.

CRC Bit (CRC Check Result Bit)

The CRC check result is stored in the CRC bit. When reading this bit, the CRC result corresponding to the receive RAM bank specified with the RCVBANKSEL bit in the BBTXRXMODE3 register is read.

CSMACA Bit (CSMA-CA Check Result Bit)

The CSMA-CA check result is stored in the CSMACA bit.

TRNRCVSQC Bit (Transmit/Receive Operation Complete Check Result Bit)

The TRNRCVSQC bit is used to store the check result on the completion of a transmit/receive operation sequence (CSMA-CA → transmission → ACK reception → retransmission → ACK reception…). If no ACK is received after repeating retransmission for the number of the set times, the TRNRCVSQC bit is set to 1 (false).

RCVBANK0 Bit (Receive Bank 0 Status Bit)
RCVBANK1 Bit (Receive Bank 1 Status Bit)

Bits RCVBANK0 and RCVBANK1 are used as the flags for capturing a frame in receive banks 0 and 1, respectively.
These bits are automatically set to 1 when frame reception starts. When the address filter is enabled, these bits are set to 1 at the same time an address filter interrupt is generated. Then, they are cleared to 0 by software after the data in the receive RAM is read. Only 0 can be written to. If reception is performed again while these bits are 1 and data is written to each receive RAM, a receive overrun interrupt is generated.

RCVPEND Bit (Receive Pending Bit)

The RCVPEND bit is used to store the value of the pending bit when an ACK frame is received.

RCVBANKST Bit (Receive Bank Pointer Bit)

The RCVBANKST bit can be used to confirm the receive RAM bank in which the last frame that has been received. After a reset, this bit indicates 1 once it is initialized.

25.2.9 Transmit Frame Length Register (BBTXFLEN)

Address 2D08h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	TXFLEN	TXFLEN	TXFLEN	TXFLEN	TXFLEN	TXFLEN	TXFLEN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXFLEN	Transmit frame length	Indicates the frame length for transmission	R/W
b1	TXFLEN			
b2	TXFLEN			
b3	TXFLEN			
b4	TXFLEN			
b5	TXFLEN			
b6	TXFLEN			
b7	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

TXFLEN Bit (Transmit Frame Length)

The frame length value for transmission is written to this register. The total of the payload data length and CRC length (2 bytes) is set as the frame length value. While the transmit frame length is equal to or less than 04h, do not set 1 in the TRNTRG bit in the BBTXRXCON register or the CSMAST bit in the BBCSMACON0 register (transmission start or automatic CSMA-CA start).

Only the ACK automatic response function enables the transmission of an ACK frame regardless of the transmit frame length.

25.2.10 Transmit/Receive Mode Register 2 (BBTXRXMODE2)

Address 2D09h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RETRN	RETRN	RETRN	RETRN	—	FLMPENDST	FLMPEND	NOCRC
After Reset	0	0	1	1	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	NOCRC	Auto CRC disable bit	0: Enabled 1: Disabled	R/W
b1	FLMPEND	Frame pending bit	0: No frame pending 1: Frame pending	R/W
b2	FLMPENDST	Frame pending status bit (1)	0: ACK frame response with no frame pending 1: ACK frame response with frame pending	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	RETRN	Retransmit counter	Set 0000b to 1000b	R/W
b5	RETRN			
b6	RETRN			
b7	RETRN			

Note:
1. This bit corresponds to the receive RAM bank.

NOCRC Bit (Auto CRC Disable Bit)

For transmission, the NOCRC bit can be used to select whether to add the CRC result automatically or only to transmit data in transmit RAM.

FLMPEND Bit (Frame Pending Bit)

The FLMPEND bit can be used to specify the value to be set in the pending bit in an ACK frame. The information of this bit is automatically included in the automatic ACK response frame.

FLMPENDST Bit (Frame Pending Status Bit)

The FLMPEMDST bit indicates whether an ACK frame is responded with pending or without pending for automatic ACK response. This bit is updated at the same time as a bank 0/1 reception complete interrupt request is generated when ACK response is completed.
The FLMPEMDST bit reflects the result of automatic ACK response performed for each bank which received a frame with an ACK request. When reading this bit, it returns the frame pending information when an ACK is responded with the receive RAM data in the bank, which is selected with the RCVBANKSEL bit in the BBTXRXMODE3 register.

RETRN Bit (Retransmit Counter)

The RETRN bit can be used to set the number of retransmit processing if there is no ACK response while automatic ACK receive mode is enabled. 0000b to 1000b can be set.

25.2.11 Transmit/Receive Mode Register 3 (BBTXRXMODE3)

Address 2D0Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	RCVOVERWREN	RCVBANKSEL	LVLFILEN1	LVLFILEN0	PANCORD	ADRSFILEN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ADRSFILEN	Address filter enable bit	0: Address filter disabled 1: Address filter enabled	R/W
b1	PANCORD	PAN coordinator bit	0: Non PAN coordinator 1: PAN coordinator	R/W
b2	LVLFILEN0	Receive level filter enable bit	b3 b2 0 0: Level filter disabled 0 1: Do not set. 1 0: Do not set. 1 1: Level filter enabled	R/W
b3	LVLFILEN1			
b4	RCVBANKSEL	Receive bank select bit	0: Bank 0 1: Bank 1	R/W
b5	RCVOVERWREN	Receive RAM overwrite enable bit	0: Overwrite disabled 1: Overwrite enabled	R/W
b6	—	Reserved bits	Set to 0.	—
b7	—			

ADRSFILEN Bit (Address Filter Enable Bit)

The ADRSFILEN bit can be used to enable the address filter for reception.

PANCORD Bit (PAN Coordinator Bit)

The PANCORD bit can use used to set whether or not to receive a receive frame with no destination address (whether a PAN coordinator or not), as a requirement for the address filter.

Bits LVLFILEN0 and LVLFILEN1 (Receive Level Filter Enable Bit)

Bits LVLFILEN0 and LVLFILEN1 can be used to set the reception of only input frames higher than or equal to the threshold level set in the BBLVLVTH register.

RCVBANKSEL Bit (Receive Bank Select Bit)

The RCVBANKSEL bit is used to specify the bank for read accesses associated with receive RAM.

RCVOVERWREN Bit (Receive RAM Overwrite Enable Bit)

The RCVOVERWREN bit can be used to control the overwriting to receive RAM. While this bit is 0, if bits RCVBANK0 and RCVBANK1 in the BBTXRXMODE0 register are set to 1 (received data present), received data is not overwritten when a write access occurs to each receive RAM. However, a receive overrun 0/1 interrupt is generated.

While the RCVOVERWREN bit is 1, if bits RCVBANK0 and RCVBANK1 in the BBTXRXMODE0 register are set to 1 (received data present), received data is overwritten when a write access occurs to each receive RAM. However, a receive overrun 0/1 interrupt is generated.

25.2.12 Receive Level Threshold Set Register (BBLVLVTH)

Address 2D0Bh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	LVLVTH	LVLVTH	LVLVTH	LVLVTH	LVLVTH	LVLVTH	LVLVTH	LVLVTH
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	LVLVTH	Receive level threshold	Sets the threshold value for the receive level filter function.	R/W
b1	LVLVTH			
b2	LVLVTH			
b3	LVLVTH			
b4	LVLVTH			
b5	LVLVTH			
b6	LVLVTH			
b7	LVLVTH			

LVLVTH Bit (Receive Level Threshold)

This register is used to set the threshold value for the receive level filter function. Set the value to two's complement in dBm units (example: 9Eh is indicated as –98 dBm).
The value set in the receive level threshold set register is compared with the value to be stored in the RSSI/CCA result register (the value added with the offset value set in the RSSI offset register).

25.2.13 Transmit/Receive Control Register (BBTXRXCON)

Address 2D0Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	CCATRG	TRNTRG	RCVTRG
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RCVTRG	Receive trigger bit (1)	0: No action 1: Reception start	W
b1	TRNTRG	Transmit trigger bit (1)	0: No action 1: Transmission start	W
b2	CCATRG	CCA trigger bit (1)	0: No action 1: CCA start	W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. Make sure to set these bits in IDLE status. Do not set two or more bits to 1 simultaneously. These bits are automatically cleared to 0 when transmission/reception or CCA is completed. To cancel transmission/reception or CCA in progress, use the RFSTOP bit in the BBTXRXCON register.

RCVTRG Bit (Receive Trigger Bit)

Setting the RCVTRG bit to 1 starts the warming up of the RF block, and reception status is enabled 136 μs later.

TRNTRG Bit (Transmit Trigger Bit)

Setting the TRNTRG bit to 1 starts the warming up of the RF block, and transmission starts 144 μs later.

CCATRG Bit (CCA Trigger Bit)

Setting the CCATRG bit to 1 starts the warming up of the RF block, and CCA operation starts 136 μs later.

25.2.14 CSMA Control Register 0 (BBCSMACON0)

Address 2D0Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	CSMATRNST	CSMAST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CSMAST	Auto CSMA-CA start bit	0: No action 1: Automatic CSMA-CA start	W
b1	CSMATRNST	Auto transmit bit after CSMA-CA	0: No action 1: Transmit processing after CSMA-CA	R/W
b2	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

CSMAST Bit (Auto CSMA-CA Start Bit)

Setting the CSMAST bit to 1 starts CSMA-CA operation. Make sure to set this bit in IDLE status.
Also, this bit is automatically cleared to 0 when CSMA-CA operation is completed. Setting this bit to 0 does not allow any write operations.

CSMATRNST Bit (Auto Transmit Bit After CSMA-CA)

Setting the CSMATRNST bit to 1 allows transmit processing to be automatically performed if the result is TRUE when CSMA-CA operation is completed.
To cancel CSMA-CA operation in progress, use the RFSTOP bit in the BBTXRXRST register.

25.2.15 CCA Level Threshold Set Register (BBCCAVTH)

Address 2D0Eh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CCAVTH	CCAVTH	CCAVTH	CCAVTH	CCAVTH	CCAVTH	CCAVTH	CCAVTH
After Reset	1	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CCAVTH	CCA threshold	Sets the threshold level of CCA.	R/W
b1	CCAVTH			
b2	CCAVTH			
b3	CCAVTH			
b4	CCAVTH			
b5	CCAVTH			
b6	CCAVTH			
b7	CCAVTH			

CCAVTH Bit (CCA Threshold)

This register is used to set the threshold level for CCA check. Set the value to two’s complement in dBm units (example: 9Eh is indicated as –98 dBm).

The value set in the CCA level threshold set register is compared with the value to be stored in the RSSI/CCA result register (the value added with the offset value set in the RSSI offset register).

25.2.16 Transmit/Receive Status Register 1 (BBTXRXST1)

Address 2D0Fh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	UNLOCKST
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	UNLOCKST	Unlock receive status bit (1)	0: Normal (no unlock) 1: Abnormal (unlock occurred)	R
b1	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. This bit corresponds to the receive RAM bank.

UNLOCKST Bit (Unlock Receive Status Bit)

The UNLOCKST bit can be used to check whether a PLL unlock has occurred during reception.
This bit is read as the result corresponding to the receive RAM bank specified with the RCVBANKSEL bit in the BBTXRXMODE3 register.

25.2.17 RF Control Register (BBRFCON)

Address 2D10h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	XINREGSEL	XINPWRON	RFPWRON
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RFPWRON	RF power ON bit (1)	0: OFF 1: RF power ON (IDLE)	RW
b1	XINPWRON	XIN power ON bit (1)	0: OFF 1: XIN power ON	RW
b2	XINREGSEL	XIN regulator switch bit (1)	0: MCU regulator 1: Clock regulator	RW
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—			
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Note:
1. Set these bits to 1 simultaneously.

RFPWRON Bit (RF Power ON Bit)

The RFPWRON bit is used to control powering ON of the RF block.
After setting 1 in the RFPWRON bit, IDLE status is selected after the wait time set in the BBIDLEWAIT register has elapsed. The wait time set in the BBIDLEWAIT register is automatically counted with XIN as the count source, and an IDLE interrupt request is generated after the startup time to IDLE status has been waited.
From OFF status, make sure to transit to CCA, reception, or transmission status via this IDLE status. While in IDLE status, set 1 (operation start) in bits RCVTRG, TRNTRG, and CCATRG in the BBTXRXCON register, and the CSMAST bit in the BBCSMACON0 register.

XINPWRON Bit (XIN Power ON Bit)

After setting 1 in the XINPWRON bit, the startup of the clock regulator is completed after the wait time set in the BBIDLEWAIT register has elapsed. The wait time set in the BBIDLEWAIT register is automatically counted with XIN as the count source, and a clock regulator interrupt request is generated after the regulator startup time has been waited.

XINREGSEL Bit (XIN Regulator Switch Bit)

The XINREGSEL bit can be used to switch the XIN power supply to a stable power supply.

25.2.18 Transmit/Receive Mode Register 4 (BBTXRXMODE4)

Address 2D11h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	ROR0INTSEL	BANK1INTSEL	BANK0INTSEL	UNLOCKSTPR	UNLOCKSTPT	PLLINTSEL	CCAINTSEL
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CCAINTSEL	CCA interrupt select bit	0: When CCA sequence is completed 1: When CSMA-CA sequence is completed	RW
b1	PLLINTSEL	PLL lock detection select bit	0: Unlock detected 1: Lock detected	RW
b2	UNLOCKSTPT	Operation stop enable bit after transmission unlock detection	0: Disabled (all frames transmitted) 1: Stop after unlock detection	RW
b3	UNLOCKSTPR	Operation stop enable bit after reception unlock detection	0: Disabled (all frames received) 1: Stop after unlock detection → transit to reception standby	RW
b4	BANK0INTSEL	Bank 0 reception complete/IDLE interrupt select bit	0: Bank 0 reception complete interrupt 1: IDLE interrupt	RW
b5	BANK1INTSEL	Bank 1 reception complete/clock regulator interrupt select bit	0: Bank 1 reception complete interrupt 1: Clock regulator interrupt	RW
b6	ROR0INTSEL	Receive overrun 0/calibration complete interrupt select bit	0: Receive overrun 0 1: Clock regulation complete interrupt	RW
b7	—	Reserved bit	Set to 0.	RW

CCAINTSEL Bit (CCA Interrupt Select Bit)

The CCAINTSEL bit can be used to select either when a CCA sequence is completed or when a CSMA-CA sequence is completed as the generation source of a CCA interrupt.

PLLINTSEL Bit (PLL Lock Detection Select Bit)

The PLLINTSEL bit can be used to select either when an unlock is detected or when a lock is detected as the generation source of a PLL lock detection interrupt.

UNLOCKSTPT Bit (Operation Stop Enable Bit After Transmission Unlock Detection)

The UNLOCKSTPT bit can be used to set the operation when an unlock occurs during transmission. When this bit is 0, frame transmission continues even if an unlock occurs. When this bit is 1, transmit operation stops if an unlock occurs. Make sure to set the PLLINTSEL bit to 0 (unlock detected) when using this function. As IDLE status is selected after operation stops, set to transmission or reception again.

UNLOCKSTPR Bit (Operation Stop Enable Bit After Reception Unlock Detection)

The UNLOCKSTPR bit can be used to set the operation if an unlock occurs during reception. When this bit is 0, frame reception is not terminated even if an unlock occurs and the reception continues until its end. When this bit is 1, reception is terminated if an unlock occurs and the status transits to reception standby. Whether an unlock has occurred or not during reception can be confirmed by reading the UNLOCKST bit in the BBTXRXST1 register, which is set when reception is completed. Make sure to set the PLLINTSEL bit to 0 (unlock detected) when using this function.

BANK0INTSEL Bit (Bank 0 Reception Complete/Idle Interrupt Select Bit)

The BANK0INTSEL bit can be used to select either a bank 0 reception complete interrupt or an IDLE interrupt.

BANK1INTSEL Bit (Bank 1 Reception Complete/Clock Regulator Interrupt Select Bit)

The BANK1INTSEL bit can be used to select either a bank 1 reception complete interrupt or a clock regulator interrupt.

ROR0INTSEL Bit (Receive Overrun 0/Calibration Complete Interrupt Select Bit)

The ROR0INTSEL bit can be used to select either a receive overrun 0 interrupt or a calibration complete interrupt.

25.2.19 CSMA Control Register 1 (BBCSMACON1)

Address 2D12h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CW	CW	BEMIN	BEMIN	BEMIN	NB	NB	NB
After Reset	1	0	0	1	1	1	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	NB	NB bit	Sets the value of macMaxCSMABackoff. Set 000b to 101b.	RW
b1	NB			
b2	NB			
b3	BEMIN	BEMIN bit	Sets the value of macMinBE.	R/W
b4	BEMIN			
b5	BEMIN			
b6	CW	CW bit	Sets the value of CW.	RW
b7	CW			

NB Bit

The NB bit is used to set the value of macMaxCSMABackoff shown in Figure 25.7. (The initial value is 04h.) 000b to 101b can be set.

BEMIN Bit

The BEMIN bit is used to set the value of macMinBE shown in Figure 25.7. (The initial value is 03h.)

CW Bit

The CW bit is used to set the value of CW shown in Figure 25.7. (The initial value is 02h.)

25.2.20 CSMA Control Register 2 (BBCSMACON2)

Address 2D13h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	BEMAX	BEMAX	BEMAX
After Reset	0	0	0	0	0	1	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	BEMAX	BEMAX bit	Sets the value of macMaxBE.	RW
b1	BEMAX			
b2	BEMAX			
b3	—	Reserved bits	Set to 0.	R/W
b4	—			
b5	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b6	—			
b7	—			

BEMAX Bit

The BEMAX bit is used to set the value of macMaxBE shown in Figure 25.7. (The initial value is 05h.)

25.2.21 PAN Identifier Register (BBPANID)

This register is for setting PAN identifiers. It consists of 16 bits and is used to detect a match with the PAN identifier of a receive frame.

Address 2D15h to 2D14h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15 to b0	PAN identifier	R/W

25.2.22 Short Address Register (BBSHORTAD)

This register is for setting short addresses. It consists of 16 bits and is used to detect a match with the short address of a receive frame.

Address 2D17h to 2D16h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15 to b0	Short address	R/W

25.2.23 Extended Address Register (BBEXTENDAD0, BBEXTENDAD1, BBEXTENDAD2, BBEXTENDAD3)

This register is for setting extended addresses. It consists of 64 bits (16 bits × 4) and is used to detect a match with the extended address of a receive frame.

Address 2D19h to 2D18h (BBEXTENDAD0), 2D1Bh to 2D1Ah (BBEXTENDAD1), 2D1Dh to 2D1Ch (BBEXTENDAD2), 2D1Fh to 2D1Eh (BBEXTENDAD3)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15 to b0	Extended address register BBEXTENDAD0: Extended address bits 15 to 0 BBEXTENDAD1: Extended address bits 31 to 16 BBEXTENDAD2: Extended address bits 47 to 32 BBEXTENDAD3: Extended address bits 63 to 48	R/W

25.2.24 Timer Read-Out Registers 0 and 1 (BBTIMEREAD0, BBTIMEREAD1)

These registers are for reading the current count value from the 26-bit timer.
When reading the timer count value, read the BBTIMEREAD0 register (lower byte) first.
When bits 7 to 0 or bits 15 to 8 in the BBTIMEREAD0 register (or both) are read, the count value of bits 25 to 16 in the BBTIMEREAD1 register (higher byte) is latched.
If the BBTIMEREAD1 register is read first, note the BBTIMEREAD0 register is not latched.
After the BBTIMEREAD0 register is read, its value is not updated even if this register is read again without reading the BBTIMEREAD1 register, and the previously read value is read.

Address 2D21h to 2D20h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15 to b0	Timer read-out register 0 BBTIMEREAD0: Lower bits (15 to 0) in the 26-bit timer	R

Address 2D23h to 2D22h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b9 to b0	Timer read-out register 1 BBTIMEREAD1: Higher bits (bits 25 to 16) in the 26-bit timer	R
b15 to b10	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—

25.2.25 Timer Compare i (i = 0 to 2) Register (BBTCOMPiREG0, BBTCOMPiREG1) (i = 0 to 2)

This register is for performing comparisons with the 26-bit timer.
Three channels are integrated and 26-bit comparison is performed in each channel.

Address 2D25h to 2D24h (BBTCOMP0REG0), 2D29h to 2D28h (BBTCOMP1REG0), 2D2Dh to 2D2Ch (BBTCOMP2REG0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15 to b0	Timer compare i register 0 BBTCOMPiREG0: Lower bits (bits 15 to 0) in the 26-bit compare i = 0 to 2	R/W

Address 2D27h to 2D26h (BBTCOMP0REG1), 2D2Bh to 2D2Ah (BBTCOMP1REG1), 2D2Fh to 2D2Eh (BBTCOMP2REG1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b9 to b0	Timer compare i register 1 BBTCOMPiREG1: Higher bits (bits 25 to 16) in the 26-bit compare i = 0 to 2	R/W
b15 to b10	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—

25.2.26 Time Stamp Registers 0 and 1 (BBTSTAMP0, BBTSTAMP1)

These registers are for storing the timer value when frame reception is completed.
The count value on completion of reception is automatically stored in time stamp registers.
The time stamp value is retained until the next reception is completed.
When these registers are read, the time stamp value corresponding to the receive RAM bank specified with the RCVBANKSEL bit in the BBTXRXMODE3 register is read.

Address 2D31h to 2D30h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b15 to b0	Time stamp register 0 BBTSTAMP0: Lower bits (bits 15 to 0) of the 26-bit stamp value (1)	R

Address 2D33h to 2D32h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Function	R/W
b9 to b0	Time stamp register 1 BBTSTAMP1: Higher bits (bits 25 to 16) of the 26-bit stamp value (1)	R
b15 to b10	Nothing is assigned. If necessary, set to 0. When read, the content is 0.	—

Note:
1. These bits correspond to the receive RAM bank.

25.2.27 Timer Control Register (BBTIMECON)

Address 2D34h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	COMP0TRG	TIMEEN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TIMEEN	Timer count enable bit	0: Timer count stops 1: Timer count enabled	R/W
b1	COMP0TRG	COMP0 transmit trigger enable bit	0: Transmit trigger disabled 1: Transmit trigger enabled	R/W
b2	—	Reserved bit	Set to 0.	R/W
b3	—	Reserved bit	Set to 0.	R/W
b4	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b5	—			
b6	—			
b7	—			

TIMEEN Bit (Timer Count Enable Bit)

The TIMEEN bit is used to control the count operation of the 26-bit timer.
Setting this bit to 1 enables the timer count. Setting this bit to 0 stops the timer count, and also initializes the timer count value to 0000000h.

COMP0TRG Bit (COMP0 Transmit Trigger Enable Bit)

The COMP0TRG bit can be used to start RF transmission when the timer compare 0 value and the timer value match. Warming up begins right after the match, and transmission starts 144 µs later. Make sure to perform operations in IDLE status.

25.2.28 Backoff Period Register (BBBOFFPROD)

Address 2D35h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	BOFFPRODEN	BOFFPROD	BOFFPROD	BOFFPROD	BOFFPROD	BOFFPROD	BOFFPROD	BOFFPROD
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	BOFFPROD	Backoff period bit	Sets the backoff period value.	R/W
b1	BOFFPROD			
b2	BOFFPROD			
b3	BOFFPROD			
b4	BOFFPROD			
b5	BOFFPROD			
b6	BOFFPROD			
b7	BOFFPRODEN	Backoff period auto random enable bit	0: Backoff period automatic random disabled 1: Backoff period automatic random enabled	R/W

BOFFPROD Bit (Backoff Period Bit)

The BOFFPROD bit can be used to set the random value of the backoff period when executing CSMA-CA.

BOFFPRODEN Bit (Backoff Period Auto Random Enable Bit)

By setting the BOFFPRODEN bit to 1, a random value is automatically generated with the value set in the BOFFPROD bit as the initial value, and the backoff period value in the CSMA-CA circuit is set. Make sure to set the BOFFPRODEN bit to 1 after the random value has been set with the BOFFPROD bit.
The BOFFPROD bit does not need to be set again while the BOFFPRODEN bit is set to 1.

25.2.29 PLL Division Registers 0 and 1 (BBPLLDIVL, BBPLLDIVH)

Address 2D3Bh to 2D3Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	0	1	1	0	0	1	0	1

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	0	0	0	0	1	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b11 to b0	PLLDIV	PLL divide ratio bit	Refer to **Table 25.3**.	R/W
b12	—	Reserved bit	Set to 0.	R/W
b15 to b13	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—

Table 25.3 Correspondence Between Register Setting Values and Channels

Channel (IEEE802.15.4)	Frequency (MHz)	PLLDIV Setting Value
0Bh (11)	2405	965h
0Ch (12)	2410	96Ah
0Dh (13)	2415	96Fh
0Eh (14)	2420	974h
0Fh (15)	2425	979h
10h (16)	2430	97Eh
11h (17)	2435	983h
12h (18)	2440	988h
13h (19)	2445	98Dh
14h (20)	2450	992h
15h (21)	2455	997h
16h (22)	2460	99Ch
17h (23)	2465	9A1h
18h (24)	2470	9A6h
19h (25)	2475	9ABh
1Ah (26)	2480	9B0h

25.2.30 Transmit Output Power Register (BBTXOUTPWR)

Address 2D3Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	TXOUTPWR	TXOUTPWR	TXOUTPWR	TXOUTPWR	TXOUTPWR
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TXOUTPWR	Transmit output power	Refer to **Table 25.4**.	R/W
b1	TXOUTPWR			
b2	TXOUTPWR			
b3	TXOUTPWR			
b4	TXOUTPWR			
b5	—	Reserved bit	Set to 0.	R/W
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

Table 25.4 Correspondence Between Register Setting Values and Output Power (Reference Data)

TXOUTPWR	Output Power (dBm)	TXOUTPWR	Output Power (dBm)
00h (Min)	–37.1	10h	–7.2
01h	–30.9	11h	–6.5
02h	–27.7	12h	–5.9
03h	–24.8	13h	–5.3
04h	–22.5	14h	–4.8
05h	–20.3	15h	–4.2
06h	–18.6	16h	–3.8
07h	–16.9	17h	–3.3
08h	–15.7	18h	–2.9
09h	–14.3	19h	–2.5
0Ah	–13.2	1Ah	–2.1
0Bh	–12.0	1Bh	–1.7
0Ch	–11.0	1Ch	–1.4
0Dh	–10.0	1Dh	–1.0
0Eh	–9.2	1Eh	–0.7
0Fh	–8.4	1Fh (Max)	–0.4

Note:
1. To set the output power further lower than the output power settings listed in Table 25.4, set registers TXOUTPWR and BBRFINI to values listed in Table 25.5. To change to another output power setting after the setting as listed in Table 25.5, write 3200h to the BBRFINI register and then set the TXOUTPWR register to a value listed in Table 25.4.

Table 25.5 Output Power Setting

Register Setting Value		Output Power (dBm)
TXOUTPWR	BBRFINI	
00h (Min)	3280h	–55.3 (1)

Note:
1. Reference value of output power.

25.2.31 RSSI Offset Register (BBRSSIOFS)

This register can be used to set an offset value as the RSSI value during CCA/ED or reception.
The value can be used to adjust the power value read from the RSSI/CCA result register to the power value applied to the antenna.
Set the value to two's complement in dBm units.
The value set in the receive level threshold set register or CCA level threshold set register is compared with the value to be stored in the RSSI/CCA result register (the value added with the offset value set in the RSSI offset register).

Example:
When the input power applied to the antenna is 0 dBm, if the value read from the RSSI/CCA result register is FDh (-3 dBm) while the value set in the RSSI offset register is F6h (initial value), the value read from the RSSI/CCA result register at the same input power level can be adjusted to 00h by setting F3h (F6h-3h) in the RSSI offset register in advance.

Address 2D3Dh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RSSIOFS	RSSIOFS	RSSIOFS	RSSIOFS	RSSIOFS	RSSIOFS	RSSIOFS	RSSIOFS
After Reset	1	1	1	1	0	1	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	RSSIOFS	RSSI offset bit	Sets the RSSI offset bit value.	R/W
b1	RSSIOFS			
b2	RSSIOFS			
b3	RSSIOFS			
b4	RSSIOFS			
b5	RSSIOFS			
b6	RSSIOFS			
b7	RSSIOFS			

25.2.32 Verification Mode Set Register (BBEVAREG)

This register can be used to set the verification mode necessary to obtain conformance certifications for technological standards.

Address 2D68h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	CONTRX	NOMOD	CONTTX
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	CONTTX	Continuous transmit mode bit (1)	0: Normal operation 1: Continuous transmit operation	R/W
b1	NOMOD	Non-modulation switch bit	0: Modulation signal 1: Non-modulation signal	R/W
b2	CONTRX	Continuous receive mode bit (1)	0: Normal operation 1: Continuous receive operation	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—			
b5	—			
b6	—			
b7	—			

Note:
1. Do not set theses bits to 1 simultaneously.

CONTTX Bit (Continuous Transmit Mode Bit)

By setting the CONTTX bit to 1 and then the TRNTRG bit in the BBTXRXCON register to 1 (transmission start), continuous transmit mode is selected. In this mode, frame transmission is repeated for the number of the (BBTXFLEN setting value − 2) bytes. The content of the frame to be transmitted is the value written to transmit RAM. Frame length value for transmission must be equal to or greater than 05h.

NOMOD Bit (Non-Modulation Switch Bit)

The NOMOD bit can be used to switch between a modulation signal and a non-modulation signal.

CONTRX Bit (Continuous Receive Mode Bit)

By setting the CONTRX bit to 1 and then the RCVTRG bit in the BBTXRXCON register to 1 (reception start), continuous receive mode is selected. In this mode, IDLE status is not selected even if frame reception is completed, and reception status remains the same. When using continuous receive mode, set 01h at address 2DA6h.

25.2.33 IDLE Wait Set Register (BBIDLEWAIT)

This register is used to set the wait time to transit to IDLE status after setting RFPWRON bit in the BBRFCON register to 1 (RF power ON) or the XINPWRON bit in the BBRFCON register to 1 (XIN power ON).
When the setting time has elapsed, an IDLE interrupt request or clock regulator interrupt is generated.
The initial value is 01h = 0.5 ms (the setting value is 1h = 0.5 ms).

Address 2D76h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	IDLEWAIT	IDLEWAIT	IDLEWAIT	IDLEWAIT	IDLEWAIT	IDLEWAIT
After Reset	0	0	0	0	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	IDLEWAIT	IDLE wait set	Sets the wait time to transit to IDLE status.	R/W
b1	IDLEWAIT			
b2	IDLEWAIT			
b3	IDLEWAIT			
b4	IDLEWAIT			
b5	IDLEWAIT			
b6	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b7	—			

25.2.34 ANTSW Output Timing Set Register (BBANTSWTIMG)

This register is used for setting the timing for the ASW pin output.
After setting the TRNTRG bit in the BBTXRXCON register to 1 (transmission start), the time to drive the ASW pin output to high can be set.
The setting value can be set in the range of 01h to 8Dh and the initial value is 72h (the setting value is 1h = about 1 μs).
Do not set values other than 01h (about 1 μs) to 8Dh (about 141 μs).

Address 2D7Ah

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ANTSWCONT	ANTSWCONT	ANTSWCONT	ANTSWCONT	ANTSWCONT	ANTSWCONT	ANTSWCONT	ANTSWCONT
After Reset	0	1	1	1	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	ANTSWCONT	ANTSW output timing set	Sets the timing for the ASW pin output. The setting value: 01h to 8Dh	R/W
b1	ANTSWCONT			
b2	ANTSWCONT			
b3	ANTSWCONT			
b4	ANTSWCONT			
b5	ANTSWCONT			
b6	ANTSWCONT			
b7	ANTSWCONT			

25.2.35 RF Initial Set Register (BBRFINI)

This is a 16-bit register used for the initial setting in the RF block.
The setting is performed at the RF power ON sequence.
To set this register, set the higher and lower bytes at the same time or set data in the lower byte first and then the higher byte.
To set this register again after having set data once, allow 40 cycles or more of f(BCLK). However, access to other registers is enabled.
If IDLE status is changed to RF OFF status, the RF initial setting is also cleared. Perform the RF initial setting again at the RF power ON sequence.

Address 2D7Dh to 2D7Ch

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	b15	b14	b13	b12	b11	b10	b9	b8
Symbol	—	—	—	—	—	—	—	—
After Reset	X	X	X	X	X	X	X	X

Bit	Symbol	Bit Name	Function	R/W
b15 to 0	RFINI	RF initial set	Sets data.	W

25.2.36 ANTSW Control Register (BBANTSWCON)

The ANTSW output enable bit can be used to output the ANTSW signal from P0_4.

Address 2D82h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	—	—	—	—	—	—	—	ANTSWEN
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ANTSWEN	ANTSW output enable bit	0: Normal port (P0_4) 1: ANTSW output (ASW)	R/W
b1	—	Reserved bits	Set to 0.	R/W
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			

ANTSWEN Bit (ANTSW Output Enable Bit)

The ANTSW signal can be output from P0_4.

25.2.37 Automatic ACK Response Timing Adjustment Register (BBACKRTNTIMG)

This register is used to adjust the ACK response timing when the automatic ACK response function is enabled.

Address 2D46h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	ACKRTN	ACKRTN	ACKRTN	ACKRTN	ACKRTN	ACKRTN	ACKRTN	ACKRTN
After Reset	0	0	1	0	0	0	1	0

Bit	Symbol	Bit Name	Function	R/W
b0	ACKRTN	Automatic ACK response timing set	Sets the ACK response timing when the automatic ACK response function is enabled.	R/W
b1	ACKRTN			
b2	ACKRTN			
b3	ACKRTN			
b4	ACKRTN			
b5	ACKRTN			
b6	ACKRTN			
b7	ACKRTN			

25.3 Control Sequence

25.3.1 RF and Baseband Block Startup Procedure Example

Use the following procedure to start up the RF and baseband blocks. (RF = OFF → RF = IDLE)

[1] Set 1 (baseband functions enabled) in the BBEN bit in the BBCON register.
[2] Set 05h at address 02D6Dh.
[3] Set 1 in bits BANK0INTSEL and ROR0INTSEL in the BBTXRXMODE4 register.
[4] Set 00h in the BBCALIC register.
[5] Set 00h in the BBIDLEIC register.
[6] Set 78h at address 2D92h.
[7] Set 87h at address 2D93h.
[8] Set 07h in the BBRFCON register.
[9] Wait until bit 7 at address 2D66h is set to 1.
[10] Set the **Register Setting Values for RF Initial Setting 1** in the BBRFINI register sequentially as listed in Table 25.6. However, wait until bit 6 at address 2D66h is set to 0 for each setting.
[11] Wait until the IR bit in the BBCALIC register is set to 1.
[12] Set the **Register Setting Values for RF Initial Setting 2** in the BBRFINI register sequentially as listed in Table 25.7. However, wait until bit 6 at address 2D66h is set to 0 for each setting.
[13] Set the **Register Setting Values** listed in Table 25.8. (1)
[14] Wait until the IR bit in the BBIDLEIC register is set to 1.
[15] Set 0 in bits BANK0INTSEL and ROR0INTSEL in the BBTXRXMODE4 register.

Notes:
1. For step [13], after reset is deasserted, the setting values are retained once they are set even if switching the RF to the OFF status. Thus, it is not necessary to perform the setting again when starting up the RF to the IDLE status for the second and subsequent times.
   However, when the RFRESET bit in the BBTXRXRST register is set to 1, the registers listed in Table 25.8 are initialized. Thus, it is necessary to perform the setting again.
2. During steps [10] to [12], calibration is performed in the RF block. This increases the current that flows into the VCCRF side for several hundreds μs, compared to the current during the IDLE status.

25.3.2 RF and Baseband Block Shutdown Procedure Example

[1] Set 00h in the BBRFCON register.
[2] Set 0 (baseband functions disabled) in the BBEN bit in the BBCON register.

25.3.3 Transmission Procedure Example

[1] Perform the procedure for starting up the RF and baseband blocks as shown in 25.3.1.
[2] Use registers BBPLLDIVL and BBPLLDIVH for channel setting.
[3] Use the BBTXOUTPWR register for output power setting.
([4] Set the AUTORCV0 bit in the BBTXRXMODE0 register.)
[5] Write to transmit RAM: addresses 2E00h to 2E7Eh
[6] Set the transmit frame length in the BBTXFLEN register.
[7] Set 1 (transmission start) in the TRNTRG bit in the BBTXRXCON register.

A transmission complete interrupt is generated when one of the following events occurs after transmission starts:
- Transmission is completed.
- ACK reception is completed after the ACK reception function is enabled and transmission with an ACK request is performed.
- The ACK is not received for a certain period after the ACK reception function is enabled and transmission with an ACK request is performed.
- The CCA result is that the channel is busy after transmission is performed with automatic CSMA-CA enabled.

25.3.4 Reception Procedure Example

[1] Perform the procedure for starting up the RF and baseband blocks as shown in 25.3.1.
[2] Use registers BBPLLDIVL and BBPLLDIVH for channel setting.
([3] Set bits BBTXRXMODE0, AUTOACKEN, AUTORCV0, and BEACONAUTORCV0 in the BBTXRXMODE0 register.)
[4] Set the PAN identifier in the BBPANID register.
[5] Set the BSHORTAD register or registers BBEXTENDAD0 to BBEXTENDAD3.
[6] Set 1 (reception start) in the RCVTRG bit in the BBTXRXCON register.
[7] Wait for the reception complete interrupt.
[8] Set the RCVBANKSEL bit in the BBTXRXMODE3 register for bank selection.
[9] Read the BBRXFLEN register.
[10] Confirm the CRC result by using the CRC bit in the BBTXRXST0 register.
[11] Read receive RAM data: addresses 2E80h to 2EFEh

Note:
1. When the automatic ACK response function is enabled, a transmission complete interrupt is generated when ACK response is completed. If no transmission complete interrupt is required, set the priority level of the transmission complete interrupt to 0 (disabled).

25.3.5 CCA Procedure Example

[1] Perform the procedure for starting up the RF and baseband blocks as shown in 25.3.1.
[2] Use registers BBPLLDIVL and BBPLLDIVH for channel setting.
[3] Set 1 (CCA start) in the CCATRG bit in the BBTXRXCON register.
[4] Wait for the CCA complete interrupt.
[5] Confirm the CCA result by using the CCA bit in the BBTXRXST0 register.

25.3.6 CSMA-CA Procedure Example

[1] Perform the procedure for starting up the RF and baseband blocks as shown in 25.3.1.
[2] Use registers BBPLLDIVL and BBPLLDIVH for channel setting.
([3] Set the BEACON bit in the BBTXRXMODE0 register.)
[4] Set the initial value in bits BOFFPROD0 to BOFFPROD6 in the BBBOFFPROD register.
Set 1 (backoff period automatic random enabled) in the BOFFPRODEN bit in the BBBOFFPROD register.
[5] Set 1 (automatic CSMA-CA start) in the CSMAST bit in the BBCSMACON0 register.
At the same time, if transmit processing is to be proceeded after CSMA-CA is completed, set 1 (transmit processing after CSMA-CA) in the CSMATRNST bit in the BBCSMACON0 register.
[6] Wait for the CSMA-CA complete interrupt.
[7] Confirm the CSMA-CA result by using the CSMACA bit in the BBTXRXST0 register.

Table 25.6 Register Setting Values for RF Initial Setting 1

No	Address 2D7Dh	Address 2D7Ch
1	00h	01h
2	02h	83h
3	4Eh	Value read from address 2D88h
4	3Eh	Value read from address 2D8Ah
5	34h	Value read from address 2D8Eh
6	04h	36h
7	22h	2Eh
8	24h	00h
9	06h	47h
10	16h	80h
11	50h	28h
12	52h	39h
13	0Ah	61h
14	5Eh	FCh
15	7Eh	00h

Table 25.7 Register Setting Values for RF Initial Setting 2

No	Address 2D7Dh	Address 2D7Ch
1	02h	00h
2	5Eh	F4h

Table 25.8 Register Setting Values

No.	Address	Setting Value	After Reset	Setting Yes/No	No.	Address	Setting Value	After Reset	Setting Yes/No	No.	Address	Setting Value	After Reset	Setting Yes/No
1	2D3Dh	F5h	F6h	Yes	69	2DDAh	5Fh	44h	Yes	137	2F3Eh	E5h	50h	Yes
2	2D46h	28h	22h	Yes	70	2DDBh	00h	00h		138	2F3Fh	0Fh	14h	Yes
3	2D4Ch	80h	00h	Yes	71	2DDCh	01h	01h		139	2F40h	E8h	E8h	
4	2D52h	FFh	42h	Yes	72	2DDDh	00h	00h		140	2F41h	03h	03h	
5	2D53h	72h	72h		73	2DDEh	05h	05h		141	2F42h	00h	E8h	Yes
6	2D54h	90h	8Dh	Yes	74	2DDFh	00h	00h		142	2F43h	04h	03h	Yes
7	2D58h	01h	48h	Yes	75	2DE0h	70h	B4h	Yes	143	2F44h	1Eh	E8h	Yes
8	2D5Ah	8Fh	00h	Yes	76	2DE1h	00h	00h		144	2F45h	02h	03h	Yes
9	2D5Bh	01h	7Ah	Yes	77	2DE2h	70h	B4h	Yes	145	2F46h	40h	58h	Yes
10	2D74h	03h	3Ch	Yes	78	2DE3h	00h	00h		146	2F47h	01h	02h	Yes
11	2DA0h	07h	07h		79	2DE4h	70h	B4h	Yes	147	2F48h	3Fh	2Ch	Yes
12	2DA1h	01h	01h		80	2DE5h	00h	00h		148	2F49h	00h	01h	Yes
13	2DA2h	0Ch	07h	Yes	81	2DE6h	88h	50h	Yes	149	2F4Ah	E1h	EAh	Yes
14	2DA3h	00h	00h		82	2DE7h	7Fh	14h	Yes	150	2F4Bh	F6h	01h	Yes
15	2DA4h	20h	E8h	Yes	83	2DE8h	70h	C8h	Yes	151	2F4Ch	0Ch	18h	Yes
16	2DA5h	01h	03h	Yes	84	2DE9h	00h	00h		152	2F4Dh	4Fh	48h	Yes
17	2DA6h	03h	03h		85	2DEAh	70h	FAh	Yes	153	2F4Eh	08h	00h	Yes
18	2DA7h	DDh	DDh		86	2DEBh	00h	00h		154	2F4Fh	00h	40h	Yes
19	2DA8h	20h	E8h	Yes	87	2DECh	70h	FAh	Yes	155	2F50h	6Ah	10h	Yes
20	2DA9h	01h	03h	Yes	88	2DEDh	00h	00h		156	2F51h	0Eh	0Eh	
21	2DAAh	20h	E8h	Yes	89	2DEEh	88h	50h	Yes	157	2F52h	08h	14h	Yes
22	2DABh	01h	03h	Yes	90	2DEFh	7Fh	14h	Yes	158	2F53h	00h	00h	
23	2DACh	14h	32h	Yes	91	2DF0h	0Eh	17h	Yes	159	2F54h	00h	00h	
24	2DADh	00h	00h		92	2DF1h	34h	67h	Yes	160	2F55h	40h	00h	Yes
25	2DAEh	05h	08h	Yes	93	2DF2h	4Ah	7Dh	Yes	161	2F56h	C8h	C8h	
26	2DAFh	09h	0Dh	Yes	94	2DF3h	6Ah	7Fh	Yes	162	2F57h	00h	00h	
27	2DB0h	58h	58h		95	2DF4h	35h	35h		163	2F58h	C8h	C8h	
28	2DB1h	02h	02h		96	2DF5h	05h	04h	Yes	164	2F59h	00h	00h	
29	2DB2h	1Eh	00h	Yes	97	2DF6h	28h	50h	Yes	165	2F5Ah	93h	93h	
30	2DB3h	02h	00h	Yes	98	2DF7h	00h	00h		166	2F5Bh	34h	34h	
31	2DB4h	32h	32h		99	2DF8h	EEh	EEh		167	2F5Ch	69h	69h	
32	2DB5h	00h	00h		100	2DF9h	01h	01h		168	2F5Dh	93h	93h	
33	2DB6h	60h	B4h	Yes	101	2DFAh	12h	12h		169	2F5Eh	34h	34h	
34	2DB7h	00h	00h		102	2DFBh	7Fh	7Eh	Yes	170	2F5Fh	69h	69h	
35	2DB8h	60h	C8h	Yes	103	2DFCh	45h	78h	Yes	171	2F60h	92h	92h	
36	2DB9h	00h	00h		104	2DFDh	A3h	D6h	Yes	172	2F61h	34h	34h	
37	2DBAh	55h	55h		105	2DFEh	34h	37h	Yes	173	2F62h	69h	69h	
38	2DBBh	00h	01h	Yes	106	2DFFh	40h	00h	Yes	174	2F63h	92h	92h	
39	2DBCh	22h	28h	Yes	107	2F20h	2Fh	3Fh	Yes	175	2F64h	34h	34h	
40	2DBDh	00h	00h		108	2F21h	00h	00h		176	2F65h	69h	69h	
41	2DBEh	00h	00h		109	2F22h	5Fh	64h	Yes	177	2F66h	D3h	93h	Yes
42	2DBFh	03h	03h		110	2F23h	00h	00h		178	2F67h	B6h	34h	Yes
43	2DC0h	00h	00h		111	2F24h	5Fh	64h	Yes	179	2F68h	6Dh	69h	Yes
44	2DC1h	00h	00h		112	2F25h	00h	00h		180	2F69h	D3h	93h	Yes
45	2DC2h	20h	20h		113	2F26h	3Fh	05h	Yes	181	2F6Ah	B6h	34h	Yes
46	2DC3h	08h	08h		114	2F27h	00h	00h		182	2F6Bh	6Dh	69h	Yes
47	2DC4h	11h	11h		115	2F28h	01h	11h	Yes	183	2F6Ch	8Ah	4Ah	Yes
48	2DC5h	34h	14h	Yes	116	2F29h	01h	01h		184	2F6Dh	A4h	B2h	Yes
49	2DC6h	2Ch	2Ch		117	2F2Ah	2Ah	28h	Yes	185	2F6Eh	44h	64h	Yes
50	2DC7h	01h	01h		118	2F2Bh	17h	0Fh	Yes	186	2F6Fh	41h	4Ah	Yes
51	2DC8h	01h	01h		119	2F2Ch	1Eh	10h	Yes	187	2F70h	A2h	B2h	Yes
52	2DC9h	00h	00h		120	2F2Dh	19h	19h		188	2F71h	44h	64h	Yes
53	2DCAh	76h	EDh	Yes	121	2F2Eh	26h	25h	Yes	189	2F72h	6Bh	6Bh	
54	2DCBh	6Bh	BAh	Yes	122	2F2Fh	15h	05h	Yes	190	2F73h	B7h	B7h	
55	2DCCh	B7h	76h	Yes	123	2F30h	C8h	C8h		191	2F74h	76h	76h	
56	2DCDh	76h	2Dh	Yes	124	2F31h	00h	00h		192	2F75h	6Bh	6Dh	Yes
57	2DCEh	0Fh	34h	Yes	125	2F32h	FAh	FAh		193	2F76h	B7h	BBh	Yes
58	2DCFh	00h	00h		126	2F33h	00h	00h		194	2F77h	76h	76h	
59	2DD0h	7Fh	7Fh		127	2F34h	C8h	FAh	Yes	195	2F78h	8Ah	8Ah	
60	2DD1h	00h	00h		128	2F35h	00h	00h		196	2F79h	A4h	A4h	
61	2DD2h	4Ch	48h	Yes	129	2F36h	C8h	50h	Yes	197	2F7Ah	44h	44h	
62	2DD3h	14h	0Dh	Yes	130	2F37h	00h	14h	Yes	198	2F7Bh	41h	41h	
63	2DD4h	3Fh	05h	Yes	131	2F38h	C8h	C8h		199	2F7Ch	A2h	A2h	
64	2DD5h	00h	00h		132	2F39h	00h	00h		200	2F7Dh	44h	44h	
65	2DD6h	00h	00h		133	2F3Ah	C8h	FAh	Yes	201	2F7Eh	6Bh	6Bh	
66	2DD7h	00h	00h		134	2F3Bh	00h	00h		202	2F7Fh	B7h	37h	Yes
67	2DD8h	C4h	48h	Yes	135	2F3Ch	C8h	FAh	Yes					
68	2DD9h	19h	0Dh	Yes	136	2F3Dh	10h	00h	Yes					

Note:

1. The setting values must be always set in the registers indicated by "Yes" in the Setting Yes/No column.

25.4 Notes on Baseband Functions

25.4.1 Processing for Specified Receive Frames

In addition to the address filtering function of the R8C/3MQ baseband functions, use software to discard the frames listed in Table 25.9 to comply with the IEEE802.15.4 standard.

Table 25.9 Frames to be Discarded

Frame Type (Frame Control Field Bits 2-0)	Transmit Destination Address Mode (Frame Control Field Bits 11-10)	Transmit Source Address Mode (Frame Control Field Bits 15-14)
000b	00b	00b
000b	01b	-
000b	-	01b
000b	10b	-
000b	11b	-

Note:
1. The frames indicated by a dash (-) in the table must be discarded regardless of their values.

25.4.2 How to Perform Transmission with Timer Trigger CSMA-CA

The following settings allow the timer compare 0 transmit trigger function to be used as a trigger for the CSMA-CA function.
- Set the time to start transmission with CSMA-CA in the BBTCOMP0REG0 register.
- Set 1 in bit 3 in the BBTIMECON register.
- Set 1 in the COMP0TRG bit in the BBTIMECON register.

25.4.3 Settings When Using Automatic CSMA-CA Function

When using the automatic CSMA-CA function, set the following values at addresses 2D4Eh and 2D4Fh.
- When the BEMIN bit in the BBCSMACON1 register = 000b:
  Set F9h at address 2D4Eh and 13h at address 2D4Fh.
- When the BEMIN bit in the BBCSMACON1 register = other than 000b:
  Set 01h at address 2D4Eh and 09h at address 2D4Fh.

After reset is deasserted, the initial values of addresses 2D4Eh and 2D4Fh are 01h and 09h, respectively. If this function is not used with the BEMIN bit = 000b, it is not necessary to set any values at addresses 2D4Eh and 2D4Fh.

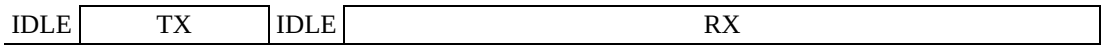
25.4.4 Notes on Stopping RF Communication Using RF Communication Stop Bit

When the RFSTOP bit in the BBTXRXRST register is set to 1 (RF communication stopped) while a radio frame is transmitted/received or during CCA operation, an interrupt related to transmission, reception, or CCA may be generated after that setting. As a countermeasure, disable related interrupts before setting the RFSTOP bit to 1. Applicable interrupts are transmission complete, bank 0 reception complete, bank 1 reception complete, address filter, CCA complete, transmit overrun, receive overrun 0, and receive overrun 1.

25.4.5 Automatic Transmit and Receive Operation Examples

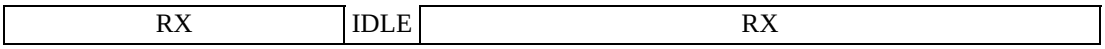
25.4.5.1 Transmission

- Set the AUTORCV0 bit in the BBTXRXMODE0 register = 1 (automatic reception switching enabled)



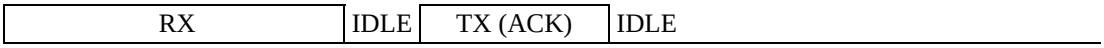
25.4.5.2 Reception

- Set the AUTORCV1 bit in the BBTXRXMODE0 register = 1 (automatic reception switching enabled)



25.4.5.3 ACK

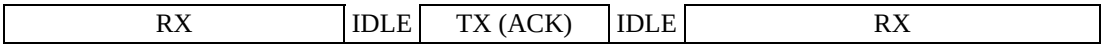
- Set the AUTOACK bit in the BBTXRXMODE0 register = 1 (automatic ACK enabled)



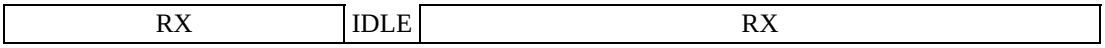
ACK requested

No ACK request

- Set the AUTOACK bit in the BBTXRXMODE0 register = 1 (automatic ACK enabled)
- Set the AUTORCV1 bit in the BBTXRXMODE0 register = 1 (automatic reception switching enabled)

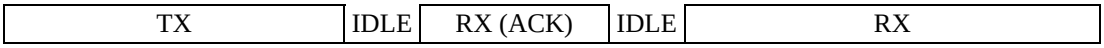


ACK requested



No ACK request

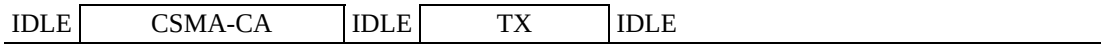
- Set the ACKRCVEN bit in the BBTXRXMODE1 register = 1 (automatic ACK reception enabled)
- Set the AUTORCV0 bit in the BBTXRXMODE0 register = 1 (automatic reception switching enabled)



ACK requested

25.4.5.4 CSMA-CA

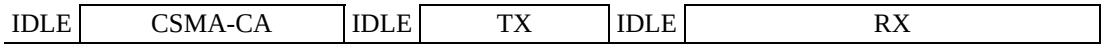
- Set the CSMATRNST bit in the BBCSMACON0 register = 1 (transmit processing after CSMA-CA)



Result TRUE

Result FALSE

- Set the CSMATRNST bit in the BBCSMACON0 register = 1 (transmit processing after CSMA-CA)
- Set the AUTORCV0 bit in the BBTXRXMODE0 register = 1 (automatic reception switching enabled)



Result TRUE

Result FALSE

26. Flash Memory

The flash memory can perform in the following three rewrite modes: CPU rewrite mode, standard serial I/O mode, and parallel I/O mode.

26.1 Overview

Table 26.1 lists the Flash Memory Version Performance (refer to **Tables 1.1 and 1.2 R8C/3MQ Group Specifications** for items not listed in Table 26.1).

Table 26.1 Flash Memory Version Performance

Item		Specification
Flash memory operating mode		3 modes (CPU rewrite, standard serial I/O, and parallel I/O)
Division of erase blocks		Refer to **Figure 26.1**.
Programming method		Byte units
Erasure method		Block erase
Programming and erasure control method (1)		Program and erase control by software commands
Rewrite control method	Blocks 0 to 7 (Program ROM) (3)	Rewrite protect control in block units by the lock bit
	Blocks A, B, C, and D (Data flash)	Individual rewrite protect control on blocks A, B, C, and D by bits FMR14, FMR15, FMR16, and FMR17 in the FMR1 register
Number of commands		7 commands
Programming and erasure endurance (2)	Blocks 0 to 7 (Program ROM) (3)	1,000 times
	Blocks A, B, C, and D (Data flash)	10,000 times
ID code check function		Standard serial I/O mode supported
ROM code protection		Parallel I/O mode supported

Notes:
1. The supply voltage when performing a programming or erase operation differs depending on the flash memory operating mode.
   Refer to **Table 26.2 Flash Memory Rewrite Mode**.
2. Definition of programming and erasure endurance
   The programming and erasure endurance is defined on a per-block basis. If the programming and erasure endurance is n (n = 1,000 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1-Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. When performing 100 or more rewrites, the actual erase count can be reduced by executing program operations in such a way that all blank areas are used before performing an erase operation. Avoid rewriting only particular blocks and try to average out the programming and erasure endurance of the blocks. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
3. The number of blocks and block division vary with the MCU. Refer to **Figure 26.1 R8C/3MQ Group Flash Memory Block Diagram** for details.

Table 26.2 Flash Memory Rewrite Mode

Flash Memory Rewrite Mode	CPU Rewrite Mode	Standard Serial I/O Mode	Parallel I/O Mode
Function	User ROM area is rewritten by executing software commands from the CPU.	User ROM area is rewritten using a dedicated serial programmer.	User ROM area is rewritten using a dedicated parallel programmer.
Rewritable area	User ROM	User ROM	User ROM
Rewrite programs	User program	Standard boot program	—
Supply voltage when programming and erasing	VCC = 1.8 V to 3.6 V	VCC = 2.7 V to 3.6 V	VCC = 2.7 V to 3.6 V

26.2 Memory Map

The flash memory contains a user ROM area and a boot ROM area (reserved area).
Figure 26.1 shows the R8C/3MQ Group Flash Memory Block Diagram.
The user ROM area contains program ROM and data flash.
Program ROM: Flash memory mainly used for storing programs
Data flash: Flash memory mainly used for storing data to be rewritten
Programs cannot be executed in the data flash.
Do not use the data flash as a program area.
The user ROM area is divided into several blocks. The user ROM area can be rewritten in CPU rewrite mode, standard serial I/O mode, or parallel I/O mode.
The rewrite control program (standard boot program) for standard serial I/O mode is stored in the boot ROM area before shipment. The boot ROM area is allocated separately from the user ROM area.

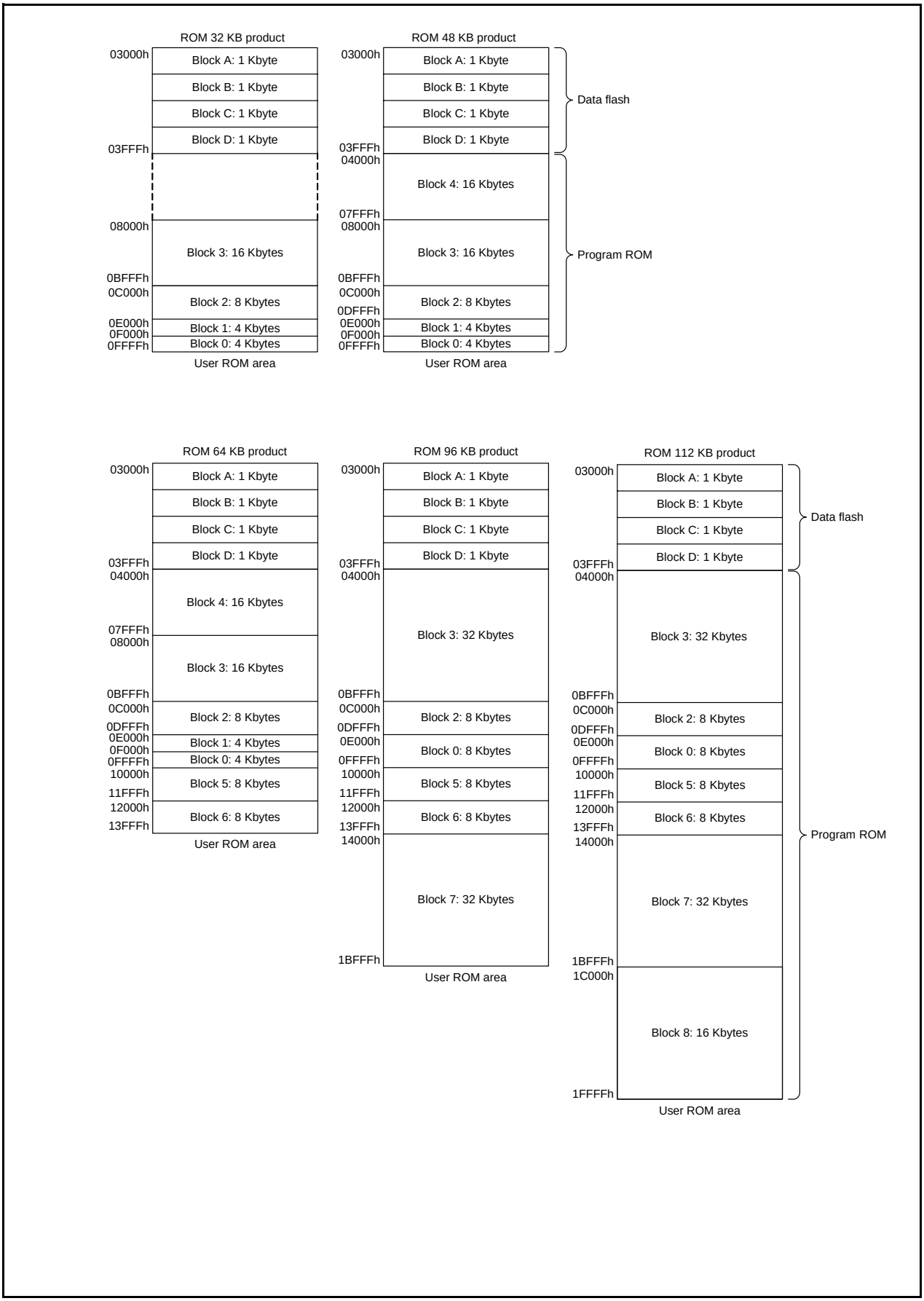


Figure 26.1 R8C/3MQ Group Flash Memory Block Diagram

26.3 Functions to Prevent Flash Memory from being Rewritten

Standard serial I/O mode has an ID code check function, and parallel I/O mode has a ROM code protect function to prevent the flash memory from being read or rewritten easily.

26.3.1 ID Code Check Function

The ID code check function is used in standard serial I/O mode. Unless 3 bytes (addresses 0FFFCh to 0FFFEh) of the reset vector are set to FFFFFFh, the ID codes sent from the serial programmer or the on-chip debugging emulator and the 7-byte ID codes written in the flash memory are checked to see if they match. If the ID codes do not match, the commands sent from the serial programmer or the on-chip debugging emulator are not accepted. For details of the ID code check function, refer to **12. ID Code Areas**.

26.3.2 ROM Code Protect Function

The ROM protect function prevents the contents of the flash memory from being read, rewritten, or erased using the OFS register in parallel I/O mode.
Refer to **13. Option Function Select Area** for details of the option function select area.

The ROM code protect function is enabled by writing 1 to the ROMCR bit and writing 0 to the ROMCP1 bit. This prevents the contents of the on-chip flash memory from being read or rewritten.
Once ROM code protection is enabled, the content of the internal flash memory cannot be rewritten in parallel I/O mode. To disable ROM code protection, erase the block including the OFS register using CPU rewrite mode or standard serial I/O mode.

26.3.3 Option Function Select Register (OFS)

Address 0FFFFh

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	CSPROINI	LVDAS	VDSEL1	VDSEL0	ROMCP1	ROMCR	—	WDTON
After Reset	User Setting Value (1)							

Bit	Symbol	Bit Name	Function	R/W
b0	WDTON	Watchdog timer start select bit	0: Watchdog timer automatically starts after reset 1: Watchdog timer is stopped after reset	R/W
b1	—	Reserved bit	Set to 1.	R/W
b2	ROMCR	ROM code protect disable bit	0: ROM code protect disabled 1: ROMCP1 bit enabled	R/W
b3	ROMCP1	ROM code protect bit	0: ROM code protect enabled 1: ROM code protect disabled	R/W
b4	VDSEL0	Voltage detection 0 level select bit (2)	b5 b4 0 0: Do not set. 0 1: 2.85 V selected (Vdet0_2) 1 0: 2.35 V selected (Vdet0_1) 1 1: 1.90 V selected (Vdet0_0)	R/W
b5	VDSEL1			R/W
b6	LVDAS	Voltage detection 0 circuit start bit (3)	0: Voltage monitor 0 reset enabled after reset 1: Voltage monitor 0 reset disabled after reset	R/W
b7	CSPROINI	Count source protection mode after reset select bit	0: Count source protect mode enabled after reset 1: Count source protect mode disabled after reset	R/W

Notes:
1. The OFS register is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
   Do not write additions to the OFS register. If the block including the OFS register is erased, the OFS register is set to FFh.
   Initial value of OFS register is FFh. The value of OFS register changes as programmed by user.
2. The same level of the voltage detection 0 level selected by bits VDSEL0 and VDESL1 is set in both functions of voltage monitor 0 reset and power-on reset.
3. To use power-on reset and voltage monitor 0 reset, set the LVDAS bit to 0 (voltage monitor 0 reset enabled after reset).

For a setting example of the OFS register, refer to **13.3.1 Setting Example of Option Function Select Area**.

LVDAS Bit (Voltage Detection 0 Circuit Start Bit)

The Vdet0 voltage to be monitored by the voltage detection 0 circuit is selected by bits VDSEL0 and VDSEL1.

26.4 CPU Rewrite Mode

In CPU rewrite mode, the user ROM area can be rewritten by executing software commands from the CPU. Therefore, the user ROM area can be rewritten directly while the MCU is mounted on a board without using a ROM programmer. Execute the software command only to blocks in the user ROM area.
The flash module has an erase-suspend function which halts the erase operation temporarily during an erase operation in CPU rewrite mode. During erase-suspend, the flash memory can be read or programmed.
Erase-write 0 mode (EW0 mode) and erase-write 1 mode (EW1 mode) are available in CPU rewrite mode.
Table 26.3 lists the Differences between EW0 Mode and EW1 Mode.

Table 26.3 Differences between EW0 Mode and EW1 Mode

Item	EW0 Mode	EW1 Mode
Operating mode	Single-chip mode	Single-chip mode
Rewrite control program allocatable area	User ROM	User ROM
Rewrite control program executable areas	RAM (The rewrite control program must be transferred before being executed.) However, the program can be executed in the program ROM area when rewriting the data flash area.	User ROM or RAM
Rewritable area	User ROM	User ROM However, blocks which contain the rewrite control program are excluded.
Software command restrictions	—	Program and block erase commands Cannot be executed to any block which contains the rewrite control program.
Mode after programming or block erasure or after entering erase-suspend	Read array mode	Read array mode
CPU and DTC state during programming and block erasure	The CPU operates.	• The CPU or DTC operates while the data flash area is being programmed or block erased. • The CPU or DTC is put in a hold state while the program ROM area is being programmed or block erased (I/O ports retain the state before the command execution).
Flash memory status detection	Read bits FST7, FST5, and FST4 in the FST register by a program.	Read bits FST7, FST5, and FST4 in the FST register by a program.
Conditions for entering erase-suspend	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program. • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.	• Set bits FMR20 and FMR21 in the FMR2 register to 1 by a program (while rewriting the data flash area). • Set bits FMR20 and FMR22 in the FMR2 register to 1 and the enabled maskable interrupt is generated.
CPU clock	1.8 V ≤ VCC < 2.15 V: Max. 4 MHz 2.15 V ≤ VCC < 2.7 V: Max. 8 MHz 2.7 V ≤ VCC ≤ 3.6 V: Max. 16 MHz	

26.4.1 Flash Memory Status Register (FST)

Address 01B2h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FST7	FST6	FST5	FST4	—	LBDATA	BSYAEI	RDYSTI
After Reset	1	0	0	0	0	X	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	RDYSTI	Flash ready status interrupt request flag (1, 4)	0: No flash ready status interrupt request 1: Flash ready status interrupt request	R/W
b1	BSYAEI	Flash access error interrupt request flag (2, 4)	0: No flash access error interrupt request 1: Flash access error interrupt request	R/W
b2	LBDATA	LBDATA monitor flag	0: Locked 1: Not locked	R
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	FST4	Program error flag (3)	0: No program error 1: Program error	R
b5	FST5	Erase error/blank check error flag (3)	0: No erase error/blank check error 1: Erase error/blank check error	R
b6	FST6	Erase-suspend status flag	0: Other than erase-suspend 1: During erase-suspend	R
b7	FST7	Ready/busy status flag	0: Busy 1: Ready	R

Notes:
1. The RDYSTI bit cannot be set to 1 (flash ready status interrupt request) by a program.
   When writing 0 (no flash ready status interrupt request) to the RDYSTI bit, read this bit (dummy read) before writing to it.
   Make sure the DTC is not activated by the flash ready status source between reading and writing.
   To confirm this bit, set the RDYSTIE bit in the FMR0 register to 1 (flash ready status interrupt enabled).
2. The BSYAEI bit cannot be set to 1 (flash access error interrupt request) by a program.
   When writing 0 (no flash access error interrupt request) to the BSYAEI bit, read this bit (dummy read) before writing to it.
   To confirm this bit, set the BSYAEIE bit in the FMR0 register to 1 (flash access error interrupt enabled) or set the CMDERIE bit in the FMR0 register to 1 (erase/write error interrupt enabled).
3. This bit is also set to 1 (error) when a command error occurs.
4. When this bit is set to 1, do not set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).

RDYSTI Bit (Flash Ready Status Interrupt Request Flag)

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled) and auto-programming or auto-erasure completes, or erase-suspend mode is entered, the RDYSTI bit is set to 1 (flash ready status interrupt request).
During interrupt handling, set the RDYSTI bit to 0 (no flash ready status interrupt request).

[Condition for setting to 0]
Set to 0 by an interrupt handling program.
[Condition for setting to 1]
When the flash memory status changes from busy to ready while the RDYSTIE bit in the FRMR0 register is set to 1, the RDYSTI bit is set to 1.
The status is changed from busy to ready in the following states:
- Completion of erasing/programming the flash memory
- Suspend acknowledgement
- Completion of forcible termination
- Completion of the lock bit program
- Completion of the read lock bit status
- Completion of the block blank check
- When the flash memory can be read after it is released from stop state.

BSYAEI Bit (Flash Access Error Interrupt Request Flag)

The BSYAEI bit is set to 1 (flash access error interrupt request) when the BSYAEIE bit in the FMR0 register is set to 1 (flash access error interrupt enabled) and the block during auto-programming/auto-erasure is accessed. This bit is also set to 1 if an erase or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).
During interrupt handling, set the BSYAEI bit to 0 (no flash access error interrupt request).

[Conditions for setting to 0]
(1) Set to 0 by an interrupt handling program.
(2) Execute the clear status register command.
[Conditions for setting to 1]
(1) Read or write the area that is being erased/written when the BSYAEIE bit in the FMR0 register is set to 1 and while the flash memory is busy.
Or, read the data flash area while erasing/writing to the program ROM area. (Note that the read value is undefined in both cases. Writing has no effect.)
(2) If a command sequence error, erase error, blank check error, or program error occurs when the CMDERIE bit in the FMR0 register is set to 1 (erase/write error interrupt enabled).

LBDATA Bit (LBDATA Monitor Flag)

This is a read-only bit indicating the lock bit status. To confirm the lock bit status, execute the read lock bit status command and read the LBDATA bit after the FST7 bit is set to 1 (ready).
The condition for updating this bit is when the program, erase, read lock bit status commands are generated.
When the read lock bit status command is input, the FST7 bit is set to 0 (busy). At the time when the FST7 bit is set to 1 (ready), the lock bit status is stored in the LBDATA bit. The data in the LBDATA bit is retained until the next command is input.

FST4 Bit (Program Error Flag)

This is a read-only bit indicating the auto-programming status. The bit is set to 1 if a program error occurs; otherwise, it is set to 0. For details, refer to the description in **26.4.12 Full Status Check**.

FST5 Bit (Erase Error/Blank Check Error Flag)

This is a read-only bit indicating the status of auto-erasure or the block blank check command. The bit is set to 1 if an erase error or blank check error occurs; otherwise, it is set to 0. Refer to **26.4.12 Full Status Check** for details.

FST6 Bit (Erase Suspend Status Flag)

This is a read-only bit indicating the suspend status. The bit is set to 1 when an erase-suspend request is acknowledged and a suspend status is entered; otherwise, it is set to 0.

FST7 Bit (Ready/Busy Status Flag)

When the FST7 bit is set to 0 (busy), the flash memory is in one of the following states:
- During programming
- During erasure
- During the lock bit program
- During the read lock bit status
- During the block blank check
- During forced stop operation
- The flash memory is being stopped
- The flash memory is being activated

Otherwise, the FST7 bit is set to 1 (ready).

26.4.2 Flash Memory Control Register 0 (FMR0)

Address 01B4h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	RDYSTIE	BSYAEIE	CMDERIE	CMDRST	FMSTP	FMR02	FMR01	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Reserved bit	Set to 0.	R/W
b1	FMR01	CPU rewrite mode select bit (1, 4)	0: CPU rewrite mode disabled 1: CPU rewrite mode enabled	R/W
b2	FMR02	EW1 mode select bit (1)	0: EW0 mode 1: EW1 mode	R/W
b3	FMSTP	Flash memory stop bit (2)	0: Flash memory operates 1: Flash memory stops (Low-power consumption state, flash memory initialization)	R/W
b4	CMDRST	Erase/write sequence reset bit (3)	When the CMDRST bit is set to 1, the erase/write sequence is reset and erasure/writing can be forcibly stopped. When read, the content is 0.	R/W
b5	CMDERIE	Erase/write error interrupt enable bit	0: Erase/write error interrupt disabled 1: Erase/write error interrupt enabled	R/W
b6	BSYAEIE	Flash access error interrupt enable bit	0: Flash access error interrupt disabled 1: Flash access error interrupt enabled	R/W
b7	RDYSTIE	Flash ready status interrupt enable bit	0: Flash ready status interrupt disabled 1: Flash ready status interrupt enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. Write to the FMSTP bit by a program transferred to the RAM. The FMSTP bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled). To set the FMSTP bit to 1 (flash memory stops), set it when the FST7 bit in the FST register is set to 1 (ready).
3. The CMDRST bit is enabled when the FMR01 bit is set to 1 (CPU rewrite mode enabled) and the FST7 bit in the FST register is set to 0 (busy).
4. To set the FMR01 bit to 0 (CPU rewrite mode disabled), set it when the RDYSTI bit in the FST register is set to 0 (no flash ready status interrupt request) and the BSYAEI bit is set to 0 (no flash access error interrupt request).

FMR01 Bit (CPU Rewrite Mode Select Bit)

When the FMR01 bit is set to 1 (CPU rewrite mode enabled), the MCU is made ready to accept software commands.

FMR02 Bit (EW1 Mode Select Bit)

When the FMR02 bit is set to 1 (EW1 mode), EW1 mode is selected.

FMSTP Bit (Flash Memory Stop Bit)

This bit is used to initialize the flash memory control circuits, and also to reduce the amount of current consumed by the flash memory. Access to the flash memory is disabled by setting the FMSTP bit to 1.
Write to the FMSTP bit by a program transferred to the RAM.
To reduce the power consumption further in low-speed on-chip oscillator mode (XIN clock stopped), and low-speed clock mode (XIN clock stopped), set the FMSTP bit to 1. Refer to **27.2.9 Stopping Flash Memory** for details.
When entering stop mode or wait mode while CPU rewrite mode is disabled, the FMR0 register does not need to be set because the power for the flash memory is automatically turned off and is turned back on when exiting stop or wait mode.
When the FMSTP bit is set to 1 (including during the busy status (the period while the FST7 bit is 0) immediately after the FMSTP bit is changed from 1 to 0), do not set to low-current-consumption read mode at the same time.

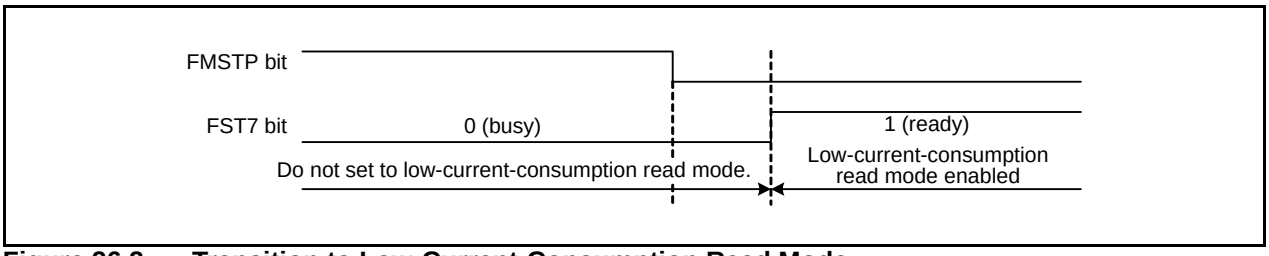


Figure 26.2 Transition to Low-Current-Consumption Read Mode

CMDRST Bit (Erase/Write Sequence Reset Bit)

This bit is used to initialize the flash memory sequence and forcibly stop a program or erase command. The program ROM area can be read when resetting the sequence of programming/erasing the data flash area.
If the program or erase command is forcibly stopped using the CMDRST bit in the FMR0 register, execute the clear status register command after the FST7 bit in the FST register is changed to 1 (ready). To program the same address again, execute the block erase command again and ensure it has been completed normally before programming. If the addresses and blocks which the program or block erase command is forcibly stopped are allocated in the program area, set the FMR13 bit in the FMR1 register to 1 (lock bit disabled) before executing the block erasure command again.
When the CMDRST bit is set to 1 (erasure/writing stopped) during erase-suspend, the suspend status is also initialized. Thus execute block erasure again to the block which the block erasure is being suspended.
When td(CMDRST-READY) has elapsed after the CMDRST bit is set to 1 (erasure/writing stopped), the executing command is forcibly stopped and reading from the flash memory is enabled.

CMDERIE Bit (Erase/Write Error Interrupt Enable Bit)

This bit enables a flash command error interrupt to be generated if the following errors occur:
- Program error
- Block erase error
- Command sequence error
- Block blank check error

If the CMDERIE bit is set to 1 (erase/write error interrupt enabled), an interrupt is generated if the above errors occur.
If a flash command error interrupt is generated, execute the clear status register command during interrupt handling.

To change the CMDERIE bit from 0 (erase/write error interrupt disabled) to 1 (erase/write error interrupt enabled), make the setting as follows:
(1) Execute the clear status register command.
(2) Set the CMDERIE bit to 1.

BSYAEIE Bit (Flash Access Error Interrupt Enable Bit)

This bit enables a flash access error interrupt to be generated if the flash memory during rewriting is accessed.

To change the BSYAEIE bit from 0 (flash access error interrupt disabled) to 1 (flash access error interrupt enabled), make the setting as follows:
(1) Read the BSYAEI bit in the FST register (dummy read).
(2) Write 0 (no flash access error interrupt request) to the BSYAEI bit.
(3) Set the BSYAEIE bit to 1 (flash access error interrupt enabled).

RDYSTIE Bit (Flash Ready Status Interrupt Enable Bit)

This bit enables a flash ready status error interrupt to be generated when the status of the flash memory sequence changes from the busy to ready status.

To change the RDYSTIE bit from 0 (flash ready status interrupt disabled) to 1 (flash ready status interrupt enabled), make the setting as follows:
(1) Read the RDYSTI bit in the FST register (dummy read).
(2) Write 0 (no flash ready status interrupt request) to the RDYSTI bit.
(3) Set the RDYSTIE bit to 1 (flash ready status interrupt enabled).

26.4.3 Flash Memory Control Register 1 (FMR1)

Address 01B5h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR17	FMR16	FMR15	FMR14	FMR13	—	—	—
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b1	—			
b2	—			
b3	FMR13	Lock bit disable select bit (1)	0: Lock bit enabled 1: Lock bit disabled	R/W
b4	FMR14	Data flash block A rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b5	FMR15	Data flash block B rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b6	FMR16	Data flash block C rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W
b7	FMR17	Data flash block D rewrite disable bit (2, 3)	0: Rewrite enabled (software command acceptable) 1: Rewrite disabled (software command not acceptable, no error occurred)	R/W

Notes:
1. To set the FMR13 bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. To set this bit to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 1 and writing 0.
3. This bit is set to 0 when the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).

FMR13 Bit (Lock Bit Disable Select Bit)

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit is disabled. When the FMR13 bit is set to 0, the lock bit is enabled. Refer to **26.4.10 Data Protect Function** for the details of the lock bit.
The FMR13 bit enables the lock bit function only and the lock bit data does not change. However, when a block erase command is executed while the FMR13 bit is set to 1, the lock bit data set to 0 (locked) changes to 1 (not locked) after erasure completes.

[Conditions for setting to 0]
The FMR13 bit is set to 0 when one of the following conditions is met.
- Completion of the program command
- Completion of the erase command
- Generation of a command sequence error
- Transition to erase-suspend
- If the FMR01 bit in the FMR0 register is set to 0 (CPU rewrite mode disabled).
- If the FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

[Condition for setting to 1]
Set to 1 by a program.

FMR14 Bit (Data Flash Block A Rewrite Disable Bit)

When the FMR 14 bit is set to 0, data flash block A accepts program and block erase commands.

FMR15 Bit (Data Flash Block B Rewrite Disable Bit)

When the FMR 15 bit is set to 0, data flash block B accepts program and block erase commands.

FMR16 Bit (Data Flash Block C Rewrite Disable Bit)

When the FMR 16 bit is set to 0, data flash block C accepts program and block erase commands.

FMR17 Bit (Data Flash Block D Rewrite Disable Bit)

When the FMR 17 bit is set to 0, data flash block D accepts program and block erase commands.

26.4.4 Flash Memory Control Register 2 (FMR2)

Address 01B6h

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Symbol	FMR27	—	—	—	—	FMR22	FMR21	FMR20
After Reset	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FMR20	Erase-suspend enable bit (1)	0: Erase-suspend disabled 1: Erase-suspend enabled	R/W
b1	FMR21	Erase-suspend request bit (2)	0: Erase restart 1: Erase-suspend request	R/W
b2	FMR22	Interrupt request suspend request enable bit (1)	0: Erase-suspend request disabled by interrupt request 1: Erase-suspend request enabled by interrupt request	R/W
b3	—	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
b4	—	Reserved bits	Set to 0.	R/W
b5	—			
b6	—			
b7	FMR27	Low-current-consumption read mode enable bit (1, 3)	0: Low-current-consumption read mode disabled 1: Low-current-consumption read mode enabled	R/W

Notes:
1. To set this bit to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
2. To set the FMR21 bit to 0 (erase restart), set it when the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled).
3. Set the FMR27 bit to 1 after setting either of the following:
   • Set the CPU clock to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
   • Set the CPU clock to the XCIN clock divided by 1 (no division), 2, 4, or 8.
   Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
   Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

FMR20 Bit (Erase-Suspend Enable Bit)

When the FMR20 bit is set to 1 (enabled), the erase-suspend function is enabled.

FMR21 Bit (Erase-Suspend Request Bit)

When the FMR21 bit is set to 1, erase-suspend mode is entered. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) when an interrupt request for the enabled interrupt is generated, and erase-suspend mode is entered. To restart auto-erasure, set the FMR21 bit to 0 (erase restart).

[Condition for setting to 0]
Set to 0 by a program.
[Conditions for setting to 1]
- When the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request) at the time an interrupt is generated.
- Set to 1 by a program.

FMR22 Bit (Interrupt Request Suspend-Request Enable Bit)

When the FMR 22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request) at the time an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when using erase-suspend while rewriting the user ROM area in EW1 mode.

FMR27 Bit (Low-Current-Consumption Read Mode Enable Bit)

When the FMR 27 bit is set to 1 (low-current-consumption read mode enabled) in low-speed clock mode (XIN clock stopped) or low-speed on-chip oscillator mode (XIN clock stopped), power consumption when reading the flash memory can be reduced. Refer to **27.2.10 Low-Current-Consumption Read Mode** for details.
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:

- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
- The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).
When the FMR27 bit is set to 1 (low-current-consumption read mode enabled), do not execute the program, block erase, or lock bit program command. To change the FMSTP bit from 1 (flash memory stops) to 0 (flash memory operates), make the setting when the FMR27 bit is set to 0 (low-current-consumption read mode disabled).

26.4.5 EW0 Mode

When the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), the MCU enters CPU rewrite mode and software commands can be accepted. At this time, the FMR02 bit in the FMR0 register is set to 0 so that EW0 mode is selected.

Software commands are used to control program and erase operations. The FST register can be used to confirm whether programming or erasure has completed.

To enter erase-suspend during auto-erasure, set the FMR20 bit to 1 (erase-suspend enabled) and the FMR21 bit to 1 (erase-suspend request). Next, verify that the FST7 bit in the FST register is set to 1 (ready), and then verify the FST6 bit is set to 1 (during erase-suspend) before accessing the flash memory. When the FST6 bit is set to 0, erasure completes.

When the FMR21 bit in the FMR2 register is set to 0 (erase restart), auto-erasure restarts. To confirm whether auto-erasure has restarted, first verify that the FST7 bit in the FST register is set to 0, and then verify that the FST6 bit is set to 0 (other than erase-suspend).

26.4.6 EW1 Mode

After the FMR01 bit in the FMR0 register is set to 1 (CPU rewrite mode enabled), EW1 mode is selected by setting the FMR02 bit is set to 1.

The FST register can be used to confirm whether programming and erasure has completed.

To enable the erase-suspend function during auto-erasure, execute the block erase command after setting the FMR20 bit in the FMR2 register to 1 (suspend enabled). To enter erase-suspend while auto-erasing the user ROM area, set the FMR22 bit in the FMR2 register to 1 (erase-suspend request enabled by interrupt request). Also, the interrupt to enter erase-suspend must be enabled beforehand.

When an interrupt request is generated, the FMR21 bit in the FMR2 register is automatically set to 1 (erase-suspend request) and auto-erasure suspends after td(SR-SUS). After interrupt handling completes, set the FMR21 bit to 0 (erase restart) to restart auto-erasure.

26.4.7 Suspend Operation

The suspend function halts the auto-erase operation temporarily during auto-erasure.
When auto-erasure is suspended, the next operation can be executed (refer to **Table 26.4 Executable Operation during Suspend**).

- When suspending the auto-erasure of any block in data flash, auto-programming and reading another block can be executed.
- When suspending the auto-erasure of data flash, auto-programming and reading program ROM can be executed.
- When suspending the auto-erasure of any block in program ROM, auto-programming and reading another block can be executed.
- When suspending the auto-erasure of program ROM, auto-programming and reading data flash can be executed.
- To check the suspend, first verify that the FST7 bit is set to 1 (ready), and then verify that the FST6 bit is set to 1 (during erase-suspend) to confirm whether erasure has been suspended. When the FST6 bit is set to 0 (other than erase suspend), erasure completes.

Figure 26.3 shows the Suspend Operation Timing.

Table 26.4 Executable Operation during Suspend

		Operation during Suspend											
		Data flash (Block during erasure execution before entering suspend)			Data flash (Block during no erasure execution before entering suspend)			Program ROM (Block during erasure execution before entering suspend)			Program ROM (Block during no erasure execution before entering suspend)		
		Erase	Program	Read	Erase	Program	Read	Erase	Program	Read	Erase	Program	Read
Areas during erasure execution before entering suspend	Data flash	D	D	D	D	E	E	N/A	N/A	N/A	D	E	E (5)
	Program ROM	N/A	N/A	N/A	D	E	E	D	D	D	D	E	E

Notes:
1. E indicates operation is enabled by using the suspend function, D indicates operation is disabled, and N/A indicates no combination is available.
2. Operation cannot be suspended during programming.
3. The block erase command can be executed for erasure. The program, lock bit program, and read lock bit status commands can be executed for programming.
   The clear status register command can be executed when the FST7 bit in the FST register is set to 1 (ready).
   The block blank check operation is disabled during suspend.
4. The MCU enters read array mode immediately after entering erase-suspend.
5. The program ROM area can be read with the BGO function while programming or block erasing data flash.

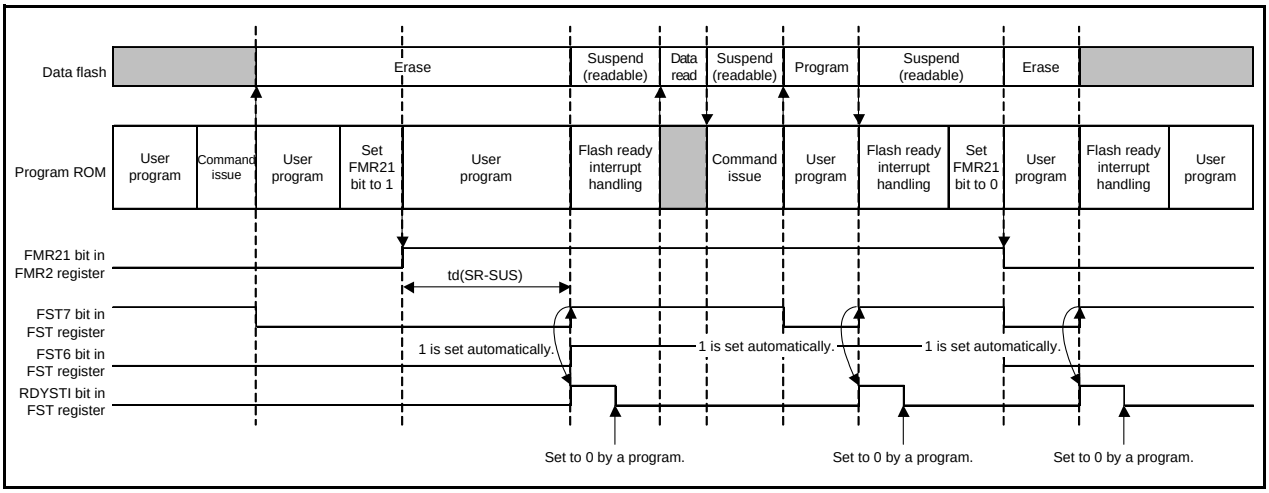


Figure 26.3 Suspend Operation Timing

26.4.8 How to Set and Exit Each Mode

Figure 26.4 shows How to Set and Exit EW0 Mode and Figure 26.5 shows How to Set and Exit EW0 Mode (When Rewriting Data Flash) and EW1 Mode.

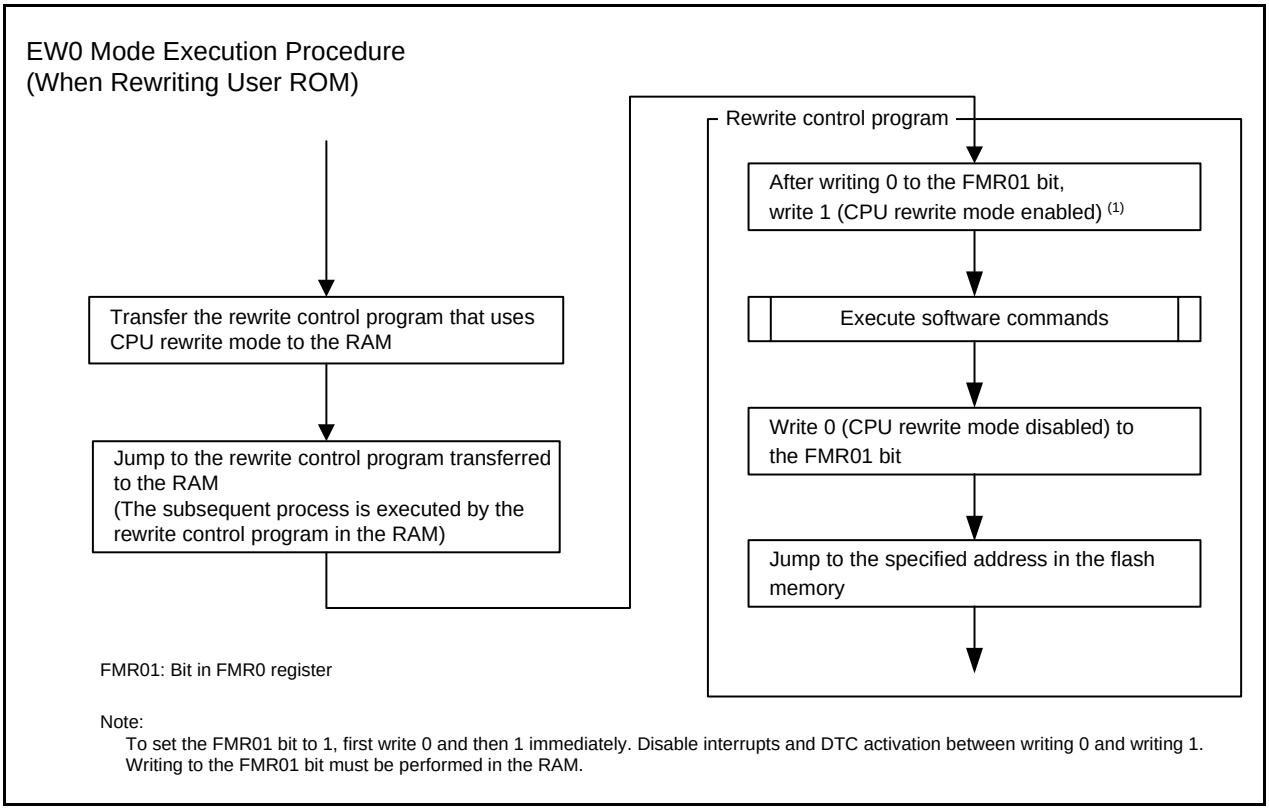


Figure 26.4 How to Set and Exit EW0 Mode

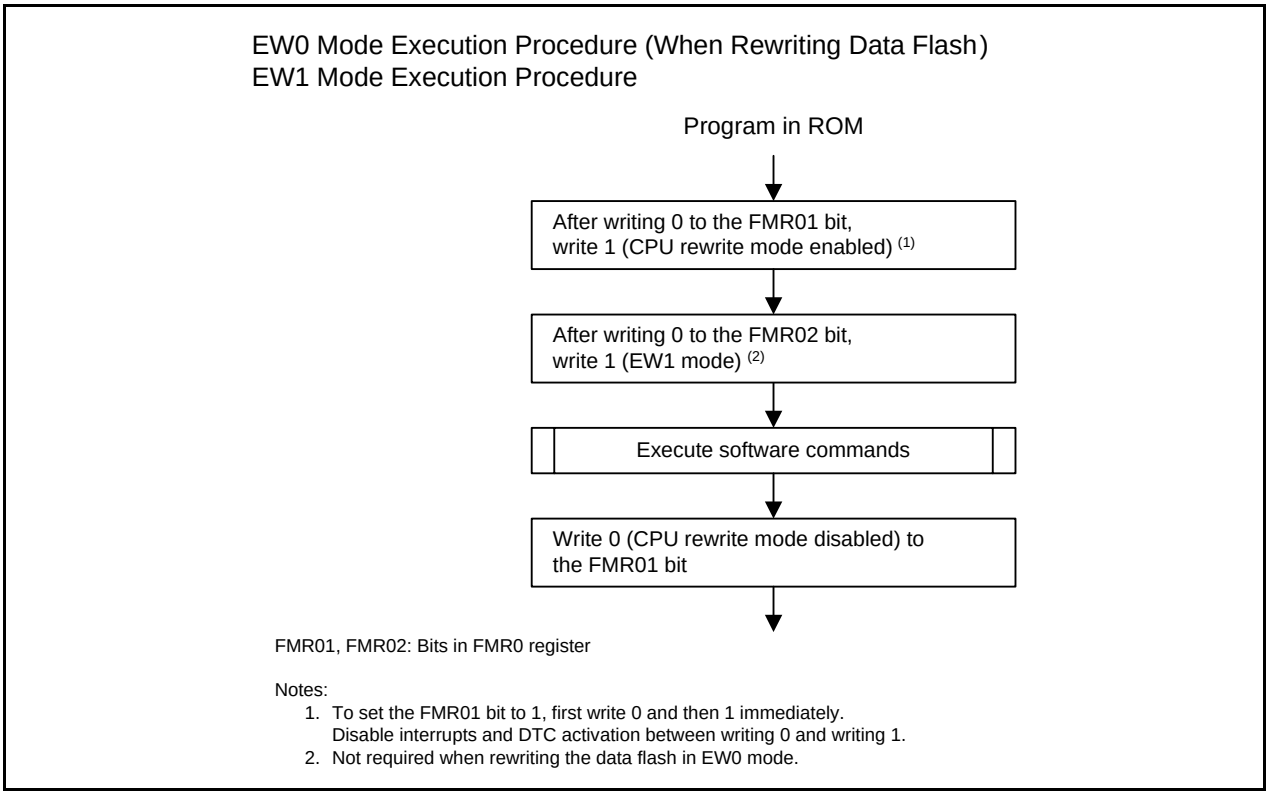


Figure 26.5 How to Set and Exit EW0 Mode (When Rewriting Data Flash) and EW1 Mode

26.4.9 BGO (BackGround Operation) Function

When the program ROM area is specified while a program or block erase operation to the data flash, array data can be read. This eliminates the need for writing software commands. Access time is the same as for normal read operations.
Any other block of the data flash cannot read during a program or block erase operation to the data flash.
Figure 26.6 shows the BGO Function.

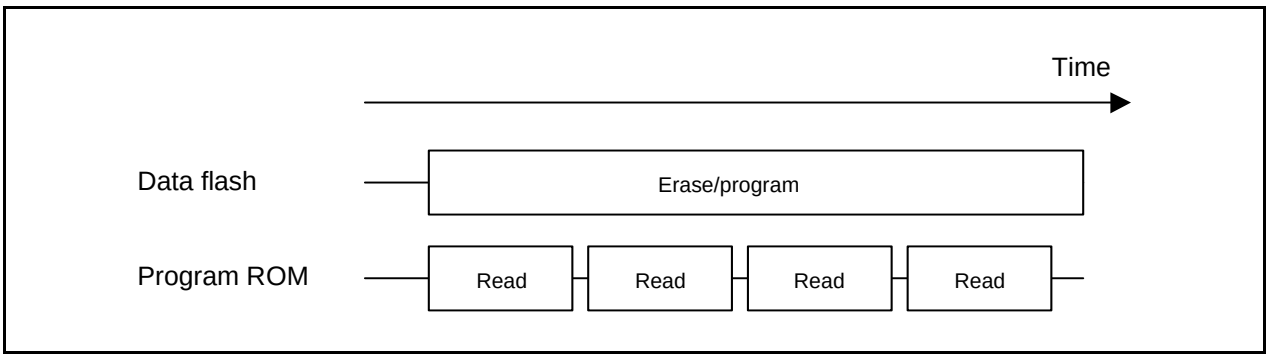


Figure 26.6 BGO Function

26.4.10 Data Protect Function

Each block in the program ROM has a nonvolatile lock bit. The lock bit is enabled by setting the FMR13 bit in the FMR1 register is set to 0 (lock bit enabled). The lock bit can be used to disable (lock) programming or erasing each block. This prevents data from being written or erased inadvertently. A block status changes according to the lock bit as follows:

- When the lock bit data is set to 0: locked (the block cannot be programmed or erased)
- When the lock bit data is set to 1: not locked (the block can be programmed and erased)

The lock bit data is set to 0 (locked) by executing the lock bit program command and to 1 (not locked) by erasing the block. No commands can be used to set only the lock bit data to 1.
The lock bit data can be read using the read lock bit status command.

When the FMR13 bit is set to 1 (lock bit disabled), the lock bit function is disabled and all blocks are not locked (each lock bit data remains unchanged). The lock bit function is enabled by setting the FMR13 bit to 0 (the lock bit data is retained).
When the block erase command is executed while the FMR13 bit is set to 1, the target block is erased regardless of the lock bit status. The lock bit of the erase target block is set to 1 after auto-erasure completes.
Refer to **26.4.11 Software Commands** for the details of individual commands.
The FMR13 bit is set to 0 after auto-erasure completes. This bit is also set to 0 if one of the following conditions is met. To erase or program a different locked block, set the FMR13 bit to 1 again and execute the block erase or program command.

- If the FST7 bit in the FST register is changed from 0 (busy) to 1 (ready).
- If a command sequence error occurs.
- If the FMR01 bit in the FMR0 register is set to 0 (CPU mode disabled).
- If the FMSTP bit in the FMR0 register is set to 1 (flash memory stops).
- If the CMDRST bit in the FMR0 register is set to 1 (erasure/writing stopped).

Figure 26.7 shows the FMR13 Bit Operation Timing.

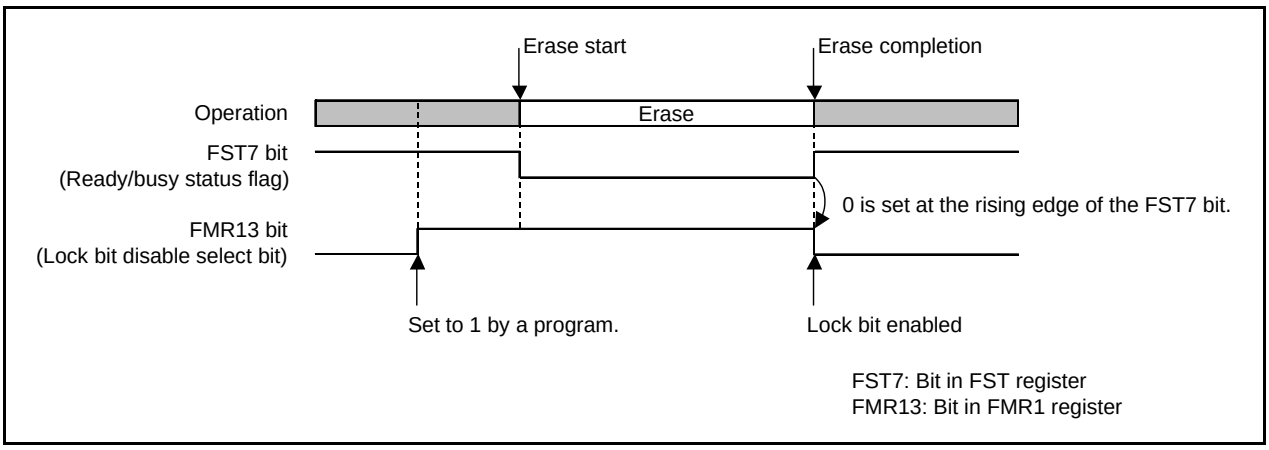


Figure 26.7 FMR13 Bit Operation Timing

26.4.11 Software Commands

The software commands are described below. Read or write commands and data in 8-bit units.
Do not input any command other than those listed in the table below.

Table 26.5 Software Commands

Command	First Bus Cycle			Second Bus Cycle		
	Mode	Address	Data	Mode	Address	Data
Read array	Write	×	FFh			
Clear status register	Write	×	50h			
Program	Write	WA	40h	Write	WA	WD
Block erase	Write	×	20h	Write	BA	D0h
Lock bit program	Write	BT	77h	Write	BT	D0h
Read lock bit status	Write	×	71h	Write	BT	D0h
Block blank check	Write	×	25h	Write	BA	D0h

WA: Write address
WD: Write data
BA: Any block address
BT: Starting block address
×: Any address in the user ROM area

26.4.11.1 Read Array Command

The read array command is used to read the flash memory.
When FFh is written in the first bus cycle, the MCU enters read array mode. When the read address is input in the following bus cycles, the content of the specified address can be read in 8-bit units.
Since read array mode remains until another command is written, the contents of multiple addresses can be read continuously.
In addition, after a reset, the MCU enters read array mode after a program, block erase, block blank check, read lock bit status, or clear status register command, or after entering erase-suspend.

26.4.11.2 Clear Status Register Command

The clear status register command is used to set bits FST4 and FST5 in the FST register to 0.
When 50h is written in the first bus cycle, bits FST4 and FST5 in the FST register are set to 0.

26.4.11.3 Program Command

The program command is used to write data to the flash memory in 1-byte units.
When 40h is written in the first bus cycle and data is written in the second bus cycle to the write address, auto-programming (data program and verify operation) starts. Make sure the address value specified in the first bus cycle is the same address as the write address specified in the second bus cycle.
The FST7 bit in the FST register can be used to confirm whether auto-programming has completed. The FST7 bit is set to 0 during auto-programming and is set to 1 when auto-programming completes.
After auto-programming has completed, the auto-program result can be confirmed by the FST4 bit in the FST register (refer to **26.4.12 Full Status Check**).
Do not write additions to the already programmed addresses.

The program command targeting each block in the program ROM can be disabled using the lock bit.
The following commands are not accepted under the following conditions:

- Block program commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Block program commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).
- Block program commands targeting data flash block C when the FMR16 bit is set to 1 (rewrite disabled).
- Block program commands targeting data flash block D when the FMR17 bit is set to 1 (rewrite disabled).

Figure 26.8 shows a Program Flowchart (Flash Ready Status Interrupt Disabled) and Figure 26.9 shows a Program Flowchart (Flash Ready Status Interrupt Enabled).

In EW1 mode, do not execute this command to any address where a rewrite control program is allocated.

When the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-programming. The auto-program result can be confirmed by reading the FST register during the interrupt routine.

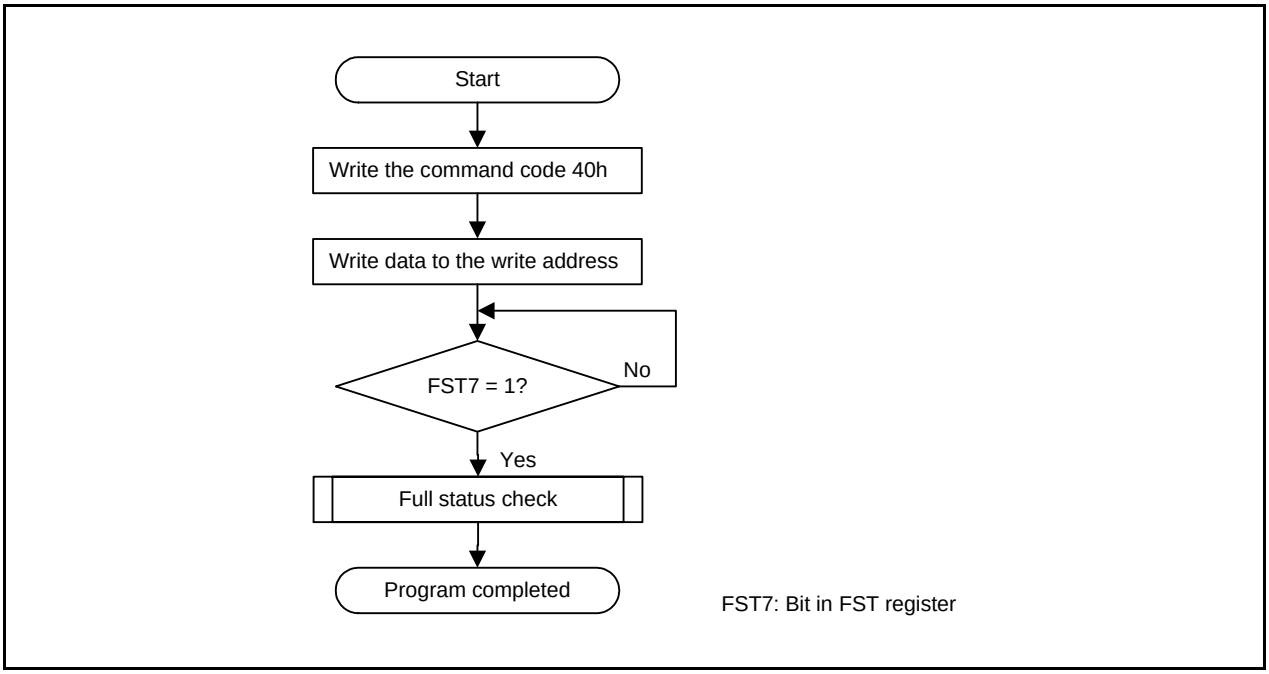


Figure 26.8 Program Flowchart (Flash Ready Status Interrupt Disabled)

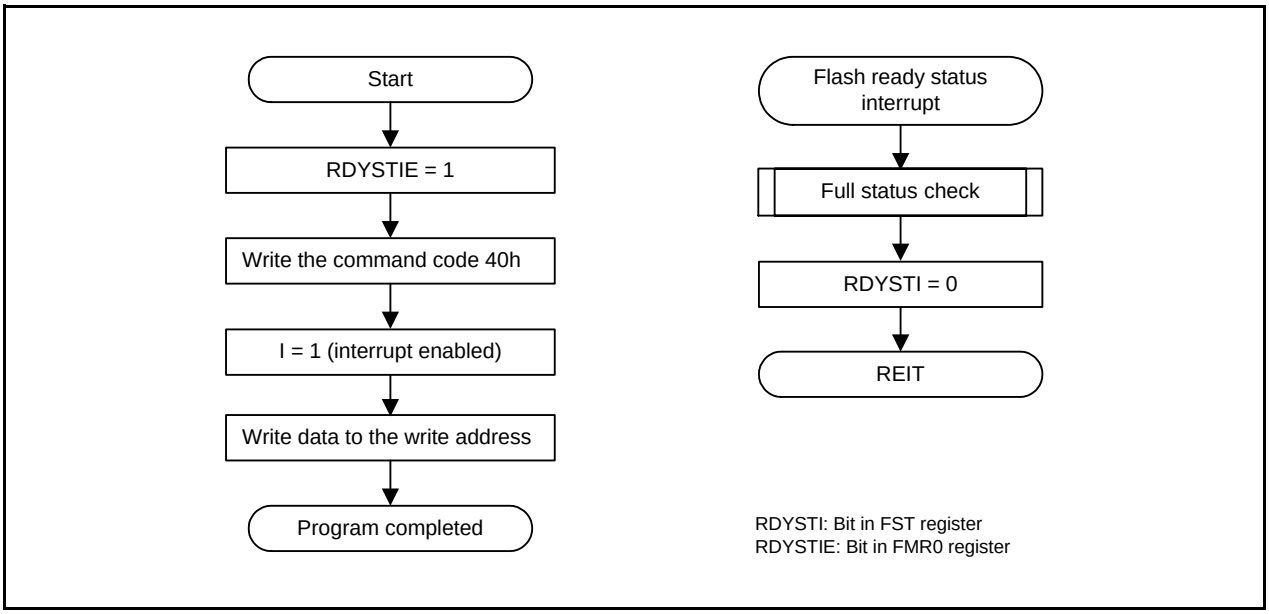


Figure 26.9 Program Flowchart (Flash Ready Status Interrupt Enabled)

26.4.11.4 Block Erase Command

When 20h is written in the first bus cycle and then D0h is written in the second bus cycle to any block address, auto-erasure (erase and erase verify operation) starts in the specified block.
The FST7 bit in the FST register can be used to confirm whether auto-erasure has completed. The FST7 bit is set to 0 during auto-erasure and is set to 1 when auto-erasure completes. After auto-erasure completes, all data in the block is set to FFh.
After auto-erasure has completed, the auto-erase result can be confirmed by the FST5 bit in the FST register (refer to **26.4.12 Full Status Check**).

The block erase command targeting each block in the program ROM can be disabled using the lock bit.
The following commands are not accepted under the following conditions:

- Block erase commands targeting data flash block A when the FMR14 bit in the FMR1 register is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block B when the FMR15 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block C when the FMR16 bit is set to 1 (rewrite disabled).
- Block erase commands targeting data flash block D when the FMR17 bit is set to 1 (rewrite disabled).

Figure 26.10 shows a Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled), Figure 26.11 shows a Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled), Figure 26.12 shows a Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled), and Figure 26.13 shows a Block Erase Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled).

In EW1 mode, do not execute this command to any block where a rewrite control program is allocated.

While the RDYSTIE bit in the FMR0 register is set to 1 (flash ready status interrupt enabled), a flash ready status interrupt can be generated upon completion of auto-erasure. While the RDYSTIE bit is set to 1 and the FMR20 bit in the FMR2 register is set to 1 (erase-suspend enabled), a flash ready status interrupt is generated when the FMR21 bit is set to 1 (erase-suspend request) and auto-erasure suspends. The auto-erase result can be confirmed by reading the FST register during the interrupt routine.

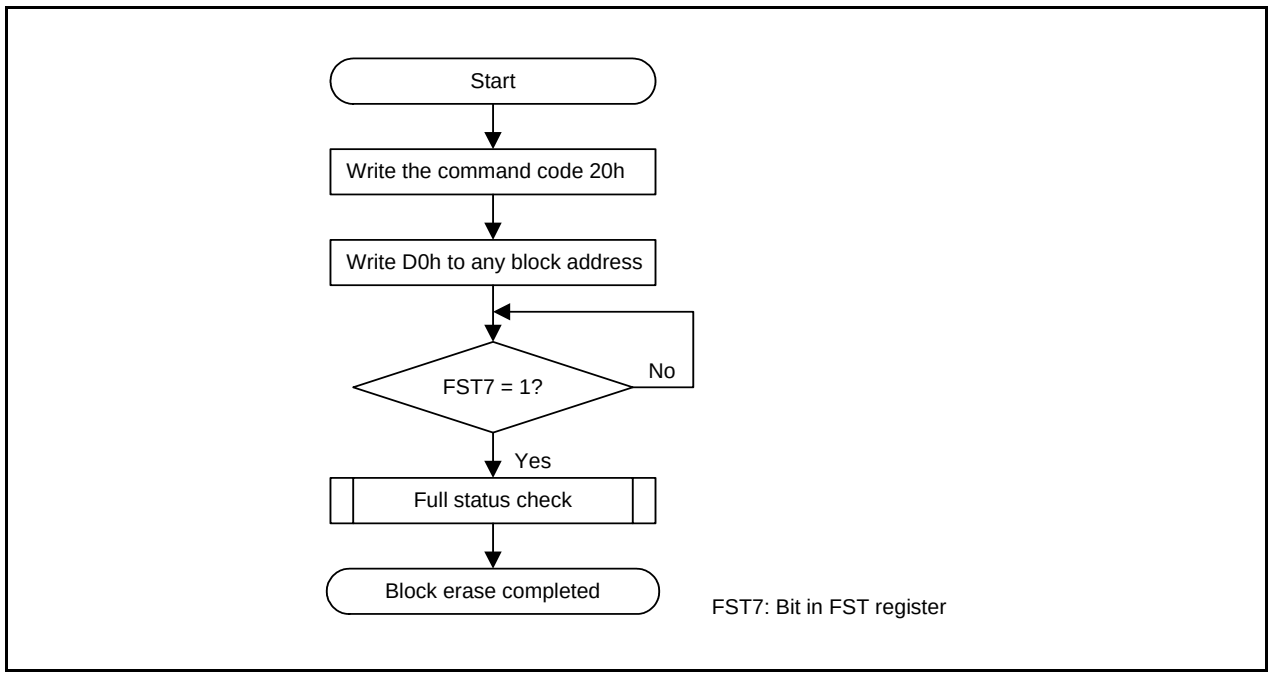
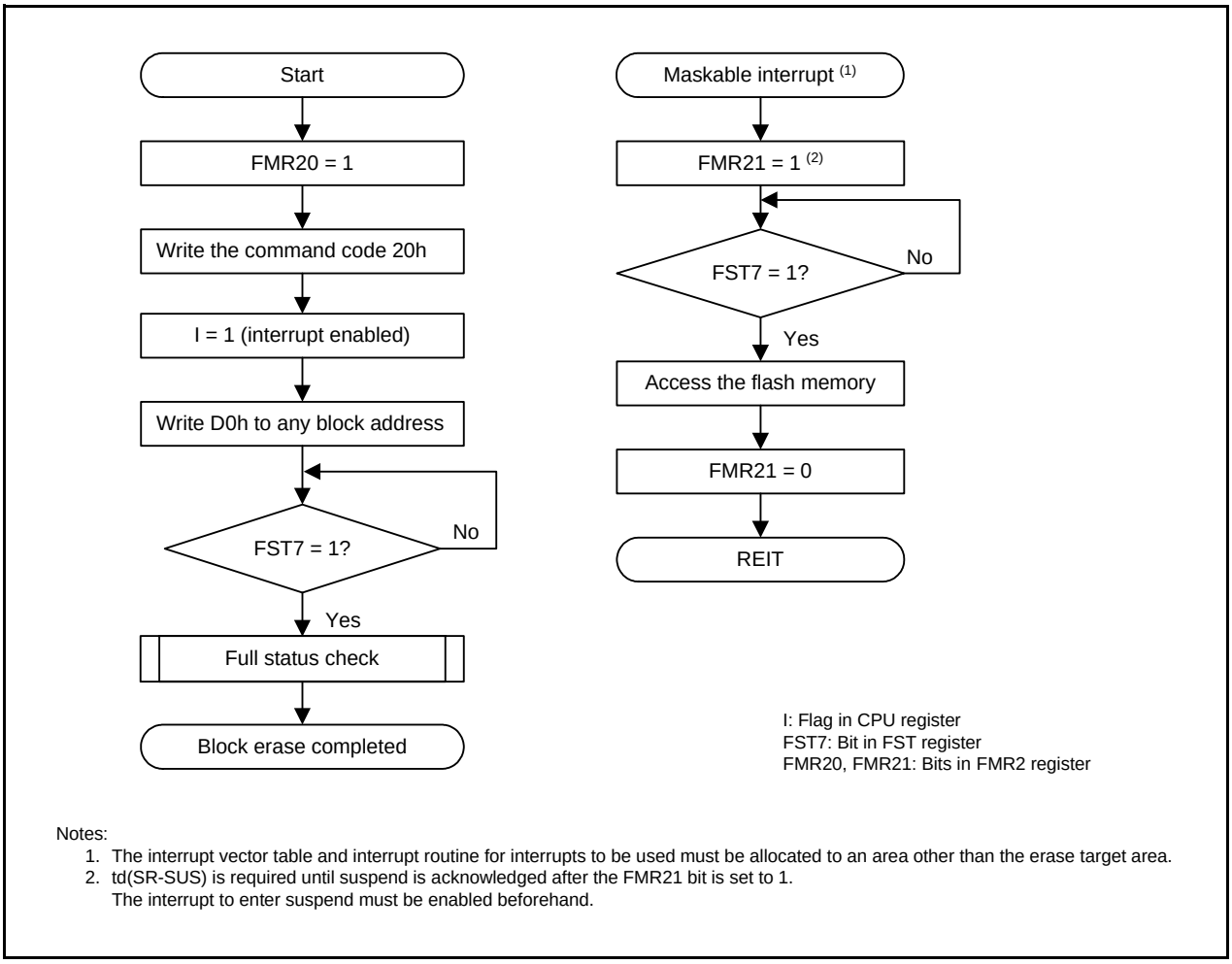
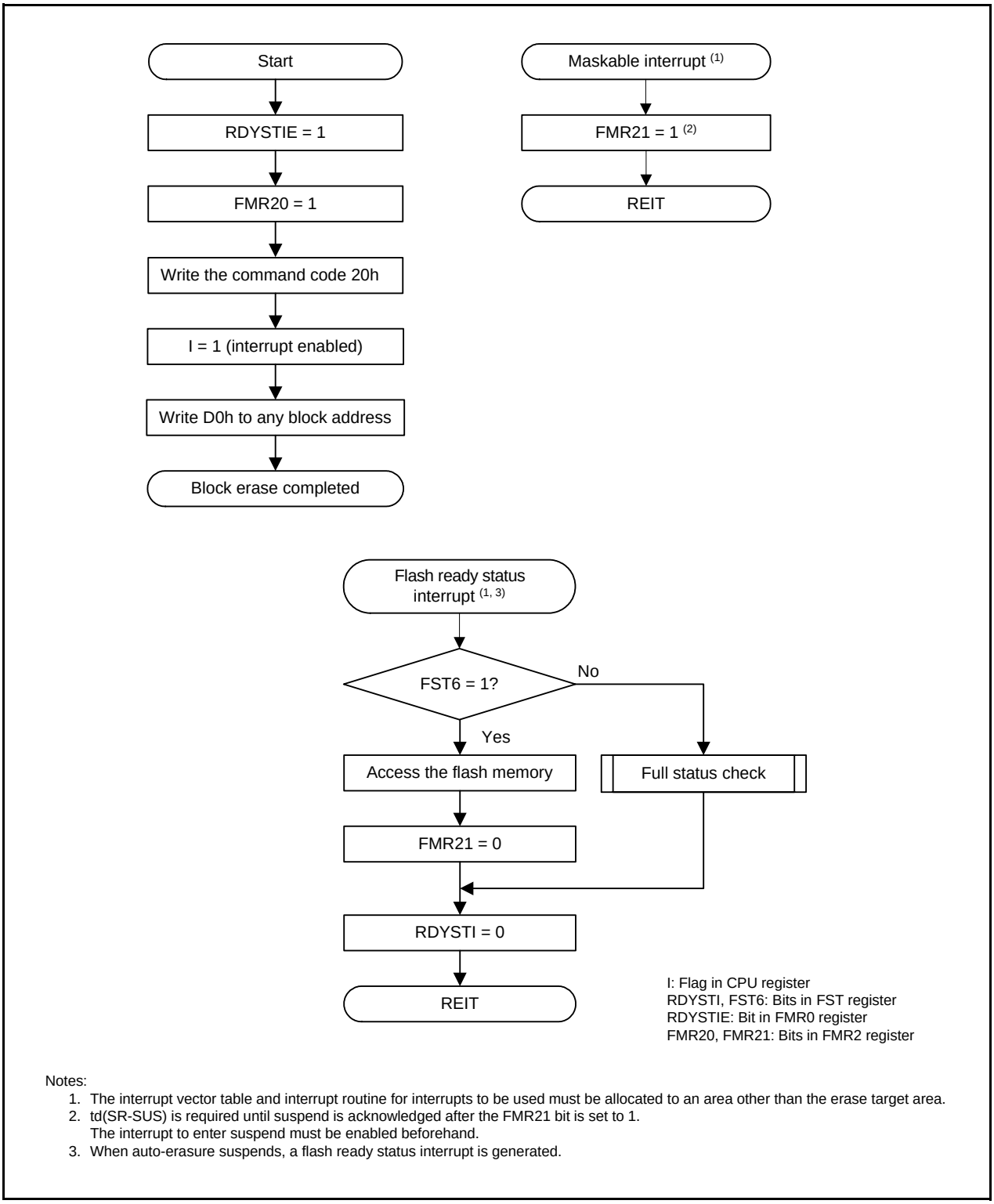


Figure 26.10 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.

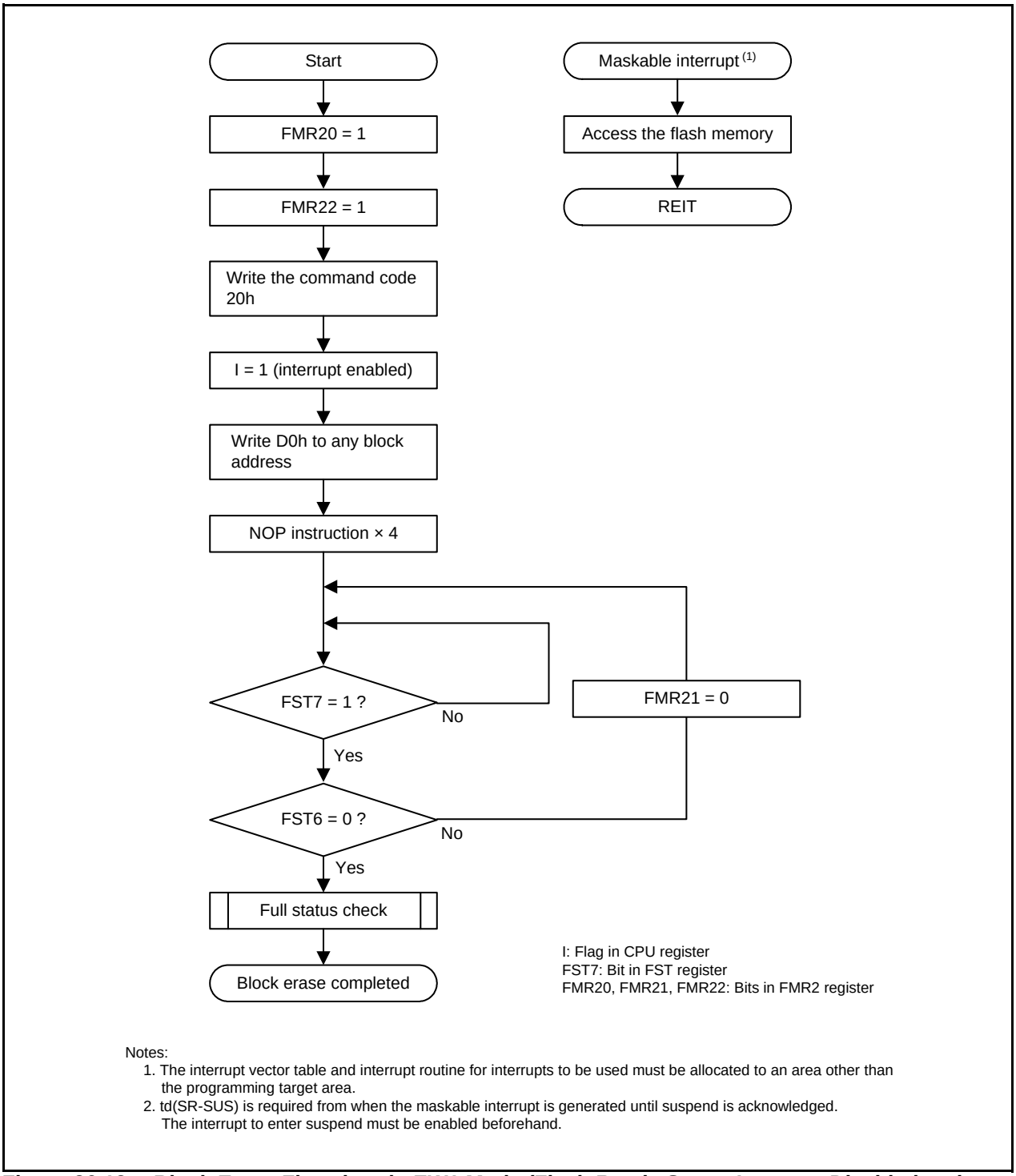
Figure 26.11 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the erase target area.
2. td(SR-SUS) is required until suspend is acknowledged after the FMR21 bit is set to 1.
   The interrupt to enter suspend must be enabled beforehand.
3. When auto-erasure suspends, a flash ready status interrupt is generated.

Figure 26.12 Block Erase Flowchart in EW0 Mode (Flash Ready Status Interrupt Enabled and Suspend Enabled)

When the FMR 22 bit is set to 1 (suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (suspend request) when an interrupt request is generated during auto-erasure. Set the FMR22 bit to 1 when suspend is used while the user ROM area is auto-erased in EW1 mode.



Notes:
1. The interrupt vector table and interrupt routine for interrupts to be used must be allocated to an area other than the programming target area.
2. td(SR-SUS) is required from when the maskable interrupt is generated until suspend is acknowledged. The interrupt to enter suspend must be enabled beforehand.

Figure 26.13 Block Erase Flowchart in EW1 Mode (Flash Ready Status Interrupt Disabled and Suspend Enabled)

26.4.11.5 Lock Bit Program Command

This command is used to set the lock bit of any block in the program ROM area to 0 (locked).
When 77h is written in the first bus cycle and D0h is written in the second bus cycle to the starting block address, 0 is written to the lock bit of the specified block. Make sure the address value in the first bus cycle is the same address as the starting block address specified in the second bus cycle.
Figure 26.14 shows a Lock Bit Program Flowchart. The lock bit status (lock bit data) can be read using the read lock bit status command.
The FST7 bit in the FST register can be used to confirm whether writing to the lock bit has completed.
Refer to **26.4.10 Data Protect Function** for the lock bit function and how to set the lock bit to 1 (not locked).

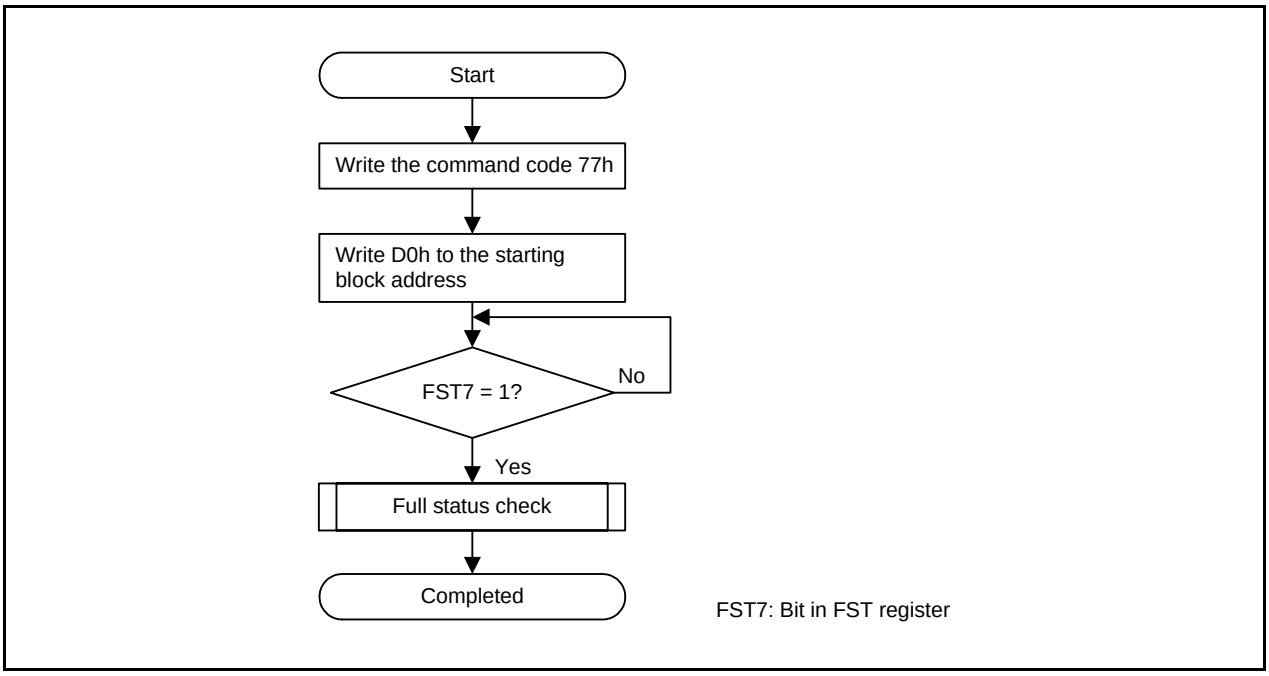


Figure 26.14 Lock Bit Program Flowchart

26.4.11.6 Read Lock Bit Status Command

This command is used to read the lock bit status of any block in the program ROM area.
When 71h is written in the first bus cycle and D0h is written in the second cycle to the starting block address, the lock bit status of the specified block is stored in the LBDATA bit in the FST register. After the FST7 bit in the FST register has been set to 1 (ready), read the LBDATA bit.
Figure 26.15 shows a Read Lock Bit Status Flowchart.

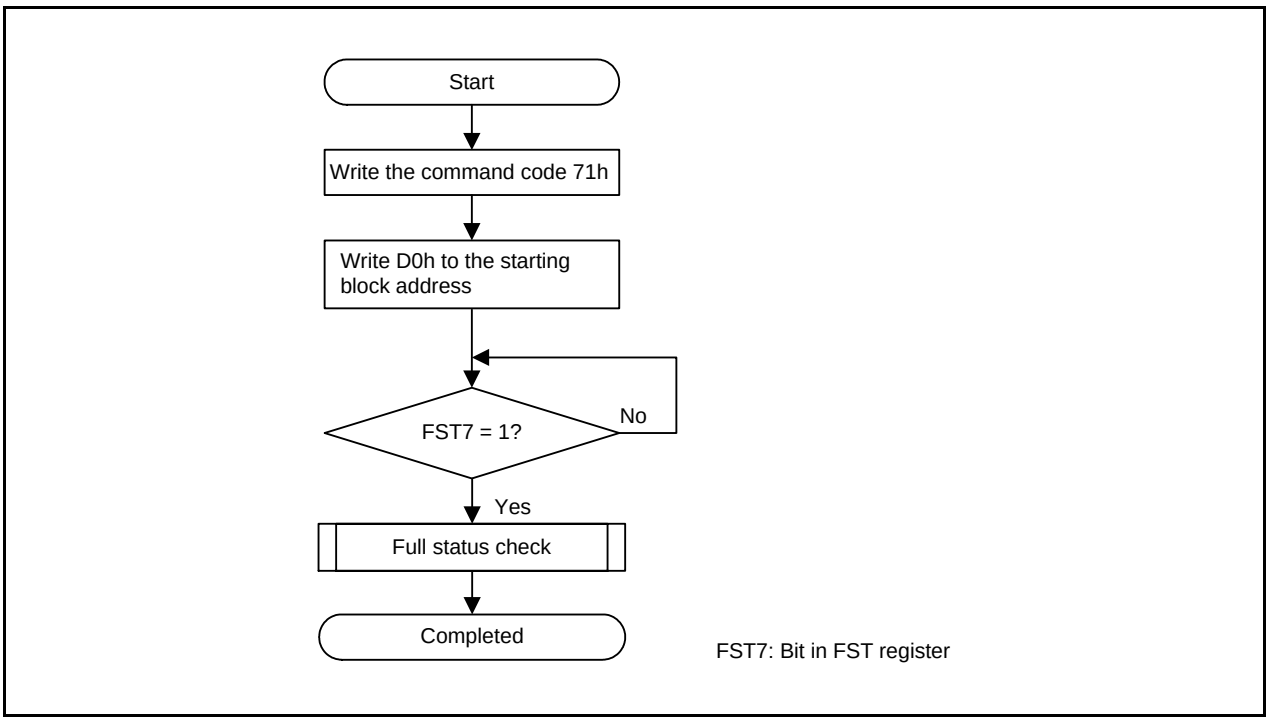


Figure 26.15 Read Lock Bit Status Flowchart

26.4.11.7 Block Blank Check Command

This command is used to confirm that all addresses in any block are blank data FFh.
When 25h is written in the first bus cycle and D0h is written in the second bus cycle to any block address, blank checking starts in the specified block. The FST7 bit in the FST register can be used to confirm whether blank checking has completed. The FST7 bit is set to 0 during the blank-check period and set to 1 when blank checking completes.
After blank checking has completed, the blank-check result can be confirmed by the FST5 bit in the FST register (refer to **26.4.12 Full Status Check**). This command is used to verify that the target block has not been written to. To confirm whether erasure has completed normally, execute the full status check.

Do not execute the block blank check command when the FST6 bit is set to 1 (during erase-suspend).
Figure 26.16 shows a Block Blank Check Flowchart.

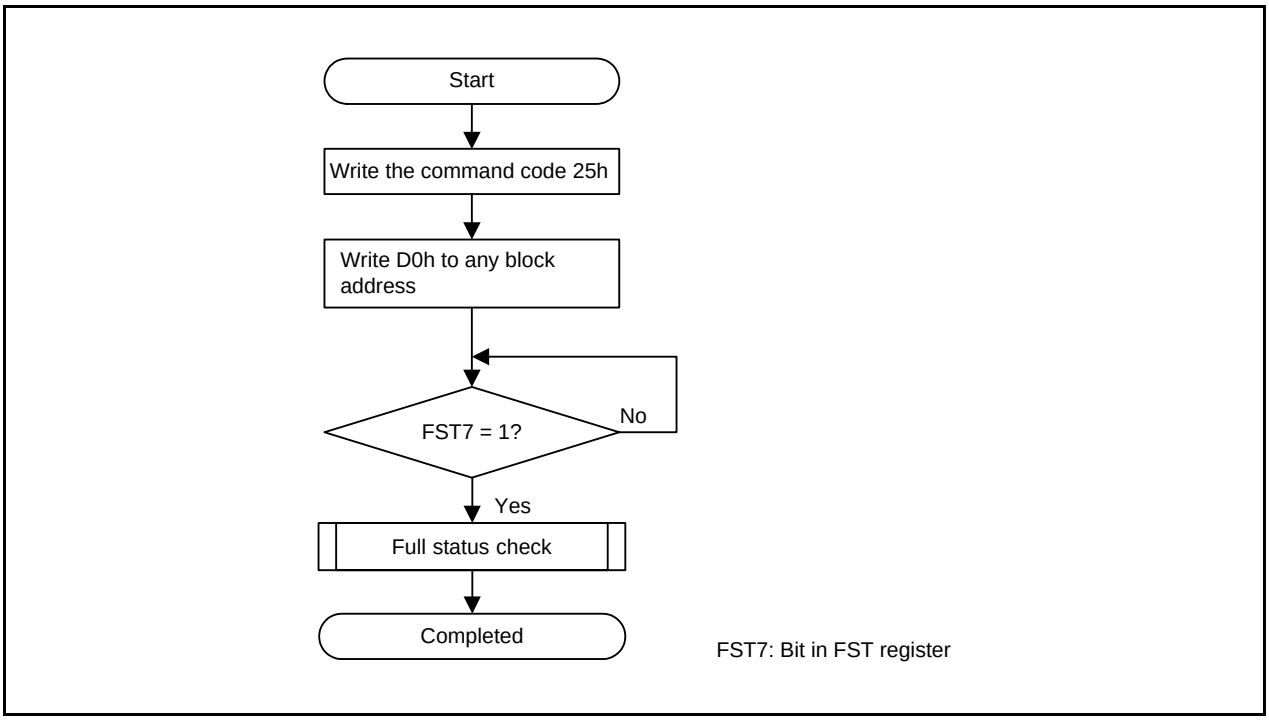


Figure 26.16 Block Blank Check Flowchart

This command is intended for programmer manufactures, not for general users.

26.4.12 Full Status Check

If an error occurs, bits FST4 and FST5 in the FST register are set to 1, indicating the occurrence of an error. The execution result can be confirmed by checking these status bits (full status check).
Table 26.6 lists the Errors and FST Register Status. Figure 26.17 shows the Full Status Check and Handling Procedure for Individual Errors.

Table 26.6 Errors and FST Register Status

FST Register Status		Error	Error Occurrence Condition
FST5	FST4		
1	1	Command sequence error	• When a command is not written correctly. • When data other than valid data (i.e., D0h or FFh) is written in the second bus cycle of the block erase command. (1) • The erase command is executed during suspend • A command is executed for a block during suspend
1	0	Erase error	When the block erase command is executed, but auto-erasure does not complete correctly.
		Blank check error	When the block blank check command is executed and data other than blank data FFh is read.
0	1	Program error	When the program command is executed, but auto-programming does not complete correctly.
		Lock bit program error	When the program command is executed, but the lock bit is not set to 1 (locked).

Note:
1. When FFh is written in the second bus cycle of these commands, the MCU enters read array mode. At the same time, the command code written in the first bus cycle is invalid.

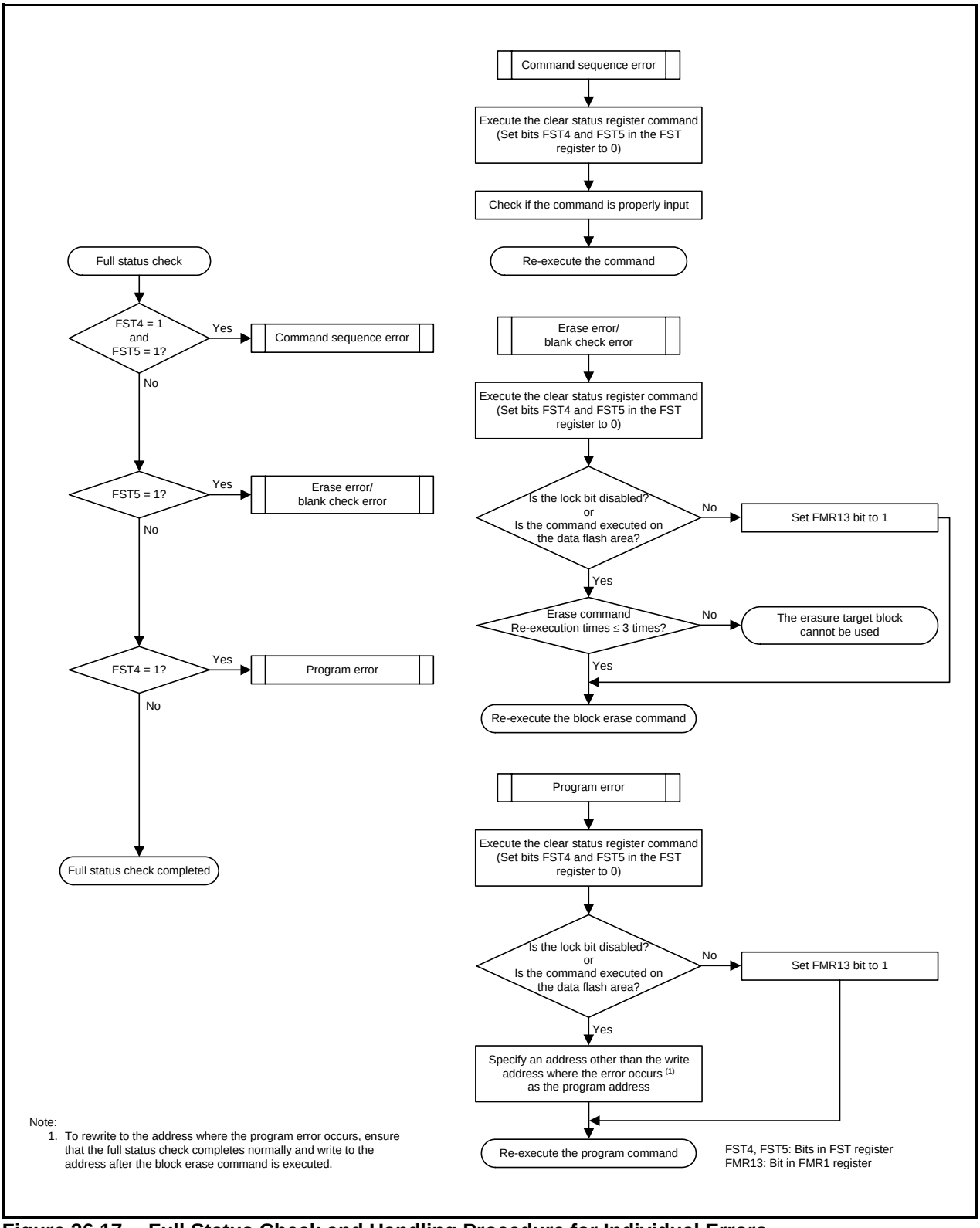


Figure 26.17 Full Status Check and Handling Procedure for Individual Errors

26.5 Standard Serial I/O Mode

In standard serial I/O mode, a serial programmer which supports the MCU can be used to rewrite the user ROM area while the MCU is mounted on-board.
There are three types of standard serial I/O modes:

- Standard serial I/O mode 1 ..... Clock synchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 2 ..... Clock asynchronous serial I/O used to connect to a serial programmer
- Standard serial I/O mode 3 ..... Special clock asynchronous serial I/O used to connect to a serial programmer

Standard serial I/O mode 2 and standard serial I/O mode 3 can be used for the MCU.

Refer to **Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator** for examples of connecting to a serial programmer. Contact the serial programmer manufacturer for more information. Refer to the user's manual included with your serial programmer for instructions.

Table 26.7 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 2) and Figure 26.18 shows Pin Handling in Standard Serial I/O Mode 2. Table 26.8 lists the Pin Functions (Flash Memory Standard Serial I/O Mode 3) and Figure 26.19 shows Pin Handling in Standard Serial I/O Mode 3.
After handling the pins shown in Table 26.8 and rewriting the flash memory using the programmer, apply a "H" level signal to the MODE pin and reset the hardware to run a program in the flash memory in single-chip mode.

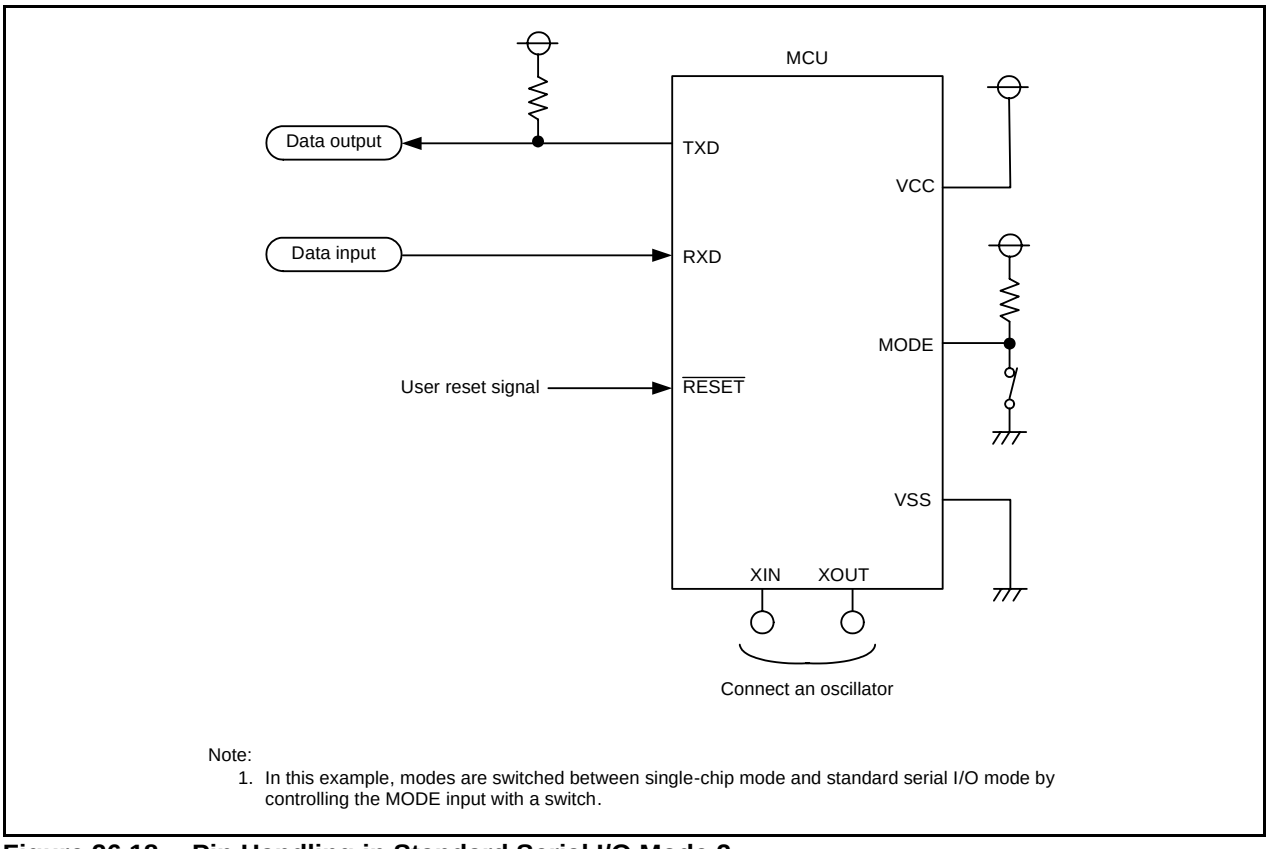
26.5.1 ID Code Check Function

The ID code check function determines whether the ID codes sent from the serial programmer and those written in the flash memory match.
Refer to **12. ID Code Areas** for details of the ID code check.

Table 26.7 Pin Functions (Flash Memory Standard Serial I/O Mode 2)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
XIN	Clock input	I	Connect a crystal oscillator between pins XIN and XOUT.
XOUT	Clock output	I/O	
P4_3/XCIN	P4_3 input/clock input	I	If an external oscillator is connected, connect a crystal oscillator between pins XCIN and XCOUT. To use as an input port, input a “H” or “L” level signal or leave the pin open.
P4_4/XCOUT	P4_4 input/clock output	I/O	
P0_4	Input port P0	I	Input a “H” or “L” level signal or leave open.
P1_0 to P1_3, P1_6, P1_7	Input port P1	I	Input a “H” or “L” level signal or leave open.
P3_0, P3_1, P3_3 to P3_5, P3_7	Input port P3	I	Input a “H” or “L” level signal or leave open.
P4_5	Input port P4	I	Input a “H” or “L” level signal or leave open.
MODE	MODE	I/O	Input a “L” level signal.
P1_4	TXD output	O	Serial data output pin.
P1_5	RXD input	I	Serial data input pin.

I: Input O: Output I/O: Input and output



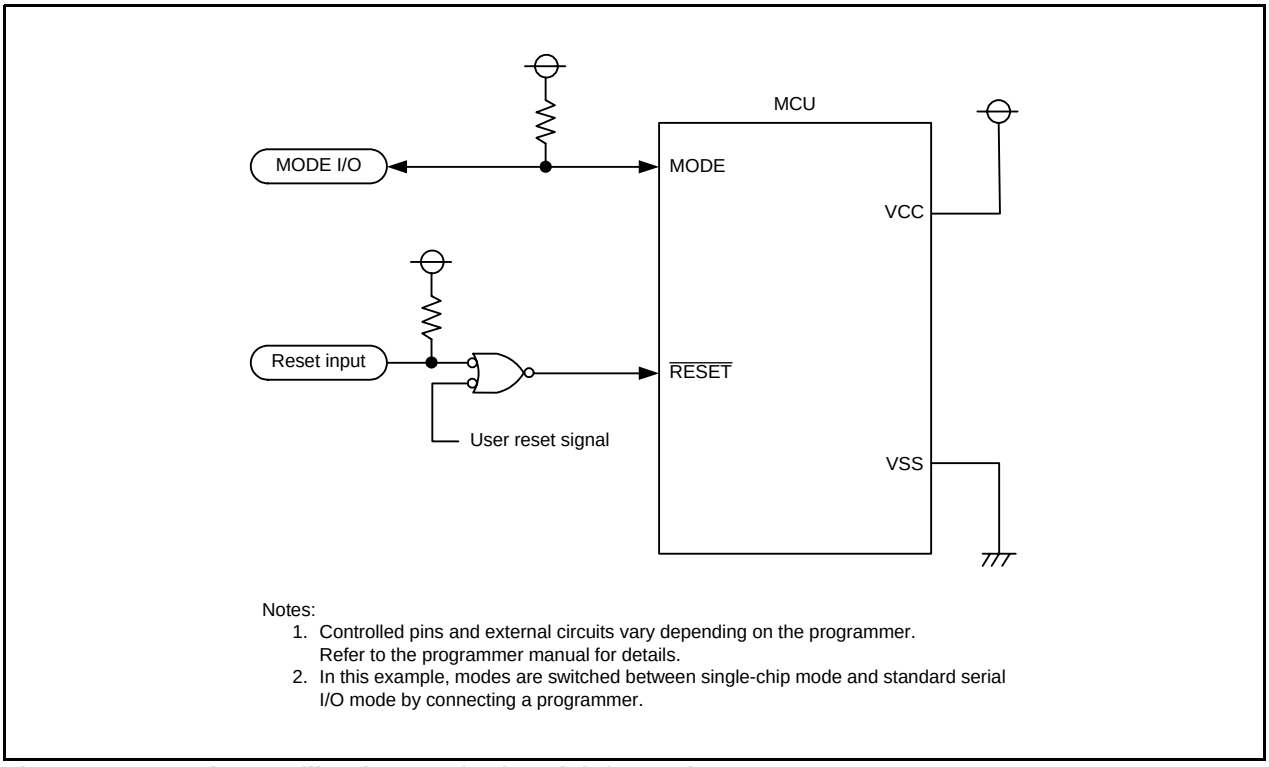
Note:
1. In this example, modes are switched between single-chip mode and standard serial I/O mode by controlling the MODE input with a switch.

Figure 26.18 Pin Handling in Standard Serial I/O Mode 2

Table 26.8 Pin Functions (Flash Memory Standard Serial I/O Mode 3)

Pin	Name	I/O	Description
VCC, VSS	Power supply input		Apply the guaranteed programming and erasure voltage to the VCC pin and 0 V to the VSS pin.
$\overline{\text{RESET}}$	Reset input	I	Reset input pin.
XIN	Clock input	I	Connect a crystal oscillator between pins XIN and XOUT.
XOUT	Clock output	I/O	
P4_3/XCIN	P4_3 input/clock input	I	If an external oscillator is connected, connect a crystal oscillator between pins XCIN and XCOUT. To use as an input port, input a “H” or “L” level signal or leave the pin open.
P4_4/XCOUT	P4_4 input/clock output	I/O	
P0_4	Input port P0	I	Input a “H” or “L” level signal or leave open.
P1_0 to P1_7	Input port P1	I	Input a “H” or “L” level signal or leave open.
P3_0, P3_1, P3_3 to P3_5, P3_7	Input port P3	I	Input a “H” or “L” level signal or leave open.
P4_5	Input port P4	I	Input a “H” or “L” level signal or leave open.
MODE	MODE	I/O	Serial data I/O pin. Connect the pin to a programmer.

I: Input O: Output I/O: Input and output



Notes:
1. Controlled pins and external circuits vary depending on the programmer. Refer to the programmer manual for details.
2. In this example, modes are switched between single-chip mode and standard serial I/O mode by connecting a programmer.

Figure 26.19 Pin Handling in Standard Serial I/O Mode 3

26.6 Parallel I/O Mode

Parallel I/O mode is used to input and output software commands, addresses and data necessary to control (read, program, and erase) the on-chip flash memory.
Use a parallel programmer which supports the MCU. Contact the parallel programmer manufacturer for more information. Refer to the user's manual included with your parallel programmer for instructions.
In parallel I/O mode, the user ROM areas shown in Figure 26.1 can be rewritten.

26.6.1 ROM Code Protect Function

The ROM code protect function prevents the flash memory from being read and rewritten (refer to **26.3.2 ROM Code Protect Function**).

26.7 Notes on Flash Memory

26.7.1 CPU Rewrite Mode

26.7.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

26.7.1.2 Interrupts

Tables 26.9 to 26.11 show CPU Rewrite Mode Interrupts.

Table 26.9 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Usable by allocating a vector in RAM.
		During auto-erasure (suspend disabled)	
		During auto-programming	
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0.
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written.
		During auto-erasure (suspend disabled or FMR22 = 0)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-programming	

FMR21, FMR22: Bits in FMR2 register

Table 26.10 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 1 (Note 1)	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

Table 26.11 CPU Rewrite Mode Interrupts (3)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 1 (Note 1)	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled or FMR22 = 0)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

26.7.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.

- The FMR01 bit or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20 bit, FMR22 bit, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 1 and writing 0.

- The FMR14 bit, FMR15 bit, FMR16 bit, or FMR17 bit in the FMR1 register

26.7.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

26.7.1.5 Programming

Do not write additions to the already programmed address.

26.7.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
If the FST7 bit in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

26.7.1.7 Programming and Erasure Voltage for Flash Memory

To program and erase program ROM in CPU rewrite mode, use Topr = 0 to 60°C as the operating ambient temperature. Do not program and erase program ROM under conditions other than Topr = 0 to 60°C.
To program and erase program ROM and data flash in standard serial I/O mode and parallel I/O mode, use VCC = 2.7 to 3.6 V as the supply voltage and Topr = 0 to 60°C as the operating ambient temperature. Do not program and erase program ROM and data flash when VCC is less than 2.7 V or under conditions other than Topr = 0 to 60°C.

26.7.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

26.7.1.9 Low-Current-Consumption Read Mode

In low-speed clock mode and low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:
- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
- The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
To reduce the power consumption, refer to **27. Reducing Power Consumption**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

26.7.2 Data Flash

Programs cannot be executed in the data flash.
Do not use the data flash as a program area.

27. Reducing Power Consumption

27.1 Overview

This chapter describes key points and processing methods for reducing power consumption.

27.2 Key Points and Processing Methods for Reducing Power Consumption

Key points for reducing power consumption are shown below. They should be referred to when designing a system or creating a program.

27.2.1 Voltage Detection Circuit

If voltage monitor 1 is not used, set the VCA26 bit in the VCA2 register to 0 (voltage detection 1 circuit disabled).
If power-on reset and voltage monitor 0 reset are not used, set the VCA25 bit in the VCA2 register to 0 (voltage detection 0 circuit disabled).

27.2.2 Ports

Even after the MCU enters wait mode or stop mode, the states of the I/O ports are retained. Current flows into the output ports in the active state, and shoot-through current flows into the input ports in the high-impedance state. Unnecessary ports should be set to input and fixed to a stable electric potential before the MCU enters wait mode or stop mode.

27.2.3 Clocks

Power consumption generally depends on the number of the operating clocks and their frequencies. The fewer the number of operating clocks or the lower their frequencies, the more power consumption decreases. Unnecessary clocks should be stopped accordingly.

Stopping low-speed on-chip oscillator oscillation:
Set the CM14 bit in CM1 register to 1 (low-speed on-chip oscillator off) and set the OCD2 bit in the OCD register to 0 (XIN clock selected).

27.2.4 Wait Mode, Stop Mode

Power consumption can be reduced in wait mode and stop mode. Refer to **9.7 Power Control** for details.

27.2.5 Stopping Peripheral Function Clocks

If the peripheral function f1, f2, f4, f8, and f32 clocks are not necessary in wait mode, set the CM02 bit in the CM0 register to 1 (peripheral function clock stops in wait mode). This will stop the f1, f2, f4, f8, and f32 clocks in wait mode.

27.2.6 Timers

If timer RA is not used, set the TCKCUT bit in the TRAMR register to 1 (count source cutoff).
If timer RB is not used, set the TCKCUT bit in the TRBMR register to 1 (count source cutoff).
If timer RC is not used, set the MSTTRC bit in the MSTCR register to 1 (standby).

27.2.7 Clock Synchronous Serial Interface

When the SSU or the I^2C bus is not used, set the MSTIIC bit in the MSTCR register to 1 (standby).

27.2.8 Reducing Internal Power Consumption

When the MCU enters wait mode using low-speed clock mode or low-speed on-chip oscillator mode, internal power consumption can be reduced by using the VCA20 bit in the VCA2 register. To enable reduced internal power consumption by the VCA20 bit, follow **9.7.2.2 Reducing Internal Power Consumption Using VCA20 Bit**.

27.2.9 Stopping Flash Memory

In low-speed on-chip oscillator mode and low-speed clock mode, power consumption can be further reduced by stopping the flash memory using the FMSTP bit in the FMR0 register.
Access to the flash memory is disabled by setting the FMSTP bit to 1 (flash memory stops). The FMSTP bit must be written to by a program transferred to RAM.
When the MCU enters stop mode or wait mode while CPU rewrite mode is disabled, the power for the flash memory is automatically turned off. It is turned back on again after the MCU exits stop mode or wait mode. This eliminates the need to set the FMR0 register.
Figure 27.1 shows the Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit.

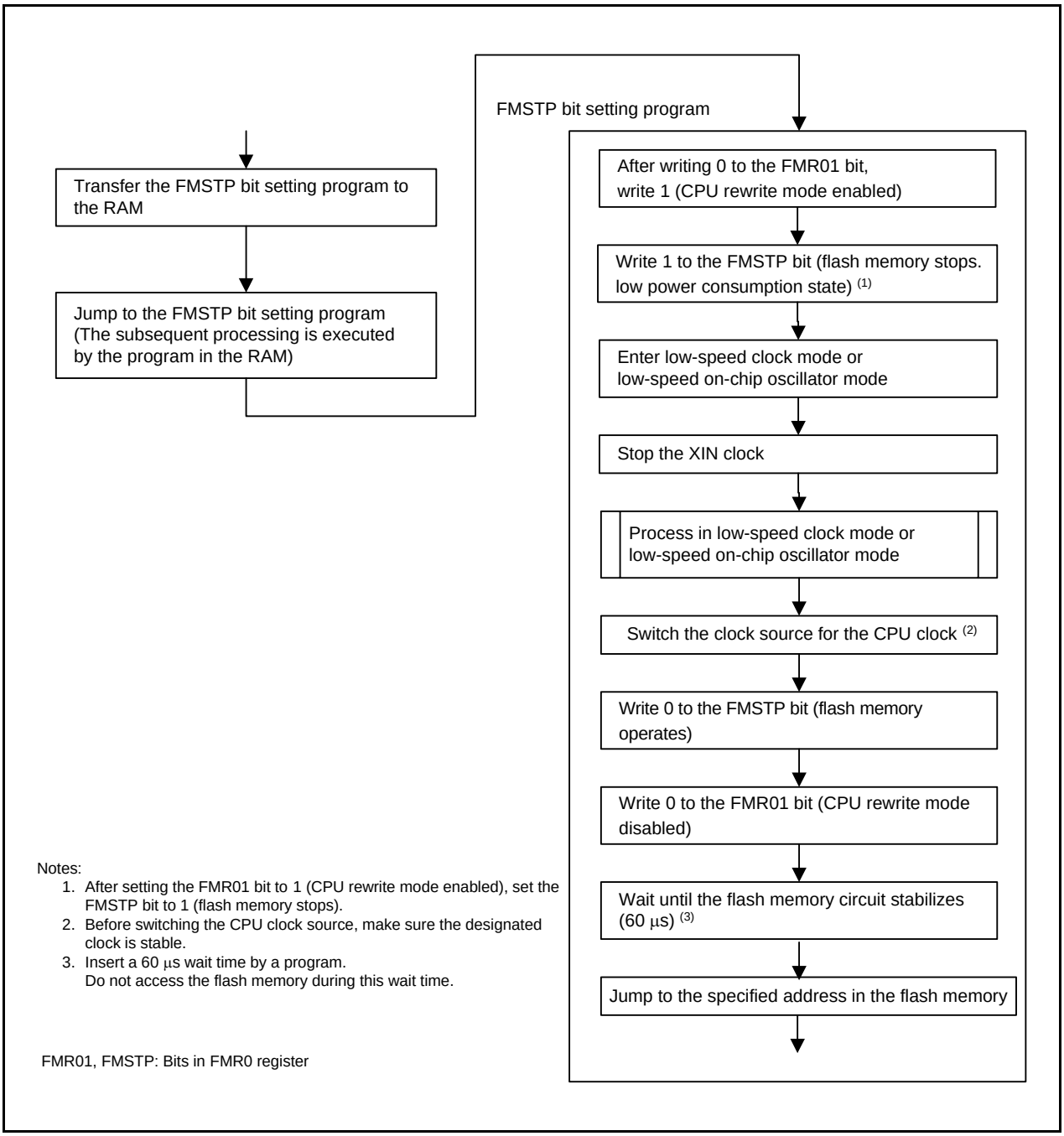


Figure 27.1 Handling Procedure Example for Reducing Power Consumption Using FMSTP Bit

27.2.10 Low-Current-Consumption Read Mode

In low-speed clock mode and low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).

Low-current-consumption read mode can be used when the CPU clock is set to either of the following:

- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
- The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.

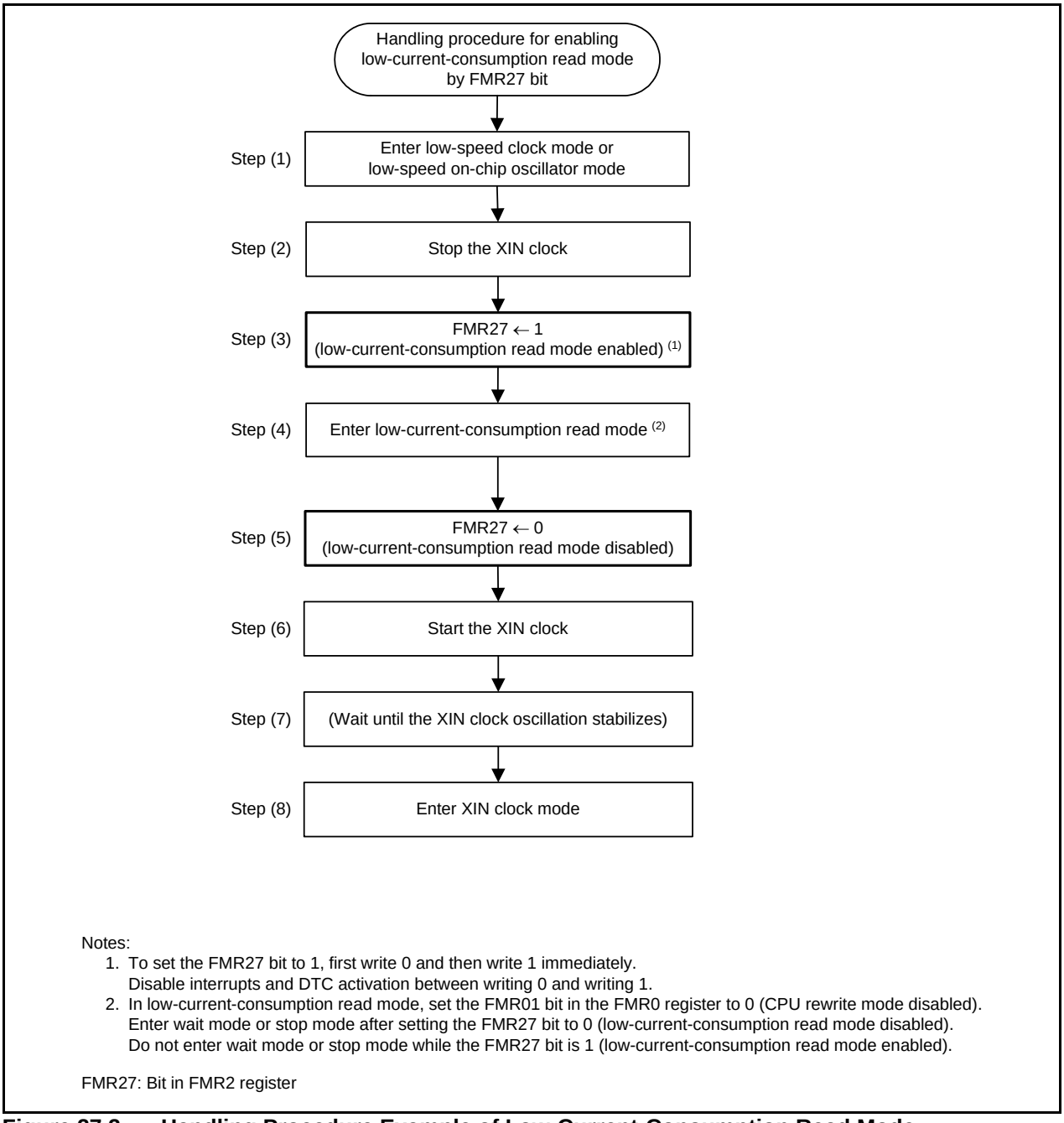
However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.

After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).

Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).

Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

Figure 27.2 shows the Handling Procedure Example of Low-Current-Consumption Read Mode.



Notes:
1. To set the FMR27 bit to 1, first write 0 and then write 1 immediately.
   Disable interrupts and DTC activation between writing 0 and writing 1.
2. In low-current-consumption read mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled).
   Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
   Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

FMR27: Bit in FMR2 register

Figure 27.2 Handling Procedure Example of Low-Current-Consumption Read Mode

28. Electrical Characteristics

Table 28.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
VCC	Digital supply voltage			–0.3 to 3.8	V
VCCRF	Analog supply voltage			–0.3 to 3.8	V
V_I	Input voltage	$\overline{\text{RESET}}$, MODE, P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5		–0.3 to V_{CC} + 0.3	V
VRFIO	RF I/O pins	RFIOP, RFION		–0.3 to 2.1	V
VTESTIO	Test ports	IFRXTP, IFRXTN		–0.3 to 2.1	V
VANAIN	1.5 V analog supply (input)	VREG1, VREG2, VREG3, VREG4		–0.3 to 2.1	V
VANAOUT	1.5 V analog supply (output)	VREGOUT1, VREGOUT2, VREGOUT3		–0.3 to 2.1	V
VXINOUT	Main clock I/O	XIN, XOUT		–0.3 to 2.1	V
P_d	Power dissipation		$-20°C \le T_{opr} \le 85°C$	300	mW
T_{opr}	Operating ambient temperature	(1) During MCU operation under the conditions other than (2) and (3) below.		–20 to 85	°C
		(2) During programming and erasing of the flash memory using a serial programmer or parallel programmer.		0 to 60	
		(3) During on-chip debugging with the E8a emulator connected		10 to 35	
T_{stg}	Storage temperature			–65 to 150	°C

Table 28.2 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
VCC	Digital supply voltage	(1) During MCU operation under the conditions other than (2) and (3) below.				1.8	3.3	3.6	V
		(2) During programming and erasing of the flash memory using a serial programmer or parallel programmer.				2.7	—	3.6	
		(3) During on-chip debugging with the E8a emulator connected				2.7	—	3.6	
VCCRF	Analog supply voltage					1.8	3.3	3.6	V
VSS/ VSS2/ VSSRF/ VSSRF1/ VSSRF2/ DIEGND	Supply voltage	VSS1, VSS2, VSSRF, VSSRF1, VSSRF2, DIEGND				—	0	—	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 Vcc	—	Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0.55 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	—	Vcc	V
				Input level selection: 0.5 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0.7 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
				Input level selection: 0.7 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0.85 Vcc	—	Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	—	Vcc	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	—	0.2 Vcc	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.2 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection: 0.5 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.3 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection: 0.7 Vcc	2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.45 Vcc	V
					1.8 V ≤ Vcc < 2.7 V	0	—	0.35 Vcc	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				—	—	–160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				—	—	–80	mA
$I_{OH(peak)}$	Peak output “H” current	Drive capacity Low				—	—	–10	mA
		Drive capacity High				—	—	–40	mA
$I_{OH(avg)}$	Average output “H” current	Drive capacity Low				—	—	–5	mA
		Drive capacity High				—	—	–20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				—	—	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				—	—	80	mA
$I_{OL(peak)}$	Peak output “L” current	Drive capacity Low				—	—	10	mA
		Drive capacity High				—	—	40	mA
$I_{OL(avg)}$	Average output “L” current	Drive capacity Low				—	—	5	mA
		Drive capacity High				—	—	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				1.8 V ≤ Vcc ≤ 3.6 V	—	16	—	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency				1.8 V ≤ Vcc ≤ 3.6 V	30	32.768	35	kHz
—	System clock frequency	f(XIN)=16 MHz			1.8 V ≤ Vcc ≤ 3.6 V	—	—	16	MHz
$f_{(BCLK)}$	CPU clock frequency	f(XIN)=16 MHz			2.7 V ≤ Vcc ≤ 3.6 V	—	—	16	MHz
					2.15 V ≤ Vcc < 2.7 V	—	—	8	
					1.8 V ≤ Vcc < 2.15 V	—	—	4	

Notes:
1. Vcc = 1.8 to 3.6 V and T_{opr} = –20°C to 85°C, unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

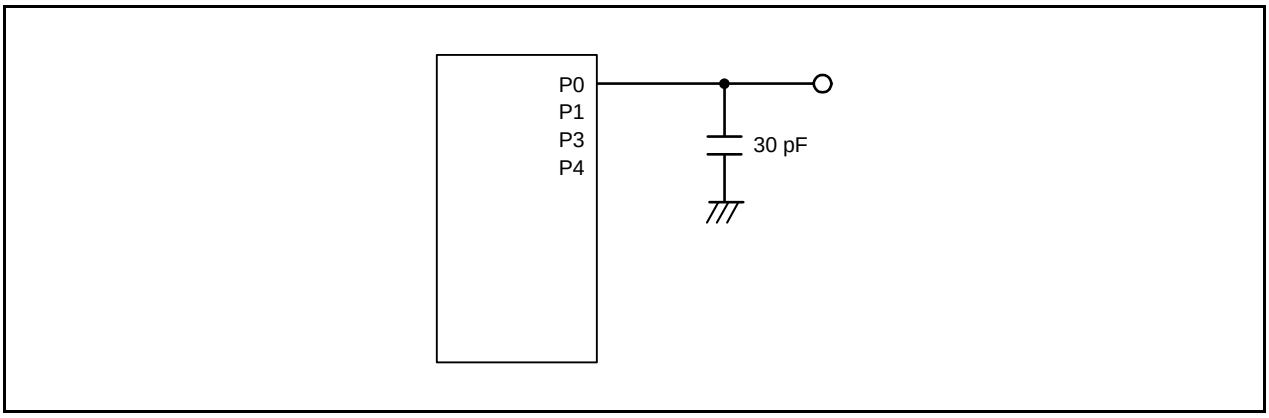


Figure 28.1 Ports P0, P1, P3 and P4 Timing Measurement Circuit

Table 28.3 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		1,000 (3)	—	—	times
—	Byte program time		—	80	500	µs
—	Block erase time		—	0.3	—	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage	CPU rewrite mode	1.8	—	3.6	V
		Standard serial I/O mode	2.7	—	3.6	
		Parallel I/O mode	2.7	—	3.6	
—	Read voltage		1.8	—	3.6	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time (7)	Ambient temperature = 55°C	20	—	—	year

Notes:
1. V_{CC} = 2.7 to 3.6 V and T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 28.4 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (2)		10,000 (3)	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	µs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	µs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage	CPU rewrite mode	1.8	—	3.6	V
		Standard serial I/O mode	2.7	—	3.6	
		Parallel I/O mode	2.7	—	3.6	
—	Read voltage		1.8	—	3.6	V
—	Program, erase temperature	CPU rewrite mode	−20	—	85	°C
		Standard serial I/O mode	0	—	60	
		Parallel I/O mode	0	—	60	
—	Data hold time (7)	Ambient temperature = 55°C	20	—	—	year

Notes:
1. V_{CC} = 1.8 to 3.6 V and T_{opr} = −20°C to 85°C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

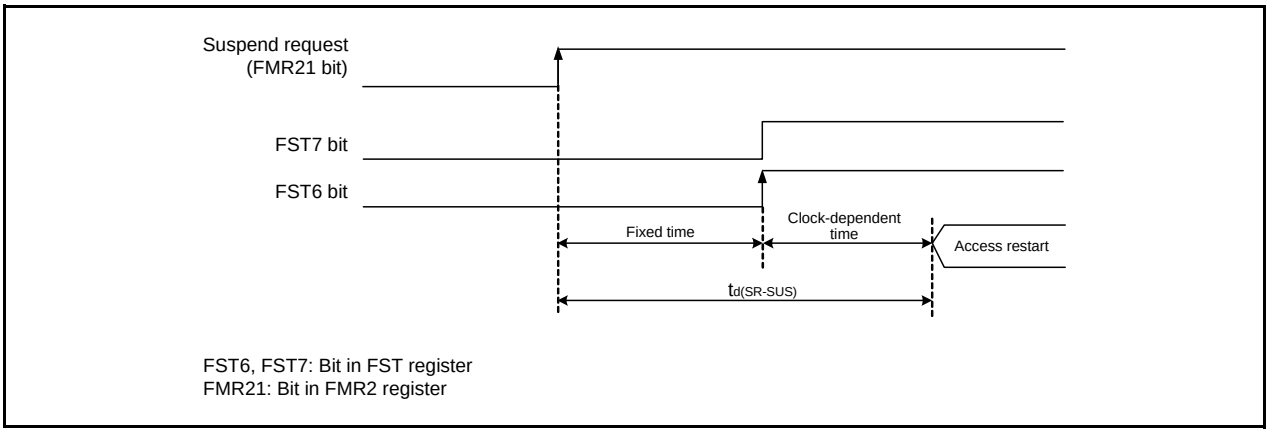


Figure 28.2 Time delay until Suspend

Table 28.5 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (4)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (4)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (4)		2.70	2.85	3.05	V
—	Voltage detection 0 circuit response time (3)	At the falling of V_{CC} from 3.6 V to (Vdet0_0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 3.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (2)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.
4. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.

Table 28.6 Voltage Detection 1 Circuit Electrical Characteristics

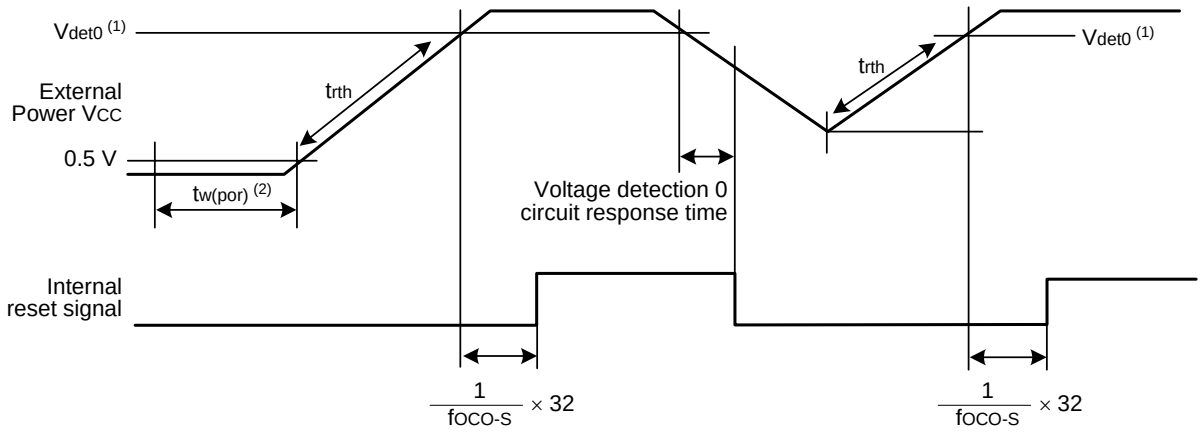
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_2 (2)	At the falling of V_{CC}	2.30	2.50	2.70	V
	Voltage detection level Vdet1_5 (2)	At the falling of V_{CC}	2.75	2.95	3.15	V
—	Hysteresis width at the rising of V_{CC} in voltage detection 1 circuit		—	0.07	—	V
—	Voltage detection 1 circuit response time (3)	At the falling of V_{CC} from 3.6 V to (Vdet1_0 – 0.1) V	—	60	150	µs
—	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 3.0 V	—	1.7	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (4)		—	—	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C.
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 28.7 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	—	50,000	mV/msec

Notes:
1. The measurement condition is T_{opr} = –20°C to 85°C, unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 28.3 Power-on Reset Circuit Electrical Characteristics

Table 28.8 System Clock Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		100	125	150	kHz
—	Oscillation stability time		—	30	100	µs

Note:
1. V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C, unless otherwise specified.

Table 28.9 Watchdog Timer Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-WDT	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time		—	30	100	µs

Note:
1. V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C, unless otherwise specified.

Table 28.10 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (2)		—	—	2,000	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 to 3.6 V and T_{opr} = 25°C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 28.11 Timing Requirements of Synchronous Serial Communication Unit (SSU) (1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	—	—	t_{CYC} (2)
t_{HI}	SSCK clock “H” width			0.4	—	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	—	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{FALL}	SSCK clock falling time	Master		—	—	1	t_{CYC} (2)
		Slave		—	—	1	µs
t_{SU}	SSO, SSI data input setup time			100	—	—	ns
t_H	SSO, SSI data input hold time			1	—	—	t_{CYC} (2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		1t_{CYC} + 50	—	—	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		1t_{CYC} + 50	—	—	ns
t_{OD}	SSO, SSI data output delay time			—	—	1.5	t_{CYC} (2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 3.6 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 3.6 V	—	—	1.5t_{CYC} + 100	ns
			1.8 V ≤ V_{CC} < 2.7 V	—	—	1.5t_{CYC} + 200	ns

Notes:
1. V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C, unless otherwise specified.
2. 1t_{CYC} = 1/f1(s)

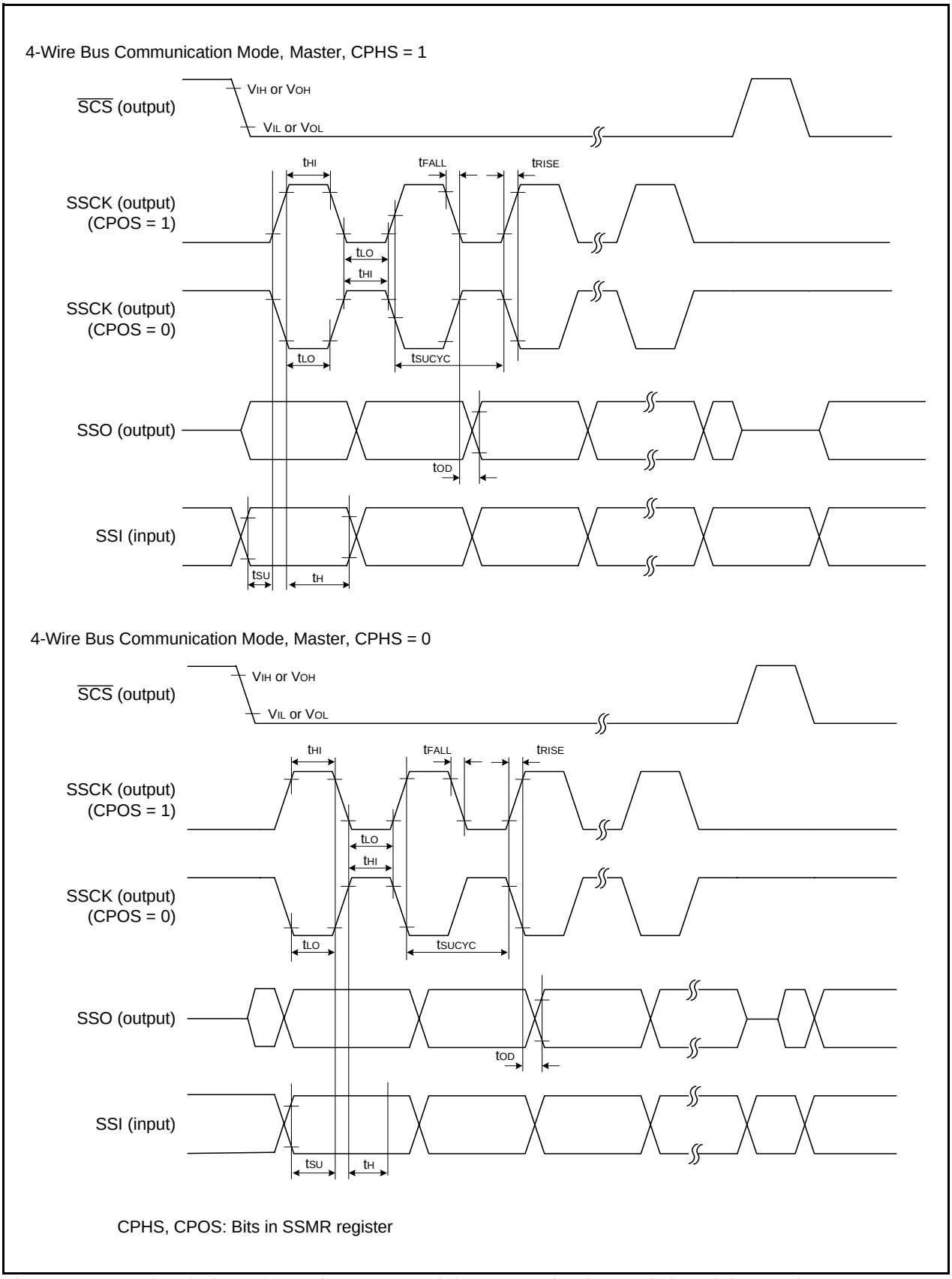


Figure 28.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

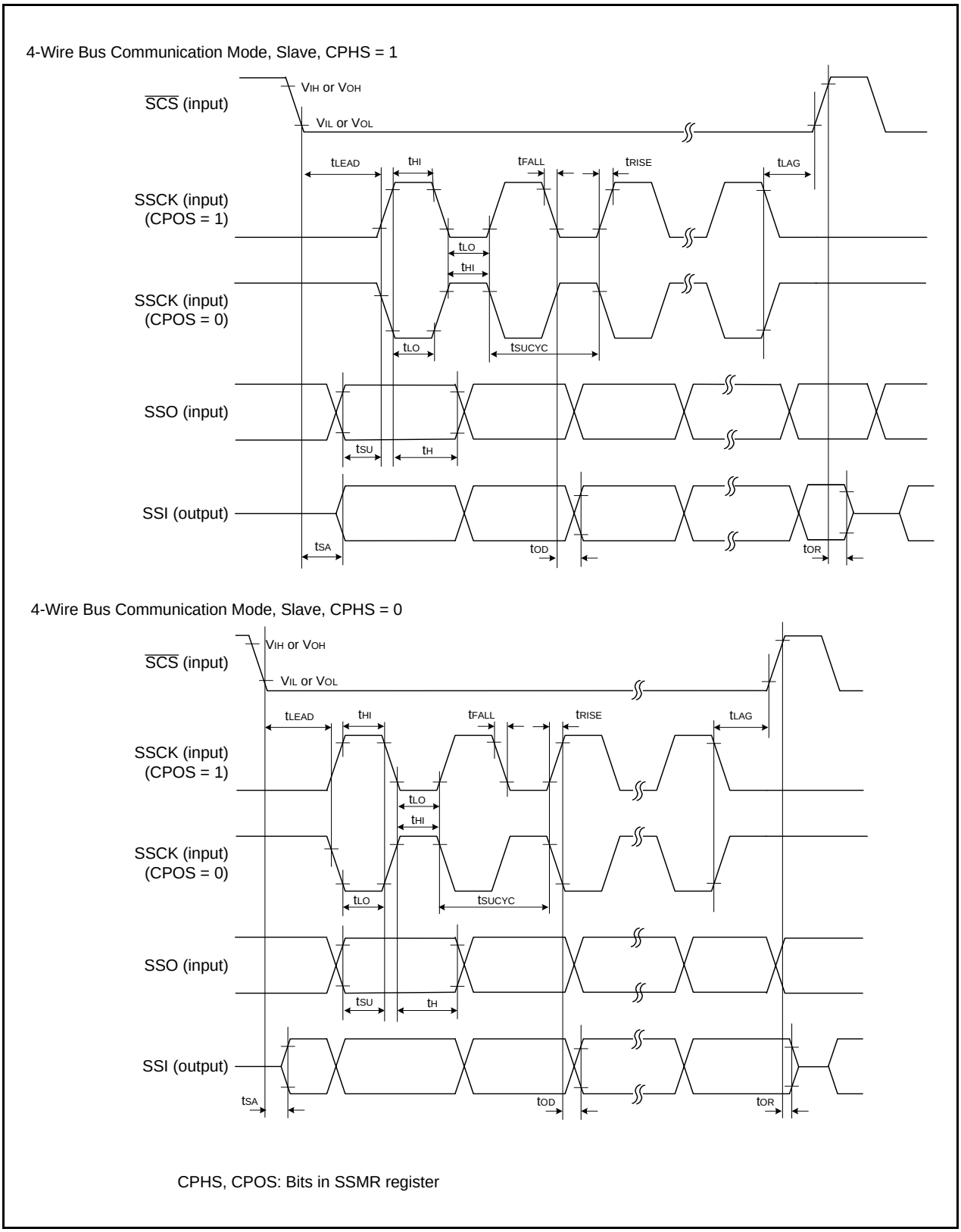


Figure 28.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

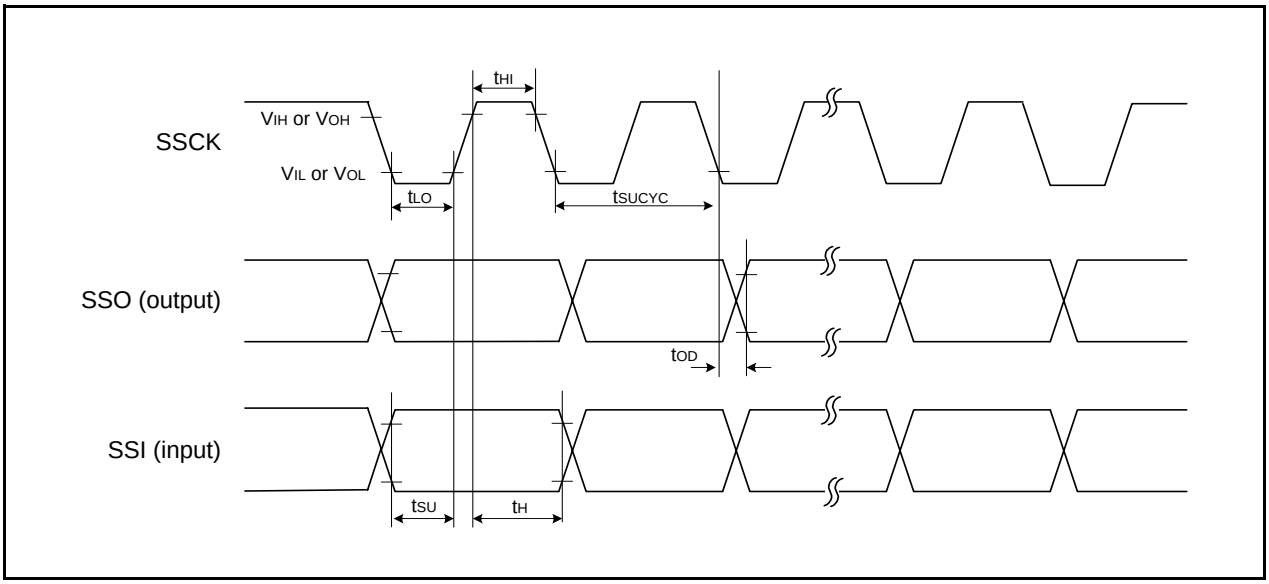
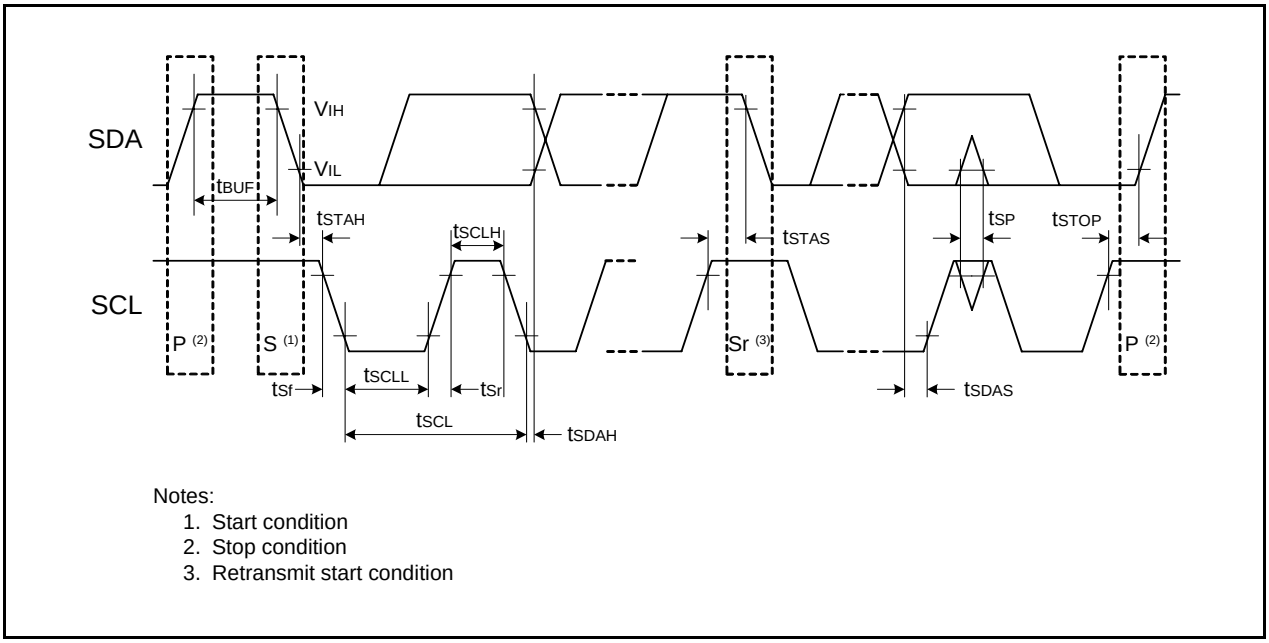


Figure 28.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 28.12 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$ (2)	—	—	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$ (2)	—	—	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$ (2)	—	—	ns
t_{sf}	SCL, SDA input fall time		—	—	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		—	—	$1t_{CYC}$ (2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ (2)	—	—	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ (2)	—	—	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ (2)	—	—	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 40$ (2)	—	—	ns
t_{SDAH}	Data input hold time		10	—	—	ns

Notes:
1. V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C, unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 28.7 I/O Timing of I²C bus Interface

Table 28.13 Electrical Characteristics (1) [1.8 V ≤ Vcc ≤ 3.6 V]
(Topr = –20°C to 85°C, unless otherwise specified)

Symbol	Parameter	Condition			Standard			Unit
					Min.	Typ.	Max.	
ICC	Power supply current Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode XIN clock oscillator on f(XIN) = 16 MHz XCIN clock oscillator on f(XCIN) = 32 kHz Low-speed on-chip oscillator on fOCO-S = 125 kHz System clock = XIN	CPU clock = Divide-by-4, (f(BCLK) = 4 MHz) 1.8 V ≤ VCC ≤ 3.6 V	RF = off	—	2.5	—	mA
				RF = idle	—	4.0	—	mA
				RF = Tx	—	18	—	mA
				RF = Rx (reception standby)	—	24	—	mA
				RF = Rx (reception in progress)	—	25	—	mA
			CPU clock = Divide-by-2, (f(BCLK) = 8 MHz) 2.15 V ≤ VCC ≤ 3.6 V	RF = off	—	3.5	—	mA
				RF = idle	—	5.0	—	mA
				RF = Tx	—	19	—	mA
				RF = Rx (reception standby)	—	25	—	mA
				RF = Rx (reception in progress)	—	26	—	mA
			CPU clock = No division (f(BCLK) = 16 MHz) 2.7 V ≤ VCC ≤ 3.6 V	RF = off	—	6.0	—	mA
				RF = idle	—	7.5	—	mA
				RF = Tx	—	21.5	—	mA
				RF = Rx (reception standby)	—	27.5	—	mA
				RF = Rx (reception in progress)	—	28.5	—	mA
		Low-speed on-chip oscillator mode XIN clock off, XCIN clock off, Low-speed on-chip oscillator on: fOCO-S = 125 kHz System clock = fOCO-S, CPU clock = Divide-by-8 FMR27 = 1, VCA20 = 0 (flash memory low-current-consumption read mode)		RF = off	—	80	—	µA
		Low-speed clock mode XIN clock off XCIN clock oscillator on f(XCIN) = 32 kHz Low-speed on-chip oscillator off System clock = XCIN CPU clock = No division	FMR27 = 1 VCA20 = 0 (flash memory low-current-consumption read mode)	RF = off	—	95	—	µA
			FMSTP = 1 VCA20 = 0 (Flash memory off, program operation on RAM)	RF = off	—	45	—	µA
		Wait mode XIN clock oscillator on: f(XIN) = 16 MHz XCIN clock oscillator on: f(XCIN) = 32 kHz Low-speed on-chip oscillator on: fOCO-S = 125 kHz System clock = XIN While a WAIT instruction is executed		RF = Rx (reception standby)	—	23	—	mA
		Wait mode XIN clock off XCIN clock oscillator on f(XCIN) = 32 kHz Low-speed on-chip oscillator off System clock = XCIN While a WAIT instruction is executed	Peripheral function clock on VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal power consumption enabled)	RF = off	—	6.0	—	µA
			Peripheral function clock off VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal power consumption enabled)	RF = off	—	4.5	—	µA
		Wait mode XIN clock off XCIN clock oscillator on Low-speed on-chip oscillator on fOCO-S = 125 kHz System clock = fOCO-S While a WAIT instruction is executed	Peripheral function clock on VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal low power consumption enabled)	RF = off	—	13.0	—	µA
			Peripheral function clock off VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal low power consumption enabled)	RF = off	—	7.5	—	µA
		Stop mode (Topr = 25°C) XIN clock off, XCIN clock off, Low-speed on-chip oscillator off, VCA26 = VCA25 = 0 (voltage detection circuit stopped)		RF = off	—	2.0	—	µA

Table 28.14 Electrical Characteristics (2) [2.7 V ≤ Vcc ≤ 3.6 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I_{OH} = –5 mA	V_{CC} – 0.5	—	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
V_{OL}	Output “L” voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, $\overline{KI4}$, $\overline{KI6}$, $\overline{KI7}$, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, RXD0, CLK0, SSI, SCL, SDA, SSO	VCC = 3.0 V		0.1	0.4	—	V
		$\overline{RESET}$	VCC = 3.0 V		0.1	0.5	—	V
I_{IH}	Input “H” current		V_I = 3 V, V_{CC} = 3.0 V		—	—	4.0	µA
I_{IL}	Input “L” current		V_I = 0 V, V_{CC} = 3.0 V		—	—	–4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 3.0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	3.6	V

Note:
1. 2.7 V ≤ V_{CC} ≤ 3.6 V, T_{opr} = –20°C to 85°C, and f(XIN) =16 MHz, unless otherwise specified.

Timing requirements (VCC = 3 V, Topr = –20°C to 85°C, unless otherwise specified)

Table 28.15 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	—	ns

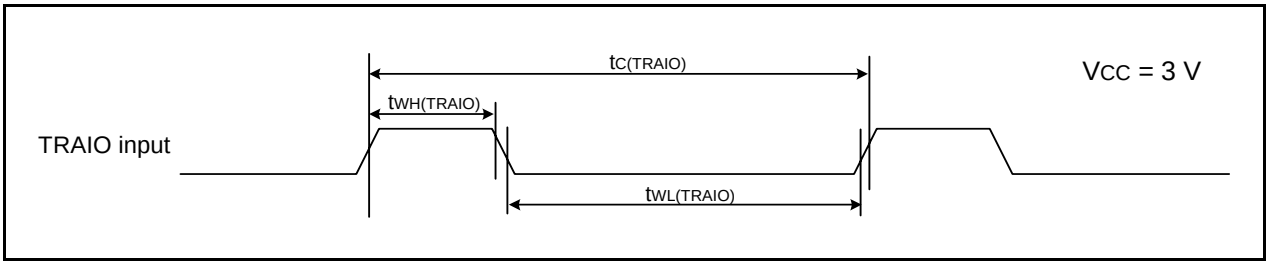


Figure 28.8 TRAIO Input Timing Diagram when VCC = 3 V

Table 28.16 Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	When an external clock is selected	300	—	ns
$t_{W(CKH)}$	CLK0 input “H” width		150	—	ns
$t_{W(CKL)}$	CLK0 Input “L” width		150	—	ns
$t_{d(C-Q)}$	TXD0 output delay time		—	120	ns
$t_{h(C-Q)}$	TXD0 hold time		0	—	ns
$t_{su(D-C)}$	RXD0 input setup time		30	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns
$t_{h(C-Q)}$	TXD0 output delay time	When an internal clock is selected	—	30	ns
$t_{su(D-C)}$	RXD0 input setup time		120	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns

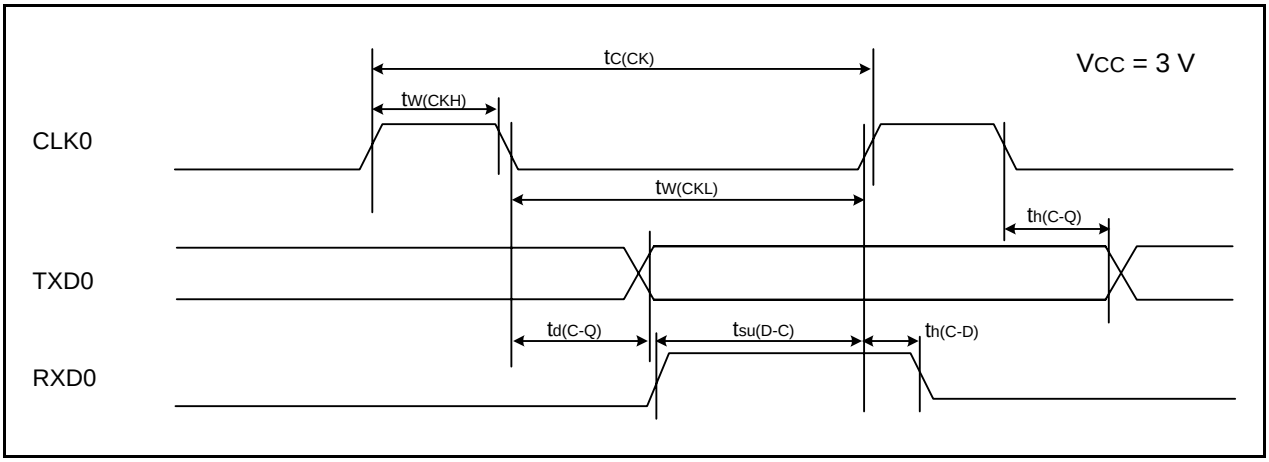


Figure 28.9 Serial Interface Timing Diagram when VCC = 3 V

Table 28.17 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 7)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	380 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	380 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

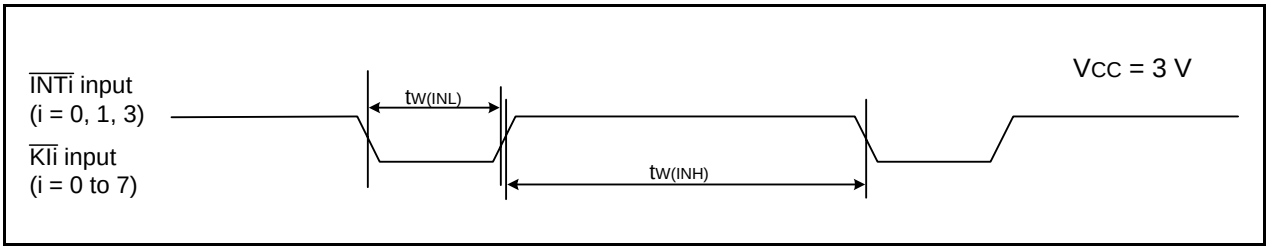


Figure 28.10 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 3 V

Table 28.18 Electrical Characteristics (3) [1.8 V ≤ Vcc < 2.7 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I_{OH} = –2 mA	V_{CC} – 0.5	—	V_{CC}	V
			Drive capacity Low	I_{OH} = –1 mA	V_{CC} – 0.5	—	V_{CC}	V
V_{OL}	Output “L” voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I_{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I_{OL} = 1 mA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, KI3, KI4, KI6, KI7, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, RXD0, CLK0, SSI, SCL, SDA, SSO	VCC = 2.15 V		0.05	0.20	—	V
		$\overline{RESET}$	VCC = 2.15 V		0.05	0.20	—	V
I_{IH}	Input “H” current		V_I = 2.15 V, V_{CC} = 2.15 V		—	—	4.0	µA
I_{IL}	Input “L” current		V_I = 0 V, V_{CC} = 2.15 V		—	—	–4.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V, V_{CC} = 2.15 V		70	140	300	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	3.6	V

Note:
1. 1.8 V ≤ V_{CC} < 2.7 V, T_{opr} = –20°C to 85°C, and f(XIN) = 16 MHz, unless otherwise specified.

Timing requirements (VCC = 2.15 V, Topr = –20°C to 85°C, unless otherwise specified)

Table 28.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	—	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	200	—	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	200	—	ns

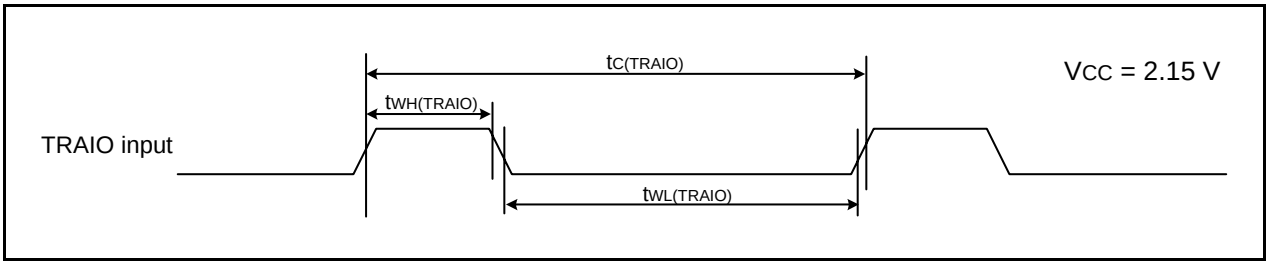


Figure 28.11 TRAIO Input Timing Diagram when VCC = 2.15 V

Table 28.20 Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	When an external clock is selected	800	—	ns
$t_{W(CKH)}$	CLK0 input “H” width		400	—	ns
$t_{W(CKL)}$	CLK0 input “L” width		400	—	ns
$t_{d(C-Q)}$	TXD0 output delay time		—	200	ns
$t_{h(C-Q)}$	TXD0 hold time		0	—	ns
$t_{su(D-C)}$	RXD0 input setup time		150	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns
$t_{h(C-Q)}$	TXD0 output delay time	When an internal clock is selected	—	200	ns
$t_{su(D-C)}$	RXD0 input setup time		150	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns

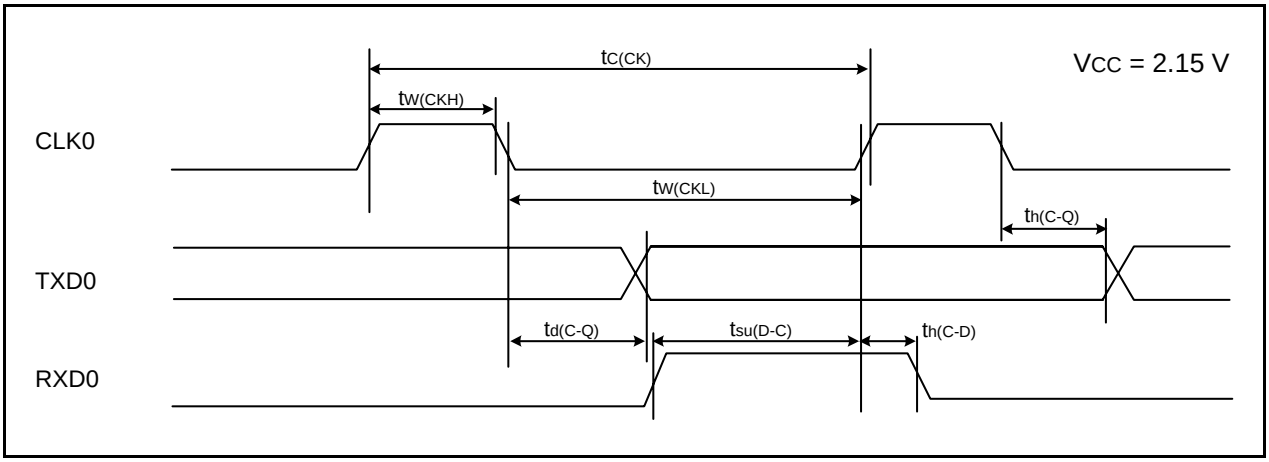


Figure 28.12 Serial Interface Timing Diagram when VCC = 2.15 V

Table 28.21 External Interrupt $\overline{INTi}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 7)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	1000 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	1000 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

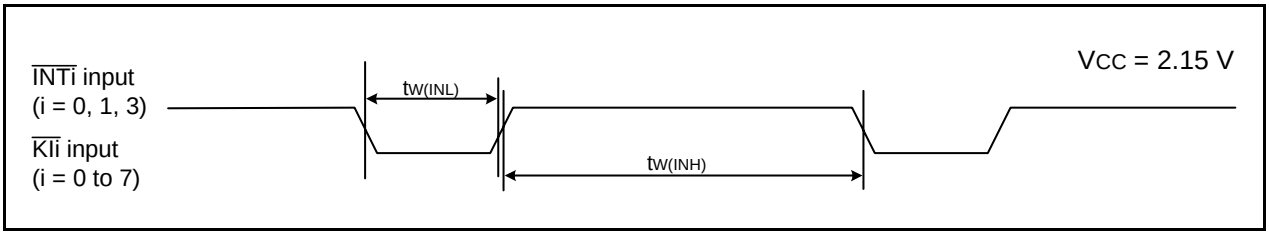


Figure 28.13 Input Timing Diagram for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when V_{CC} = 2.15 V

Table 28.22 Transceiver Transmission Characteristics (VCC = VCCRF = 3.3 V, Topr = 25°C, unless otherwise specified)

Parameter		Condition	Standard			IEEE802.15.4 standard	Unit
			Min.	Typ.	Max.		
Internal voltage			—	1.45	—	—	V
Nominal output power			–3	0	3	–3 or more	dBm
Transmit bit rate			—	250	—	250	kbps
Transmit chip rate			—	2000	—	2000	kchips/s
Programmable output power range		32 steps	—	32	—	32 steps	dB
Harmonics	2nd harmonics	External notch filter	—	—	–47.2	–41.2 or less	dBm
	3rd harmonics		—	—	–47.2	—	
Spurious emission	30 – 88 MHz	Maximum output power, Renesas evaluation board	—	—	–55.2	FCC	dBm
	88 – 216 MHz		—	—	–51.7	FCC	
	216 – 960 MHz		—	—	–49.2	FCC	
	960 – 1000 MHz		—	—	–41.2	FCC	
	1 – 12.75 GHz		—	—	–41.2	FCC (1)	
	1.8 – 1.9 GHz		—	—	–47	ETSI	
	5.15 – 5.3 GHz		—	—	–47	ETSI	
Error vector magnitude EVM		1000 chips	—	—	35	35 or less	%
Power spectral density	Absolute limit	|f-fc| > 3.5 MHz	—	—	–30	–30 or less	dBm
	Relative limit	|f-fc| > 3.5 MHz	—	—	–20	–20 or less	dB
Frequency tolerance		Including crystal ±20 ppm	–40	—	40	Within ±40	ppm

Note:
1. Notes on FFC certification testing
When using 26 CH (2480 MHz), adjust the transmit power to meet the FCC requirements and standards at 2483.5 MHz.

Table 28.23 Transceiver Reception Characteristics (VCC = VCCRF = 3.3 V, Topr = 25°C, unless otherwise specified)

Parameter		Condition	Standard			IEEE802.15.4 standard	Unit
			Min.	Typ.	Max.		
Internal voltage			—	1.45	—	—	V
RF input frequency			2405	—	2480	Min. 2405/ Max. 2480	MHz
Receiver sensitivity		PER = 1% PSDU Length = 20 octets Interframe spacing 12 symbols (IEEE802.15.4 minimum spacing)	—	–95	–85	–85 or less	dBm
Maximum input level		PER = 1%	0	—	—	–20 or more	dBm
Adjacent channel rejection	+5 MHz	PER = 1% Prf = –82 dBm	0	—	—	0 or more	dB
	–5 MHz		0	—	—		
Alternate channel rejection	+10 MHz	PER = 1% Prf= –82 dBm	30	—	—	30 or more	dB
	–10 MHz		30	—	—		
Rejection	> +15 MHz	PER = 1% Prf= –82 dBm	30	—	—	—	dB
	< –15 MHz		30	—	—		
Spurious emission	30 – 1000 MHz	Renesas evaluation board	—	—	–57	ETSI EN300/328	dBm
	1 – 12.75 GHz		—	—	–47		
Symbol error tolerance			–80	—	80	±40 or more (±80 for the total of transmission and reception)	ppm
RSSI range		Prf (min) = –75 dBm	40	75	—	40 or more	dB
RSSI accuracy		Prf = –75 to –35 dBm	–6	—	6	Within ±6	dB

29. Usage Notes

29.1 Notes on Clock Generation Circuit

29.1.1 Stop Mode

To enter stop mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and then the CM10 bit in the CM1 register to 1 (stop mode). An instruction queue pre-reads 4 bytes from the instruction which sets the CM10 bit to 1 (stop mode) and the program stops.
Insert at least four NOP instructions following the JMP.B instruction after the instruction which sets the CM10 bit to 1.

- Program example to enter stop mode

```
        BCLR    1, FMR0     ; CPU rewrite mode disabled
        BCLR    7, FMR2     ; Low-current-consumption read mode disabled
        BSET    0, PRCR     ; Writing to CM1 register enabled
        FSET    I           ; Interrupt enabled
        BSET    0, CM1      ; Stop mode
        JMP.B   LABEL_001
LABEL_001:
        NOP
        NOP
        NOP
        NOP
```

29.1.2 Wait Mode

When entering wait mode, set the FMR01 bit in the FMR0 register to 0 (CPU rewrite mode disabled) and the FMR27 bit to 0 (low-current-consumption read mode disabled) before entering the mode. Do not enter wait mode while the FMR01 bit is 1 (CPU rewrite mode enabled) or the FMR27 bit is 1 (low-current-consumption read mode enabled).
To enter wait mode by setting the CM30 bit to 1, set the I flag to 0 (maskable interrupt disabled).
To enter wait mode using the WAIT instruction, set the I flag to 1 (maskable interrupt enabled). An instruction queue pre-reads 4 bytes from the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction, and then the program stops. Insert at least four NOP instructions after the instruction to set the CM30 bit to 1 (MCU enters wait mode) or the WAIT instruction.

- Program example to execute the WAIT instruction

```
BCLR    1, FMR0     ; CPU rewrite mode disabled
BCLR    7, FMR2     ; Low-current-consumption read mode disabled
FSET    I           ; Interrupt enabled
WAIT                ; Wait mode
NOP
NOP
NOP
NOP
```

- Program example to execute the instruction to set the CM30 bit to 1

```
BCLR    1, FMR0     ; CPU rewrite mode disabled
BCLR    7, FMR2     ; Low-current-consumption read mode disabled
BSET    0, PRCR     ; Writing to CM3 register enabled
FCLR    I           ; Interrupt disabled
BSET    0, CM3      ; Wait mode
NOP
NOP
NOP
NOP
BCLR    0, PRCR     ; Writing to CM3 register disabled
FSET    I           ; Interrupt enabled
```

29.1.3 Reducing Internal Power Using VCA20 Bit

Set the VCA20 bit to 1 in low-speed clock mode or low-speed on-chip oscillator mode before entering wait mode.
To enter wait mode by setting the CM30 bit in the CM3 register to 1 (MCU enters wait mode), follow the procedure shown in Figure 9.5 to set the procedure for reducing internal power consumption using the VCA20 bit.
To enter wait mode by executing WAIT instruction, follow the procedure shown in Figure 9.6 to set the procedure for reducing internal power consumption using the VCA20 bit.

29.1.4 Oscillator Stop Detection Function

The oscillation stop detection function cannot be used when the XIN clock frequency is below 2 MHz. In this case, set bits OCD1 to OCD0 in the OCD register to 00b. In addition, the OCD3 bit cannot be used to confirm whether the XIN clock oscillation is stable.

29.1.5 Oscillation Circuit Constants

Consult the oscillator manufacturer to determine the optimal oscillation circuit constants for the user system.

29.2 Notes on Interrupts

29.2.1 Reading Address 00000h

Do not read address 00000h by a program. When a maskable interrupt request is acknowledged, the CPU reads interrupt information (interrupt number and interrupt request level) from 00000h in the interrupt sequence. At this time, the IR bit for the acknowledged interrupt is set to 0.
If address 00000h is read by a program, the IR bit for the interrupt which has the highest priority among the enabled interrupts is set to 0. This may cause the interrupt to be canceled, or an unexpected interrupt to be generated.

29.2.2 SP Setting

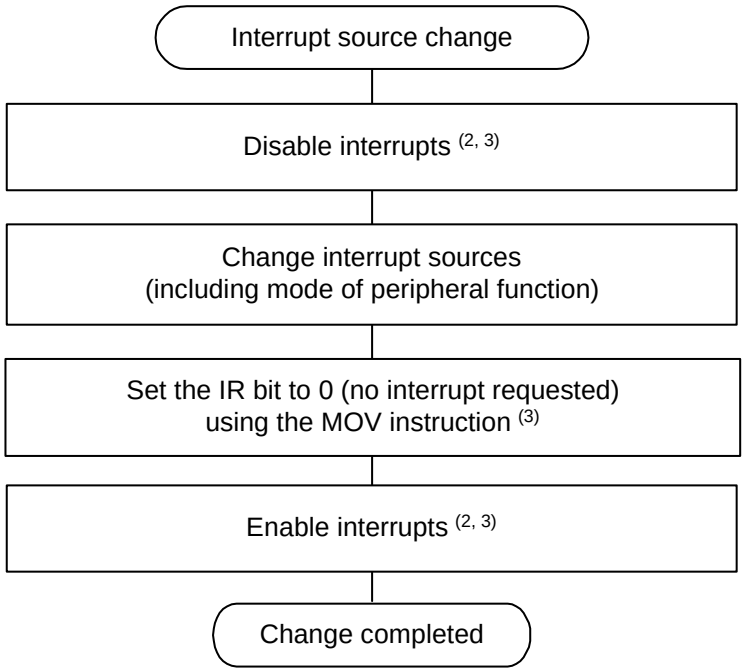
Set a value in the SP before an interrupt is acknowledged. The SP is set to 0000h after a reset. If an interrupt is acknowledged before setting a value in the SP, the program may run out of control.

29.2.3 External Interrupt and Key Input Interrupt

Either the “L” level width or “H” level width shown in the Electrical Characteristics is required for the signal input to pins $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$ and pins $\overline{\text{KI0}}$ to $\overline{\text{KI7}}$, regardless of the CPU clock.
For details, refer to **Table 28.17** (VCC = 3 V), **Table 28.21** (VCC = 2.15 V) **External Interrupt $\overline{\text{INTi}}$ (i = 0, 1, 3) Input, Key Input Interrupt $\overline{\text{KIi}}$ (i = 0 to 7)**.

29.2.4 Changing Interrupt Sources

The IR bit in the interrupt control register may be set to 1 (interrupt requested) when the interrupt source changes. To use an interrupt, set the IR bit to 0 (no interrupt requested) after changing interrupt sources.
Changing interrupt sources as referred to here includes all factors that change the source, polarity, or timing of the interrupt assigned to a software interrupt number. Therefore, if a mode change of a peripheral function involves the source, polarity, or timing of an interrupt, set the IR bit to 0 (no interrupt requested) after making these changes. Refer to the descriptions of the individual peripheral functions for related interrupts.
Figure 29.1 shows a Procedure Example for Changing Interrupt Sources.



IR bit: The interrupt control register bit for the interrupt whose source is to be changed

Notes:
1. The above settings must be executed individually. Do not execute two or more settings simultaneously (using one instruction).
2. To prevent interrupt requests from being generated, disable the peripheral function before changing the interrupt source. In this case, use the I flag if all maskable interrupts can be disabled.
   If all maskable interrupts cannot be disabled, use bits ILVL0 to ILVL2 for the interrupt whose source is to be changed.
3. To change the interrupt source to the input with the digital filter used, wait for three or more cycles of the sampling clock of the digital filter before setting the IR bit to 0 (no interrupt requested). Refer to **11.9.5 Rewriting Interrupt Control Register** for the instructions to use and related notes.

Figure 29.1 Procedure Example for Changing Interrupt Sources

29.2.5 Rewriting Interrupt Control Register

(a) The contents of the interrupt control register can be rewritten only while no interrupt requests corresponding to that register are generated. If an interrupt request may be generated, disable the interrupt before rewriting the contents of the interrupt control register.

(b) When rewriting the contents of the interrupt control register after disabling the interrupt, be careful to choose appropriate instructions.
Changing any bit other than the IR bit
If an interrupt request corresponding to the register is generated while executing the instruction, the IR bit may not be set to 1 (interrupt requested), and the interrupt may be ignored. If this causes a problem, use one of the following instructions to rewrite the contents of the register: AND, OR, BCLR, and BSET.

Changing the IR bit
Depending on the instruction used, the IR bit may not be set to 0 (no interrupt requested). Use the MOV instruction to set the IR bit to 0.

(c) When using the I flag to disable an interrupt, set the I flag as shown in the sample programs below. Refer to (b) regarding rewriting the contents of interrupt control registers using the sample programs.

Examples 1 to 3 show how to prevent the I flag from being set to 1 (interrupts enabled) before the contents of the interrupt control register are rewritten for the effects of the internal bus and the instruction queue buffer.

Example 1: Use the NOP instructions to pause program until the interrupt control register is rewritten

```
INT_SWITCH1:
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    NOP                     ;
    NOP
    FSET    I               ; Enable interrupts
```

Example 2: Use a dummy read to delay the FSET instruction

```
INT_SWITCH2:
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    MOV.W   MEM, R0         ; Dummy read
    FSET    I               ; Enable interrupts
```

Example 3: Use the POPC instruction to change the I flag

```
INT_SWITCH3:
    PUSHC   FLG
    FCLR    I               ; Disable interrupts
    AND.B   #00H, 0056H     ; Set the TRAIC register to 00h
    POPC    FLG             ; Enable interrupts
```

29.3 Notes on ID Code Areas

29.3.1 Setting Example of ID Code Areas

The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set 55h in all of the ID code areas

```
.org 00FFDCH
.lword dummy | (55000000h)   ; UND
.lword dummy | (55000000h)   ; INTO
.lword dummy                 ; BREAK
.lword dummy | (55000000h)   ; ADDRESS MATCH
.lword dummy | (55000000h)   ; SET SINGLE STEP
.lword dummy | (55000000h)   ; WDT
.lword dummy | (55000000h)   ; ADDRESS BREAK
.lword dummy | (55000000h)   ; RESERVE
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

29.4 Notes on Option Function Select Area

29.4.1 Setting Example of Option Function Select Area

The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. The following shows a setting example.

- To set FFh in the OFS register

```
.org 00FFFCH
.lword reset | (0FF000000h)    ; RESET
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

- To set FFh in the OFS2 register

```
.org 00FFDBH
.byte 0FFh
```

(Programming formats vary depending on the compiler. Check the compiler manual.)

29.5 Notes on DTC

29.5.1 DTC activation source

- Do not generate any DTC activation sources before entering wait mode or during wait mode.
- Do not generate any DTC activation sources before entering stop mode or during stop mode.

29.5.2 DTCENi (i = 0 to 3, 5, 6) Registers

- Modify bits DTCENi0 to DTCENi7 only while an interrupt request corresponding to the bit is not generated.
- When the interrupt source flag in the status register for the peripheral function is 1, do not modify the corresponding activation source bit among bits DTCENi0 to DTCENi7.
- Do not access the DTCENi registers using DTC transfers.
- The bits with no interrupt sources assigned are reserved. Set these bits to 0.

29.5.3 Peripheral Modules

- Do not set the status register bit for the peripheral function to 0 using a DTC transfer.
- When the DTC activation source is SSU/I^{2}C bus receive data full, read the SSRDR register/the ICDRR register using a DTC transfer.
  The RDRF bit in the SSSR register/the ICSR register is set to 0 (no data in SSRDR/ICDRR register) by reading the SSRDR register/the ICDRR register.
  However, the RDRF bit is not set to 0 by reading the SSRDR register/the ICDRR register when the DTC data transfer setting is either of the following:
  -Transfer causing the DTCCTj (j = 0 to 23) register value to change from 1 to 0 in normal mode
  -Transfer causing the DTCCRj register value to change from 1 to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode.
- When the DTC activation source is SSU/I^{2}C bus transmit data empty, write to the SSTDR register/the ICDRT register using a DTC transfer. The TDRE bit in the SSSR register/the ICSR register is set to 0 (data is not transferred from registers SSTDR/ICDRT to SSTRSR/ICDRS) by writing to the SSTDR register/the ICDRT register.

29.5.4 Interrupt Requests

No interrupt is generated for the CPU during DTC operation in any of the following cases:
- When the DTC activation source is SSU/I^{2}C transmit data empty or flash ready status
- When performing the data transfer causing the DTCCTj (j = 0 to 23) register value to change to 0 in normal mode
- When performing the data transfer causing the DTCCRj register value to change to 0 while the RPTINT bit in the DTCCRj register is 1 (interrupt generation enabled) in repeat mode

29.5.5 DTC Chain Transfers

When performing chain transfers using several control data, the number of transfers set to the first control data is enabled and the number of transfers proceeded after the first control data is disabled.
Examples:
- When DTCCT0 = 5 and DTCCT1 = 10, chain transfers are performed as DTCCT0 = DTCCT1 = 5.
- When DTCCT0 = 10 and DTCCT1 = 5, chain transfers are performed as DTCCT0 = DTCCT1 = 10.
- When DTCCT0 = 10, DTCCT1 = 5, and DTCCT2 = 2, chain transfers are performed as DTCCT0 = DTCCT1 = DTCCT2 = 10.

29.6 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse width measurement mode and pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse width measurement mode and pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).

  The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RA counting is stopped when the TCSTF bit is set to 0.

  During this time, do not access registers associated with timer RA (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

- When the TRAPRE register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the count source clock for each write interval.
- When the TRA register is continuously written during count operation (TCSTF bit is set to 1), allow three or more cycles of the prescaler underflow for each write interval.
- Do not set 00h to the TRA register in pulse width measurement mode and pulse period measurement mode.

29.7 Notes on Timer RB

- Timer RB stops counting after a reset. Set the values in the timer RB and timer RB prescalers before the count starts.
- Even if the prescaler and timer RB is read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In programmable one-shot generation mode and programmable wait one-shot generation mode, when setting the TSTART bit in the TRBCR register to 0 (stops counting) or setting the TOSSP bit in the TRBOCR register to 1 (stops one-shot), the timer reloads the value of reload register and stops. Therefore, in programmable one-shot generation mode and programmable wait one-shot generation mode, read the timer count value before the timer stops.
- The TCSTF bit remains 0 (count stops) for 1 to 2 cycles of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit. Timer RB starts counting at the first valid edge of the count source after the TCSTF bit is set to 1 (during count).
  The TCSTF bit remains 1 for 1 to 2 cycles of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress. Timer RB counting is stopped when the TCSTF bit is set to 0.
  During this time, do not access registers associated with timer RB (1) other than the TCSTF bit.

  Note:
  1. Registers associated with timer RB: TRBCR, TRBOCR, TRBIOC, TRBMR, TRBPRE, TRBSC, and TRBPR.

- If the TSTOP bit in the TRBCR register is set to 1 during timer operation, timer RB stops immediately.
- If 1 is written to the TOSST or TOSSP bit in the TRBOCR register, the value of the TOSSTF bit changes after one or two cycles of the count source have elapsed. If the TOSSP bit is written to 1 during the period between when the TOSST bit is written to 1 and when the TOSSTF bit is set to 1, the TOSSTF bit may be set to either 0 or 1 depending on the content state. Likewise, if the TOSST bit is written to 1 during the period between when the TOSSP bit is written to 1 and when the TOSSTF bit is set to 0, the TOSSTF bit may be set to either 0 or 1.
- To use the underflow signal of timer RA as the count source for timer RB, set timer RA in timer mode, pulse output mode, or event count mode.

29.7.1 Timer Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

29.7.2 Programmable Waveform Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

29.7.3 Programmable One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

29.7.4 Programmable Wait One-shot Generation Mode

To write to registers TRBPRE and TRBPR during count operation (TCSTF bit in the TRBCR register is set to 1), note the following points:

- When the TRBPRE register is written continuously, allow three or more cycles of the count source for each write interval.
- When the TRBPR register is written continuously, allow three or more cycles of the prescaler underflow for each write interval.

29.8 Notes on Timer RC

29.8.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (clear TRC register at compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC    ; Write
                    JMP.B   L1             ; JMP.B instruction
                L1: MOV.W   TRC, DATA      ; Read
```

29.8.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR    ; Write
                    JMP.B   L1             ; JMP.B instruction
                L1: MOV.B   TRCSR, DATA    ; Read
```

29.8.3 Count Source Switching

- Stop the count before switching the count source.

Switching procedure

(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

29.8.4 Input Capture Function

- Set the pulse width of the input capture signal as follows:
  [When the digital filter is not used]
  Three or more cycles of the timer RC operation clock (refer to **Table 19.1 Timer RC Operation Clock**)
  [When the digital filter is used]
  Five cycles of the digital filter sampling clock + three cycles of the timer RC operating clock, minimum (refer to **Figure 19.5 Digital Filter Block Diagram**)
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).
- When the input capture function is used, if an edge selected by bits IOj0 and IOj1 (j = A, B, C, or D) in the TRCIOR0 or TRCIOR1 register is input to the TRCIOj pin, the IMFj bit in the TRCSR register is set to 1 even when the TSTART bit in the TRCMR register is 0 (count stops).

29.8.5 TRCMR Register in PWM2 Mode

When the CSEL bit in the TRCCR2 register is set to 1 (count stops at compare match with the TRCGRA register), do not set the TRCMR register at compare match timing of registers TRC and TRCGRA.

29.9 Notes on Timer RE

29.9.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit, which indicates count start or stop. Bits TSTART and TCSTF are in the TRECR1 register.
Timer RE starts counting and the TCSTF bit is set to 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to 2 cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE (1) other than the TCSTF bit.
Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to 2 cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

Note:
1. Registers associated with timer RE: TREMIN, TREHR, TREWK, TRECR1, TRECR2, and TRECSR.

29.9.2 Register Setting

Write to the following registers or bits when timer RE is stopped.
- Registers TRESEC, TREMIN, TREHR, TREWK, and TRECR2
- Bits H12_H24, PM, and INT in TRECR1 register
- Bits RCS0 to RCS3 in TRECSR register

Timer RE is stopped when bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer RE stopped).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TRECR2 register.
Figure 29.2 shows a Setting Example in Real-Time Clock Mode.

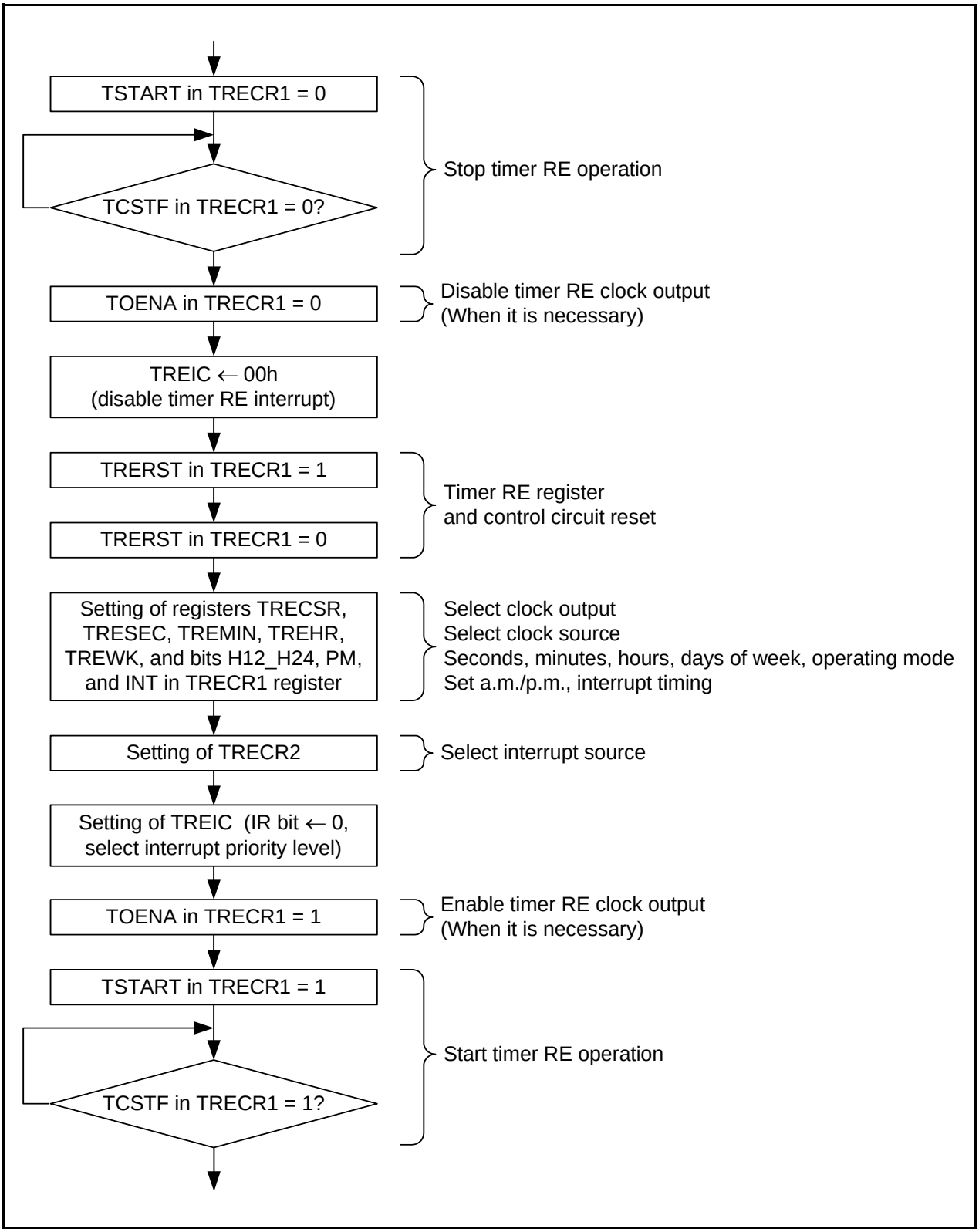


Figure 29.2 Setting Example in Real-Time Clock Mode

29.9.3 Time Reading Procedure of Real-Time Clock Mode

In real-time clock mode, read registers TRESEC, TREMIN, TREHR, and TREWK when time data is updated and read the PM bit in the TRECR1 register when the BSY bit is set to 0 (not while data is updated).
Also, when reading several registers, an incorrect time will be read if data is updated before another register is read after reading any register.
In order to prevent this, use the reading procedure shown below.

- Using an interrupt
  Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register in the timer RE interrupt routine.

- Monitoring with a program 1
  Monitor the IR bit in the TREIC register with a program and read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the IR bit in the TREIC register is set to 1 (timer RE interrupt request generated).

- Monitoring with a program 2

(1) Monitor the BSY bit.
(2) Monitor until the BSY bit is set to 0 after the BSY bit is set to 1 (approximately 62.5 ms while the BSY bit is set to 1).
(3) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register after the BSY bit is set to 0.

- Using read results if they are the same value twice

(1) Read necessary contents of registers TRESEC, TREMIN, TREHR, and TREWK and the PM bit in the TRECR1 register.
(2) Read the same register as (1) and compare the contents.
(3) Recognize as the correct value if the contents match. If the contents do not match, repeat until the read contents match with the previous contents.

Also, when reading several registers, read them as continuously as possible.

29.10 Notes on Serial Interface (UART0)

- When reading data from the U0RB register either in clock synchronous serial I/O mode or in clock asynchronous serial I/O mode, always read data in 16-bit units.
  When the high-order byte of the U0RB register is read, bits PER and FER in the U0RB register and the RI bit in the U0C1 register are set to 0.
  To check receive errors, read the U0RB register and then use the read data.

  Program example to read the receive buffer register:
  ```
  MOV.W    00A6H, R0    ; Read the U0RB register
  ```

- When writing data to the U0TB register in clock asynchronous serial I/O mode with 9-bit transfer data length, write data to the high-order byte first and then the low-order byte, in 8-bit units.

  Program example to write to the transmit buffer register:
  ```
  MOV.B    #XXH, 00A3H    ; Write to the high-order byte of the U0TB register
  MOV.B    #XXH, 00A2H    ; Write to the low-order byte of the U0TB register
  ```

29.11 Notes on Synchronous Serial Communication Unit

Set the IICSEL bit in the SSUIICSR register to 0 (select SSU function) to use the synchronous serial communication unit function.

29.12 Notes on I2C bus Interface

To use the I2C bus interface, set the IICSEL bit in the SSUIICSR register to 1 (I2C bus interface function selected).

29.12.1 Master Receive Mode

After a master receive operation is completed, when a stop condition generation or a start condition regeneration overlaps with the falling edge of the ninth clock cycle of SCL, an additional cycle is output after the ninth clock cycle.

29.12.1.1 Countermeasure

After a master receive operation is completed, confirm the falling edge of the ninth clock cycle of SCL and generate a stop condition or regenerate a start condition.
Confirm the falling edge of the ninth clock cycle of SCL as follows: Confirm the SCLO bit in the ICCR2 register (SCL monitor flag) becomes 0 (SCL pin is low) after confirming the RDRF bit in the ICSR register (receive data register full flag) becomes 1.

29.12.2 ICE Bit in ICCR1 Register and IICRST Bit in ICCR2 Register

When writing 0 to the ICE bit or 1 to the IICRST bit during an I2C bus interface operation, the BBSY bit in the ICCR2 register and the STOP bit in the ICSR register may become undefined.

29.12.2.1 Conditions When Bits Become Undefined

- When this module occupies the bus in master transmit mode (bits MST and TRS in the ICCR1 register are 1).
- When this module occupies the bus in master receive mode (the MST bit is 1 and the TRS bit is 0).
- When this module transmits data in slave transmit mode (the MST bit is 0 and the TRS bit is 1).
- When this module transmits an acknowledge in slave receive mode (bits MST and TRS are 0).

29.12.2.2 Countermeasures

- When the start condition (the SDA falling edge when SCL is high) is input, the BBSY bit becomes 1.
- When the stop condition (the SDA rising edge when SCL is high) is input, the BBSY bit becomes 0.
- When writing 1 to the BBSY bit, 0 to the SCP bit, and the start condition (the SDA falling edge when SCL is high) is output while SCL and SDA are high in master transmit mode, the BBSY bit becomes 1.
- When writing 0 to bits BBSY and SCP, the stop condition (the SDA rising edge when SCL is high) is output while SDA is low, and this is the only module that holds SCL low in master transmit mode or master receive mode, the BBSY bit becomes 0.
- When writing 1 to the FS bit in the SAR register, the BBSY bit becomes 0.

29.12.2.3 Additional Descriptions Regarding IICRST Bit

- When writing 1 to the IICRST bit, bits SDAO and SCLO in the ICCR2 register become 1.
- When writing 1 to the IICRST bit in master transmit mode and slave transmit mode, the TDRE bit in the ICSR register becomes 1.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, writing to bits BBSY, SCP, and SDAO is disabled. Write 0 to the IICRST bit before writing to the BBSY bit, SCP bit, or SDAO bit.
- Even when writing 1 to the IICRST bit, the BBSY bit does not become 0. However, the stop condition (the SDA rising edge when SCL is high) may be generated depending on the states of SCL and SDA and the BBSY bit may become 0. There may also be a similar effect on other bits.
- While the control block of the I2C bus interface is reset by setting the IICRST bit to 1, data transmission/reception is stopped. However, the function to detect the start condition, stop condition, or arbitration lost operates. The values in the ICCR1 register, ICCR2 register, or ICSR register may be updated depending on the signals applied to pins SCL and SDA.

29.13 Notes on Flash Memory

29.13.1 CPU Rewrite Mode

29.13.1.1 Prohibited Instructions

The following instructions cannot be used while the program ROM area is being rewritten in EW0 mode because they reference data in the flash memory: UND, INTO, and BRK.

29.13.1.2 Interrupts

Tables 29.1 to 29.3 show CPU Rewrite Mode Interrupts.

Table 29.1 CPU Rewrite Mode Interrupts (1)

Mode	Erase/ Write Target	Status	Maskable Interrupt
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Usable by allocating a vector in RAM.
		During auto-erasure (suspend disabled)	
		During auto-programming	
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit to 0.
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.
		During auto-programming	
	Program ROM	During auto-erasure (suspend enabled)	Auto-erasure suspends after td(SR-SUS) and interrupt handling is executed. Auto-erasure can be restarted by setting the FMR21 bit to 0 after interrupt handling completes. While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written.
		During auto-erasure (suspend disabled or FMR22 = 0)	Auto-erasure and auto-programming have priority and interrupt requests are put on standby. Interrupt handling is executed after auto-erase and auto-program complete.
		During auto-programming	

FMR21, FMR22: Bits in FMR2 register

Table 29.2 CPU Rewrite Mode Interrupts (2)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 1 (Note 1)	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW0	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1 (erase-suspend request enabled by interrupt request), the FMR21 bit is automatically set to 1 (erase-suspend request). The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0 (erase-suspend request disabled by interrupt request), set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

Table 29.3 CPU Rewrite Mode Interrupts (3)

Mode	Erase/ Write Target	Status	• Watchdog Timer • Oscillation Stop Detection • Voltage Monitor 1 (Note 1)	• Undefined Instruction • INTO Instruction • BRK Instruction • Single Step • Address Match • Address Break (Note 1)
EW1	Data flash	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, interrupt handling is executed. If the FMR22 bit is set to 1, the FMR21 bit is automatically set to 1. The flash memory suspends auto-erasure after td(SR-SUS). If erase-suspend is required while the FMR22 bit is set to 0, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit is set to 0 (erase restart).	When an interrupt request is acknowledged, interrupt handling is executed. If erase-suspend is required, set the FMR21 bit to 1 during interrupt handling. The flash memory suspends auto-erasure after td(SR-SUS). While auto-erasure is being suspended, any block other than the block during auto-erasure execution can be read or written. Auto-erasure can be restarted by setting the FMR21 bit in the FMR2 register is set to 0 (erase restart).
		During auto-erasure (suspend disabled or FMR22 = 0)	Interrupt handling is executed while auto-erasure or auto-programming is being performed.	
		During auto-programming		
	Program ROM	During auto-erasure (suspend enabled)	When an interrupt request is acknowledged, auto-erasure or auto-programming is forcibly stopped immediately and the flash memory is reset. Interrupt handling starts when the flash memory restarts after the fixed period. Since the block during auto-erasure or the address during auto-programming is forcibly stopped, the normal value may not be read. After the flash memory restarts, execute auto-erasure again and ensure it completes normally. The watchdog timer does not stop during the command operation, so interrupt requests may be generated. Initialize the watchdog timer regularly using the erase-suspend function.	Not usable during auto-erasure or auto-programming.
		During auto-erasure (suspend disabled or FMR22 = 0)		
		During auto-programming		

FMR21, FMR22: Bits in FMR2 register

Note:

1. Do not use a non-maskable interrupt while block 0 is being auto-erased because the fixed vector is allocated in block 0.

29.13.1.3 How to Access

To set one of the following bits to 1, first write 0 and then 1 immediately. Disable interrupts and DTC activation between writing 0 and writing 1.
- The FMR01 bit or FMR02 bit in the FMR0 register
- The FMR13 bit in the FMR1 register
- The FMR20 bit, FMR22 bit, or FMR 27 bit in the FMR2 register

To set one of the following bits to 0, first write 1 and then 0 immediately. Disable interrupts and DTC activation between writing 1 and writing 0.
- The FMR14 bit, FMR15 bit, FMR16 bit, or FMR17 bit in the FMR1 register

29.13.1.4 Rewriting User ROM Area

In EW0 mode, if the supply voltage drops while rewriting any block in which a rewrite control program is stored, it may not be possible to rewrite the flash memory because the rewrite control program cannot be rewritten correctly. In this case, use standard serial I/O mode.

29.13.1.5 Programming

Do not write additions to the already programmed address.

29.13.1.6 Entering Stop Mode or Wait Mode

Do not enter stop mode or wait mode during erase-suspend.
If the FST7 bit in the FST register is set to 0 (busy (during programming or erasure execution), do not enter to stop mode or wait mode.
Do not enter stop mode or wait mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

29.13.1.7 Programming and Erasure Voltage for Flash Memory

To program and erase program ROM in CPU rewrite mode, use Topr = 0 to 60°C as the operating ambient temperature. Do not program and erase program ROM under conditions other than Topr = 0 to 60°C.
To program and erase program ROM and data flash in standard serial I/O mode and parallel I/O mode, use VCC = 2.7 to 3.6 V as the supply voltage and Topr = 0 to 60°C as the operating ambient temperature. Do not program and erase program ROM and data flash when VCC is less than 2.7 V or under conditions other than Topr = 0 to 60°C.

29.13.1.8 Block Blank Check

Do not execute the block blank check command during erase-suspend.

29.13.1.9 Low-Current-Consumption Read Mode

In low-speed clock mode and low-speed on-chip oscillator mode, the current consumption when reading the flash memory can be reduced by setting the FMR27 bit in the FMR2 register to 1 (low-current-consumption read mode enabled).
Low-current-consumption read mode can be used when the CPU clock is set to either of the following:
- The CPU clock is set to the low-speed on-chip oscillator clock divided by 4, 8, or 16.
- The CPU clock is set to the XCIN clock divided by 1 (no division), 2, 4, or 8.

However, do not use low-current-consumption read mode when the frequency of the selected CPU clock is 3 kHz or below.
After setting the divide ratio of the CPU clock, set the FMR27 bit to 1 (low-current-consumption read mode enabled).
To reduce the power consumption, refer to **27. Reducing Power Consumption**.
Enter wait mode or stop mode after setting the FMR27 bit to 0 (low-current-consumption read mode disabled).
Do not enter wait mode or stop mode while the FMR27 bit is 1 (low-current-consumption read mode enabled).

29.13.2 Data Flash

Programs cannot be executed in the data flash.
Do not use the data flash as a program area.

29.14 Notes on Noise

29.14.1 Inserting a Bypass Capacitor between VCC and VSS Pins as a Countermeasure against Noise and Latch-up

Connect a bypass capacitor (10 μF) using the shortest and thickest wire possible.

29.14.2 Countermeasures against Noise Error of Port Control Registers

During rigorous noise testing or the like, external noise (mainly power supply system noise) can exceed the capacity of the MCU's internal noise control circuitry. In such cases the contents of the port related registers may be changed.

As a firmware countermeasure, it is recommended that the port registers, port direction registers, and pull-up control registers be reset periodically. However, examine the control processing fully before introducing the reset routine as conflicts may be created between the reset routine and interrupt routines.

29.15 Note on Supply Voltage Fluctuation

After reset is deasserted, the supply voltage applied to the VCC pin must meet either or both the allowable ripple voltage Vr (vcc) or ripple voltage falling gradient dVr (vcc)/dt shown in Figure 29.3.

Symbol	Parameter	Standard			Unit
		Min.	Typ.	Max.	
Vr (vcc)	Allowable ripple voltage			0.1 VCC	V
dVr (vcc)/dt	Ripple voltage falling gradient			10	V/ms

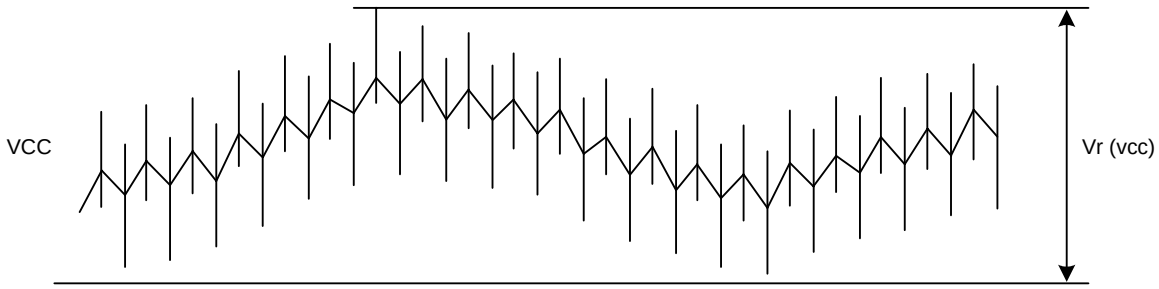


Figure 29.3 Definition of ripple voltage

30. Notes on On-Chip Debugger

When using the on-chip debugger to develop and debug programs for the R8C/3MQ Group, take note of the following.

(1) Some of the user flash memory and RAM areas are used by the on-chip debugger. These areas cannot be accessed by the user.
Refer to the on-chip debugger manual for which areas are used.
(2) Do not set the address match interrupt (registers AIER0, AIER1, RMAD0, and RMAD1 and fixed vector tables) in a user system.
(3) Do not use the BRK instruction in a user system.
(4) Debugging is available under the condition of supply voltage VCC = 2.7 V to 3.6 V.

Connecting and using the on-chip debugger has some special restrictions. Refer to the on-chip debugger manual for details.

31. Usage note for the development tool for R5F213MCQNNP

C/C++ Compiler Package for M16C Series and R8C Family [M3T-NC30WA] and On-chip Debugging Emulators E8a, E1 and E20 do not have the choice for 112 Kbytes program ROM. The recommended changes while using these development tools are described below.

31.1 C/C++ Compiler Package for M16C Series and R8C Family [M3T-NC30WA]

In creating the new project, select “128K” for “ROM size” menu (Figure 31.1(1)). In selecting “C source startup Application”, select “None” for “Use On-Chip Debugging Emulator” menu (Figure 31.1(2)). Address assignment of the firmware or the debug monitor for the on-chip debugging emulator is controlled by the emulator setting.

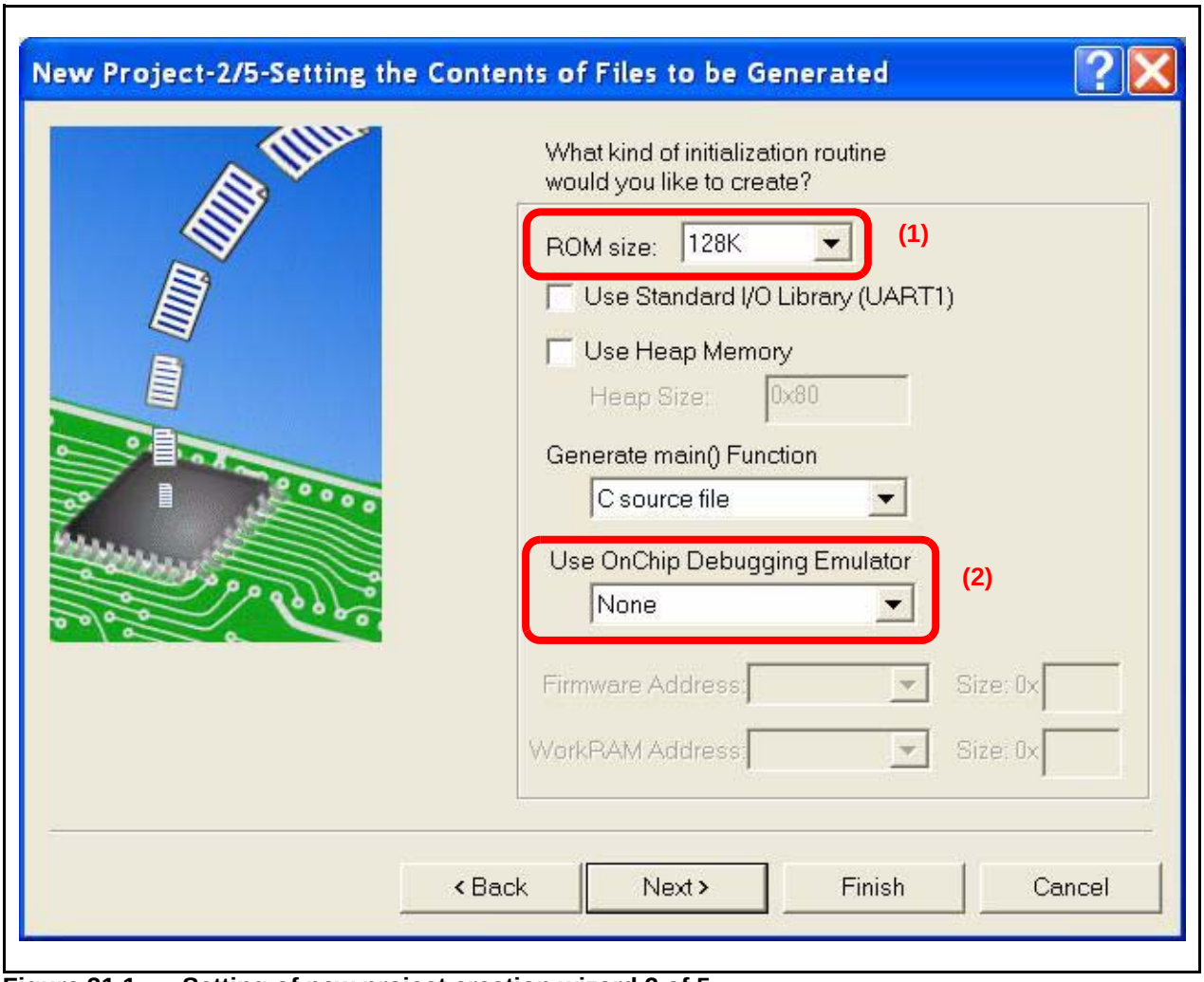


Figure 31.1 Setting of new project creation wizard 2 of 5

31.2 On-chip Debugging Emulator E8a

31.2.1 Firmware location

In starting the E8a emulator connection, select the “Firmware Location” tab on the “Emulator Setting” dialogue (Figure 31.2(1)) and check “Enable advanced setting” (figure Figure 31.3(2)). Then you can select the firmware location. Select “User Flash Area” for firmware location. Specify the address among the range from 04000h to 1FFFFh and do not include the fixed interrupt vector area. For example set there as 1F800 - 1FFFF like figure Figure 31.3(3). Do not select “Data Flash Area” for “Firmware Location” menu as the program code cannot be assigned on data flash.

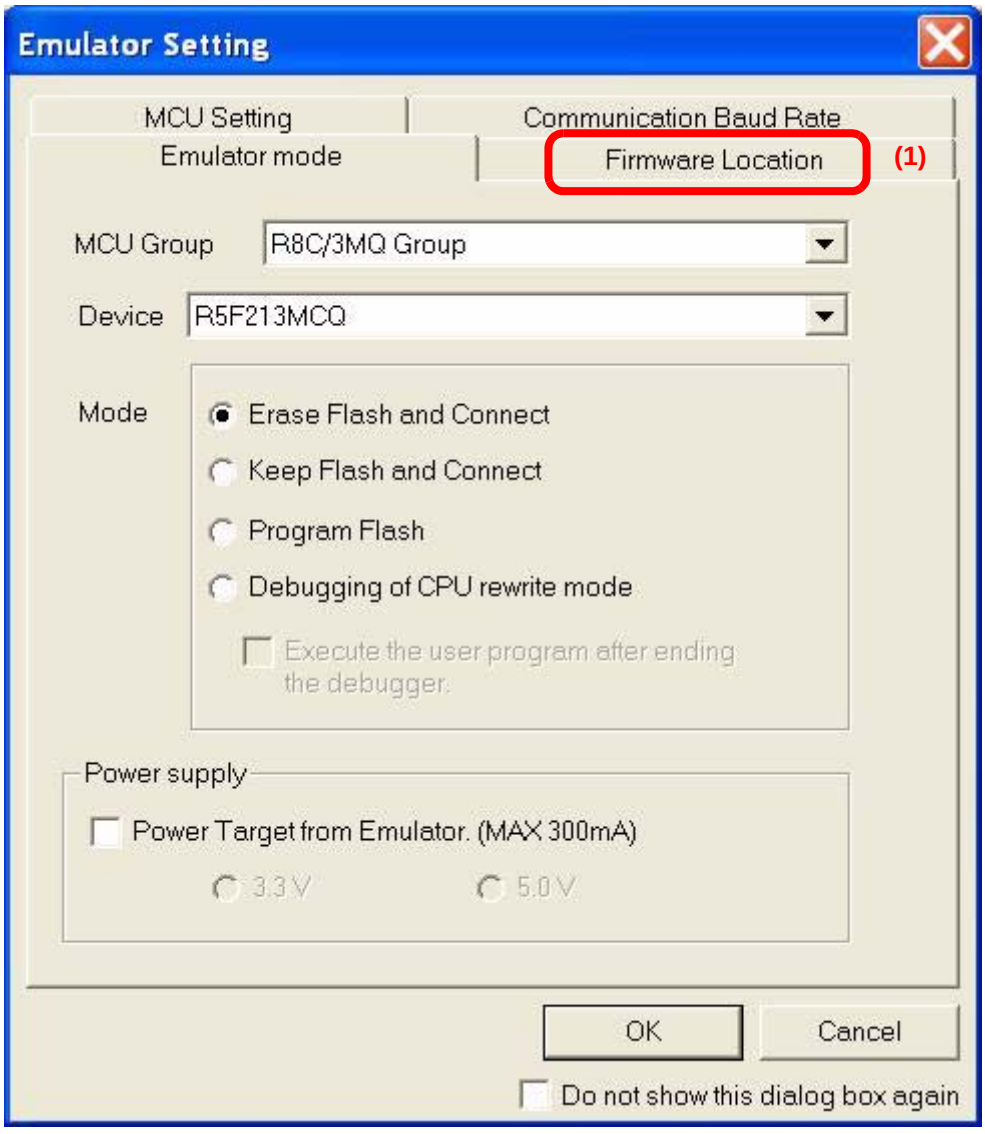


Figure 31.2 First “Emulator setting” dialogue for E8a

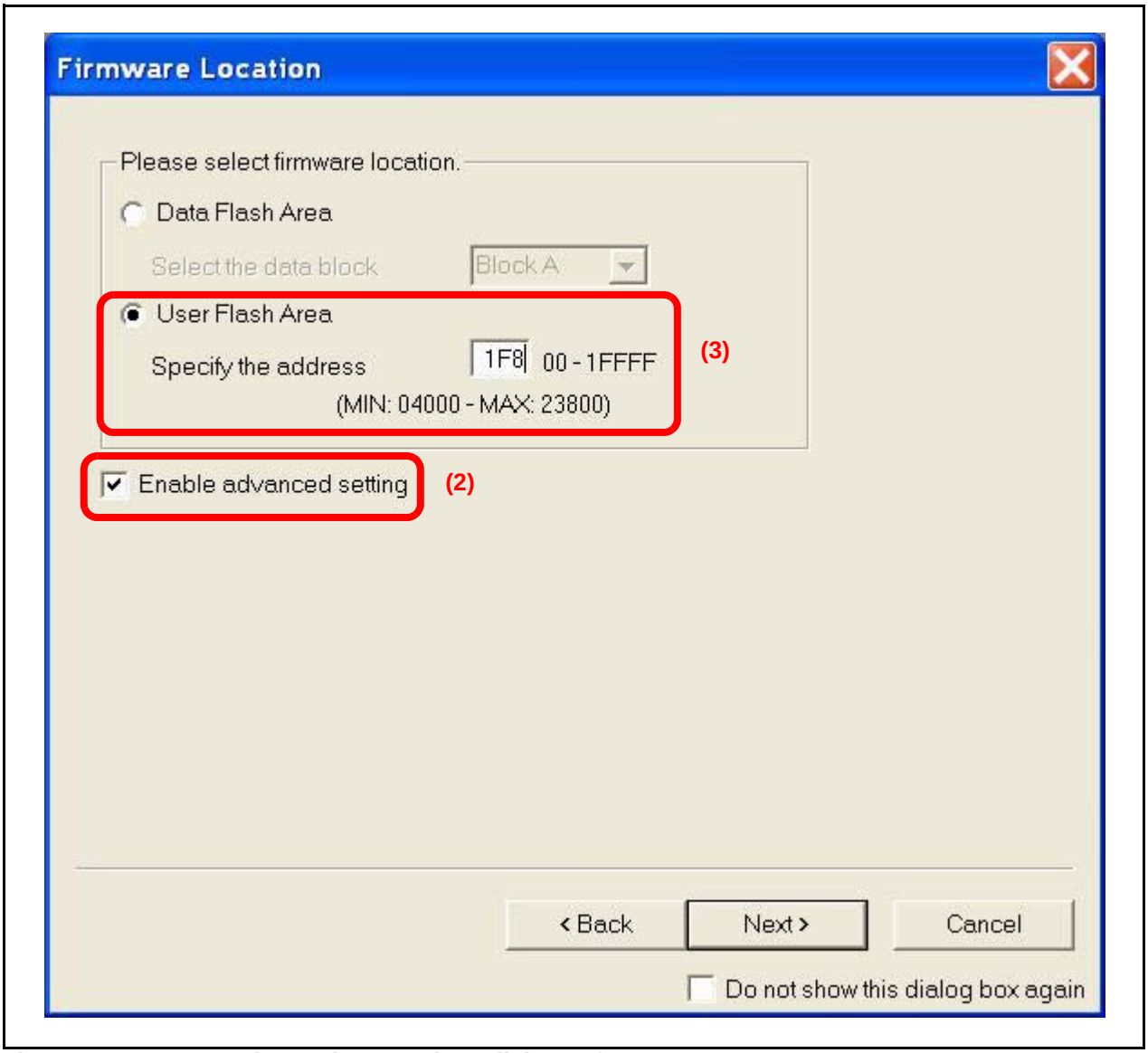


Figure 31.3 Second “Emulator setting” dialogue for E8a

31.2.2 Download the user program

No warning message will be displayed on the development tool window if the user program size exceeds the 112 Kbytes memory location area, in downloading the program code from the development tool to the device. Check the “map” file for the allocation of program code before download.

31.3 On-chip Debugging Emulators E1 and E20

31.3.1 Debug monitor location

In starting the E1 or E20 emulator connection, select the “System” tab on the “Configuration Properties” dialogue (Figure 31.4(1)) and specify the debug monitor location. Select “User flash area” for “Debug monitor location” menu. Specify the address among the range from 04000h to 1F800h and do not include the fixed interrupt vector area. For example set there as 1F800 - 1FFFF like Figure 31.4(2). Do not select “Data flash area” for “Debug monitor location” menu as the program code cannot be assigned on data flash.

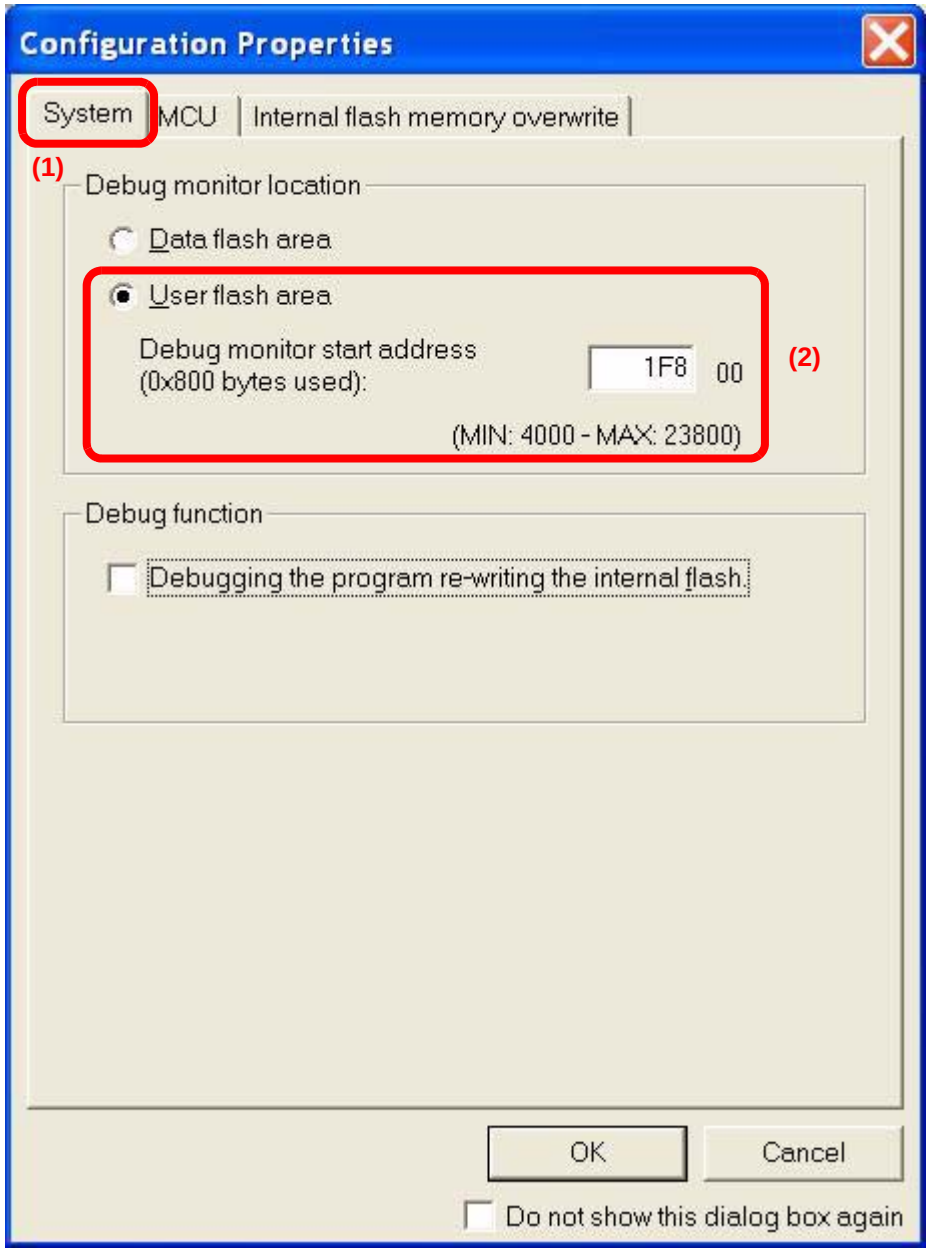


Figure 31.4 Setting of “Configuration Properties” for E1 and E20

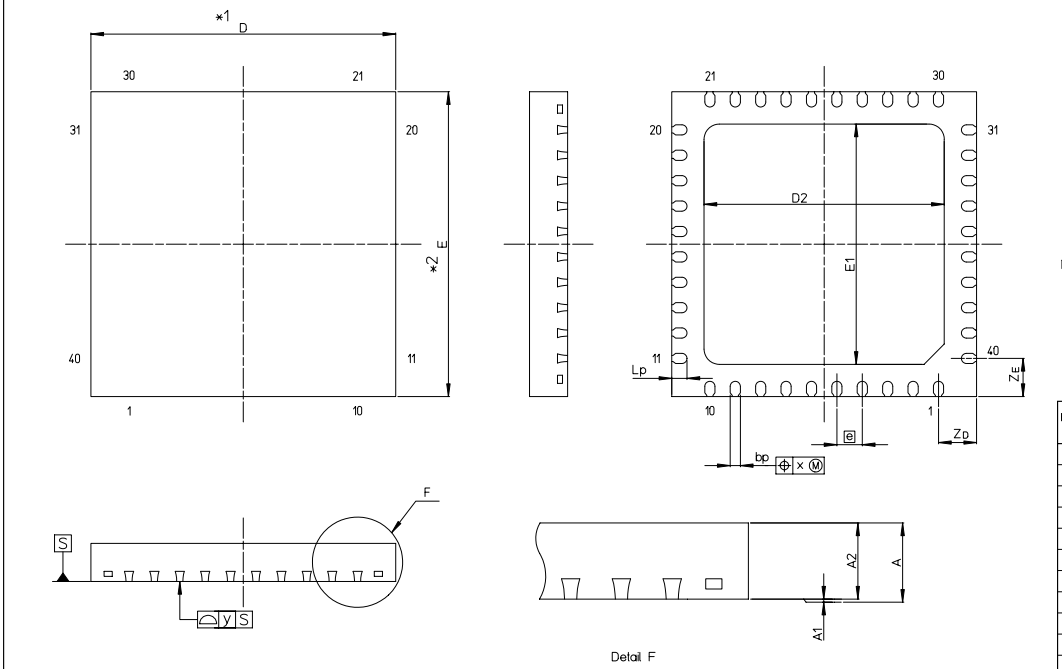
31.3.2 Download the user program

No warning message displayed on development tool window if the user program size exceeds the 112 Kbytes memory location area, in download the program code from the development tool to the device. Check the “map” file for the allocation of program code before download.

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN40-6x6-0.50	PWQN0040KB-A	40PJS-A	0.07g

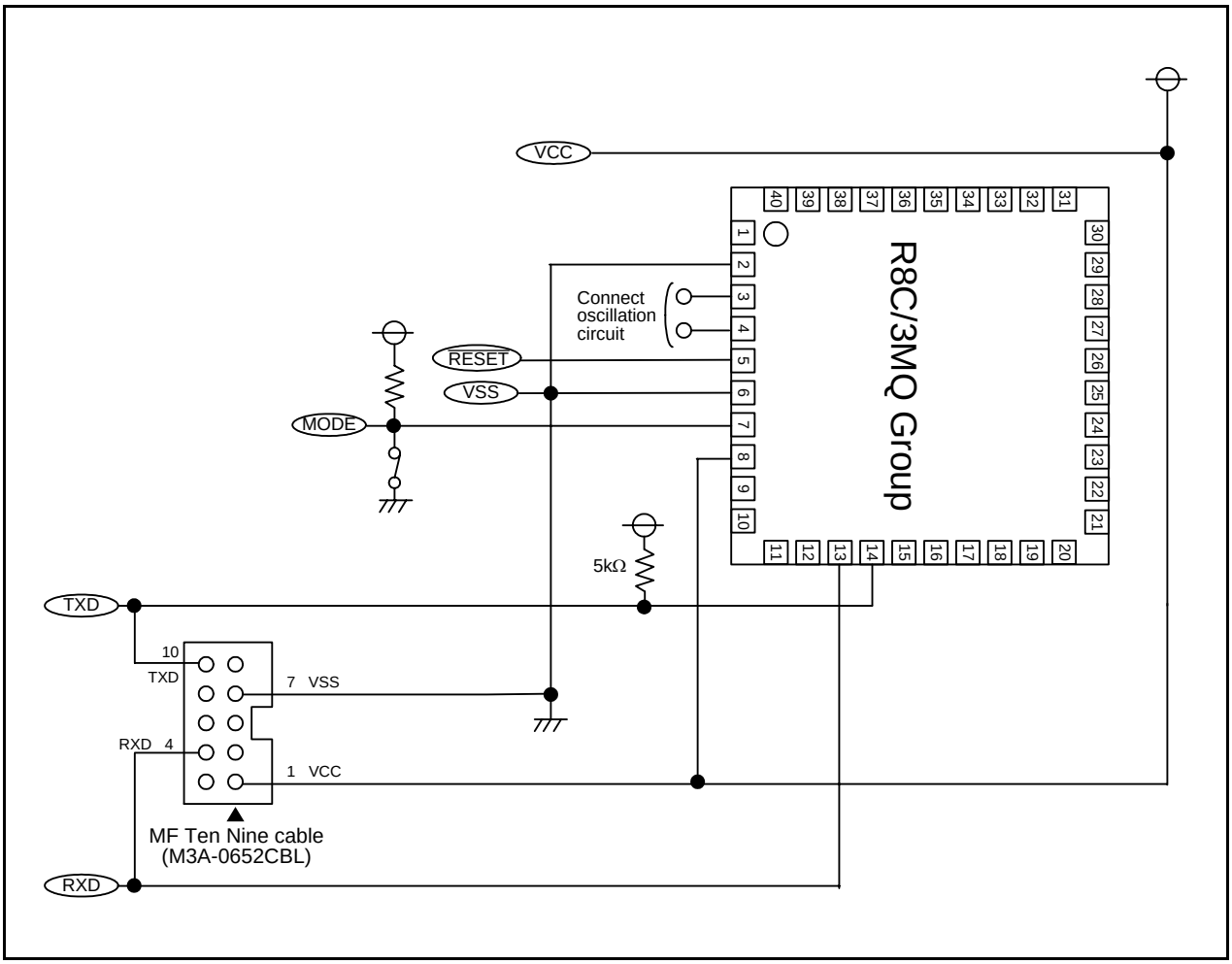


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.

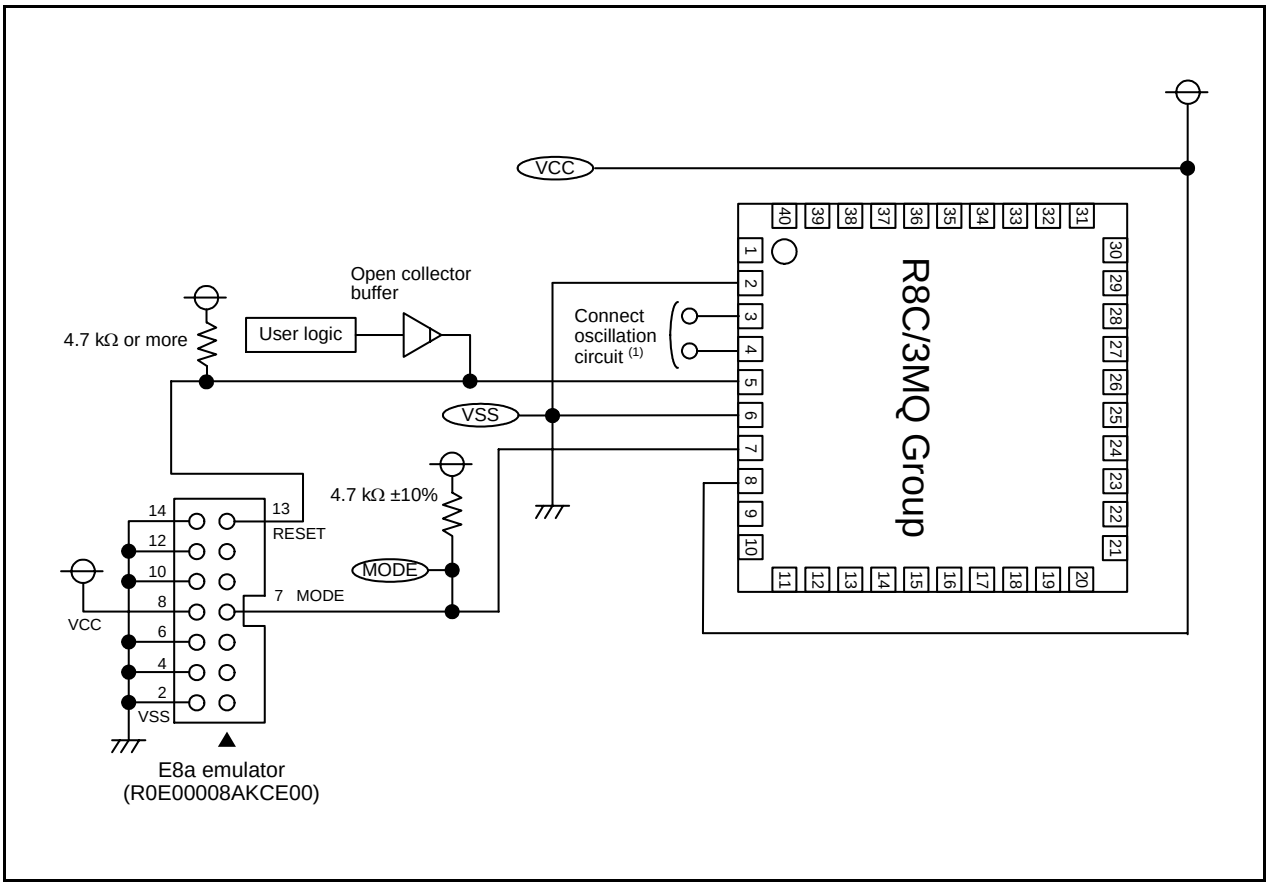
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.9	6.0	6.1
E	5.9	6.0	6.1
A2	—	0.75	—
A	—	—	0.8
A1	0	0	0.05
bp	0.15	0.2	0.25
e	—	0.5	—
Lp	0.2	0.3	0.4
x	—	—	0.05
y	—	—	0.05
ZD	—	0.75	—
ZE	—	0.75	—
D2	—	4.73	—
E1	—	4.73	—

Appendix 2. Connection Examples between Serial Programmer and On-Chip Debugging Emulator

Appendix Figure 2.1 shows a Connection Example with MF Ten Nine Cable (M3A-0652CBL) and Appendix Figure 2.2 shows a Connection Example with E8a Emulator (R0E00008AKCE00).



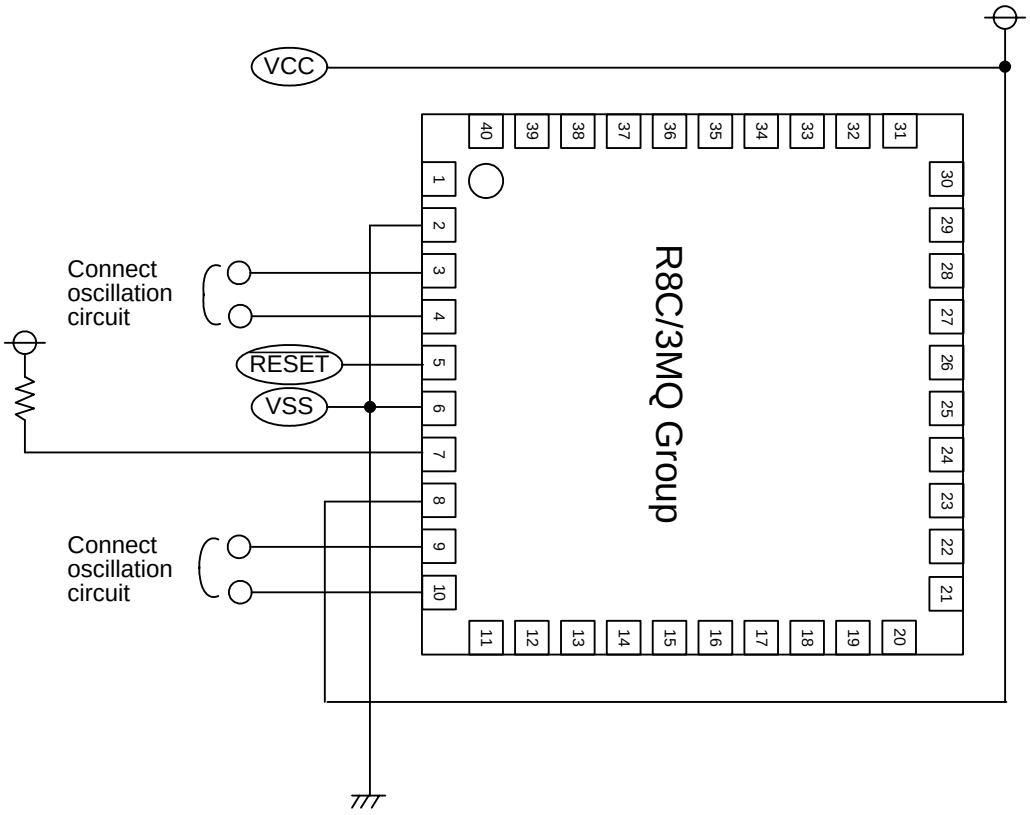
Appendix Figure 2.1 Connection Example with MF Ten Nine Cable (M3A-0652CBL)



Appendix Figure 2.2 Connection Example with E8a Emulator (R0E00008AKCE00)

Appendix 3. Example of Oscillation Evaluation Circuit

Appendix Figure 3.1 shows an Example of Oscillation Evaluation Circuit.

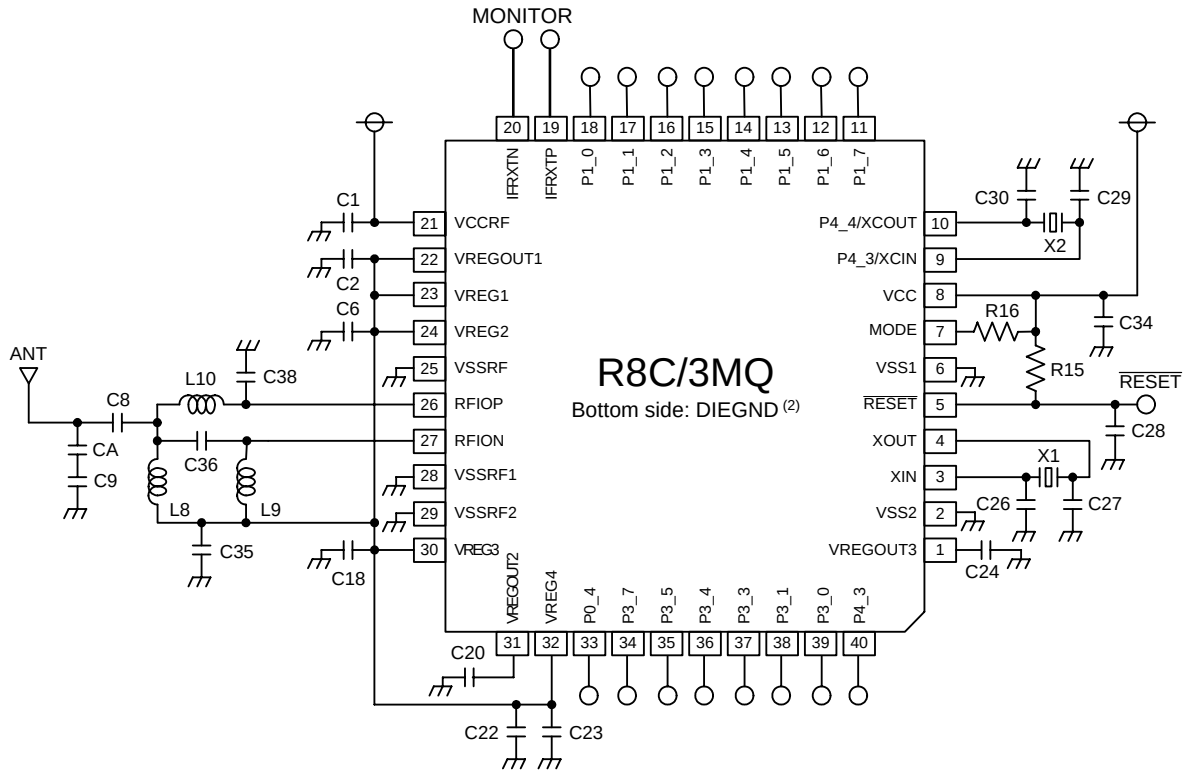


Notes:
1. Just after the reset, XIN and XCIN oscillation circuit aren't working. Set the XIN and XCIN oscillation circuit to work in the first step of program.
2. The recommended value of capacitor connected with pin 3 and pin 4 for crystal oscillation circuit need to be consulted with the crystal oscillator manufacturer as the oscillation signal duty coming within 45 to 55 percent.

Appendix Figure 3.1 Example of Oscillation Evaluation Circuit

Appendix 4. Example of Peripheral Circuit

Appendix Figure 4.1 shows an Example of Peripheral Circuit.



Appendix Table 4.1 LCR Constants

Part	Value	Part	Value
C1	10 µF	C28	100 pF (4)
C2	0.1 µF	C34	10 µF
C6	1 µF	C35	3.3 pF
C8	1.8 pF	C36	1.5 pF
C9	0.5 pF (3)	C38	2 pF
C18	1 µF		
C20	0.47 µF	CA	6.8 pF (3)
C22	0.1 µF	L8	33 nH
C23	100 pF	L9	1.5 nH
C24	0.1 µF	L10	1.0 nH
		R15	56 kΩ (4)
		R16	4.7 kΩ (5)

Appendix Table 4.2 X1 (16 MHz Crystal Oscillator)

Manufacturer Name	Part Number	CL	C26	C27
Nihon Dempa Kogyo Co., Ltd.	NX2520SA	12 pF	27 pF	8 pF
KYOCERA Crystal Device Corporation	CX2520DB	8 pF	27 pF	3 pF

Appendix Table 4.2 X2 (32.768 kHz Crystal Oscillator)

Manufacturer Name	Part Number	CL	C29	C30
Nihon Dempa Kogyo Co., Ltd.	NX3215SA	12.5 pF	18 pF	18 pF
KYOCERA Crystal Device Corporation	ST3215SB	7 pF	12 pF	12 pF

Appendix Table 4.4 L Marker Location

L8	VREGOUT1 side
L9	C36 side
L10	C38 side

Notes:
1. The constants are reference values for Renesas boards.
2. Connect the bottom side DIEGND to the board GND.
3. C9 and CA are used as notch filters for suppressing second harmonics for transmission output on Renesas boards. An inductor may be used for CA depending on the board wiring.
4. The optimal constants of R15 and C28 to be connected to the $\overline{\text{RESET}}$ pin (pin 5) will vary depending on applications and boards. Determine the optimal constants based on your system.
5. The recommended value of R16 to be connected to the MODE pin (pin 7) is 4.7 kΩ ±10%. Selecting a resistance other than this value may affect on-chip debugging. Careful evaluation should be performed in the user system before determining the value.
6. The optical constants of the crystal oscillator external circuit CIN and COUT will vary depending on the board, the oscillator, and the oscillation drive capacity. Use the values recommended by the crystal oscillator manufacturer.

Appendix Figure 4.1 Example of Peripheral Circuit

Appendix 5. Notes on Board Design

Each symbol corresponds to an example of the peripheral circuit shown in Appendix Figure 4.1.

[Power Supply]

- Be sure to connect the die pad of the IC bottom side to the GND because it is the GND reference point of the analog block.
- Pin 21 (VCCRF) and pin 8 (VCC) are 3 V power supply pins. Allocate C1 and C34 of 10 μF or more near the IC pins. When there is a large amount of noise at the power supply to be connected, the decoupling capacitance of C1 and C34 must be increased.
- Pin 22 (VREGOUT1) is a 1.45 V regulator output pin. Connect this pin to pins 23, 24, 30, and 32 (VREG1 to VREG4). Allocate each decoupling capacitance near the IC pins as below.
  C2 → 0.1 μF or more for stabilizing the internal regulator to pin 22 (VREGOUT1)
  C6 → 1 μF for stabilizing the internal RF/IF block to pin 24 (VREG2)
  C18 → 1 μF or more for stabilizing the internal PLL analog block to pin 30 (VREG3)
  C22, 23 → 0.1 μF for stabilizing the internal PLL digital block and 120 pF for reducing noise to pin 32 (VREG4)
  Select the constants so that the total of the above capacitance is 2.2 μF or more.
- Make sure that the wiring from VREGOUT1 to VREG3 and VREG4 and the RFIOP/N line path cross at minimum.
- Pin 31 (VREGOUT2) and pin 1 (VREGOUT3) are regulator decoupling pins for the VCO and crystal buffer. Allocate C20 and C24 near the IC pins.

[RF]

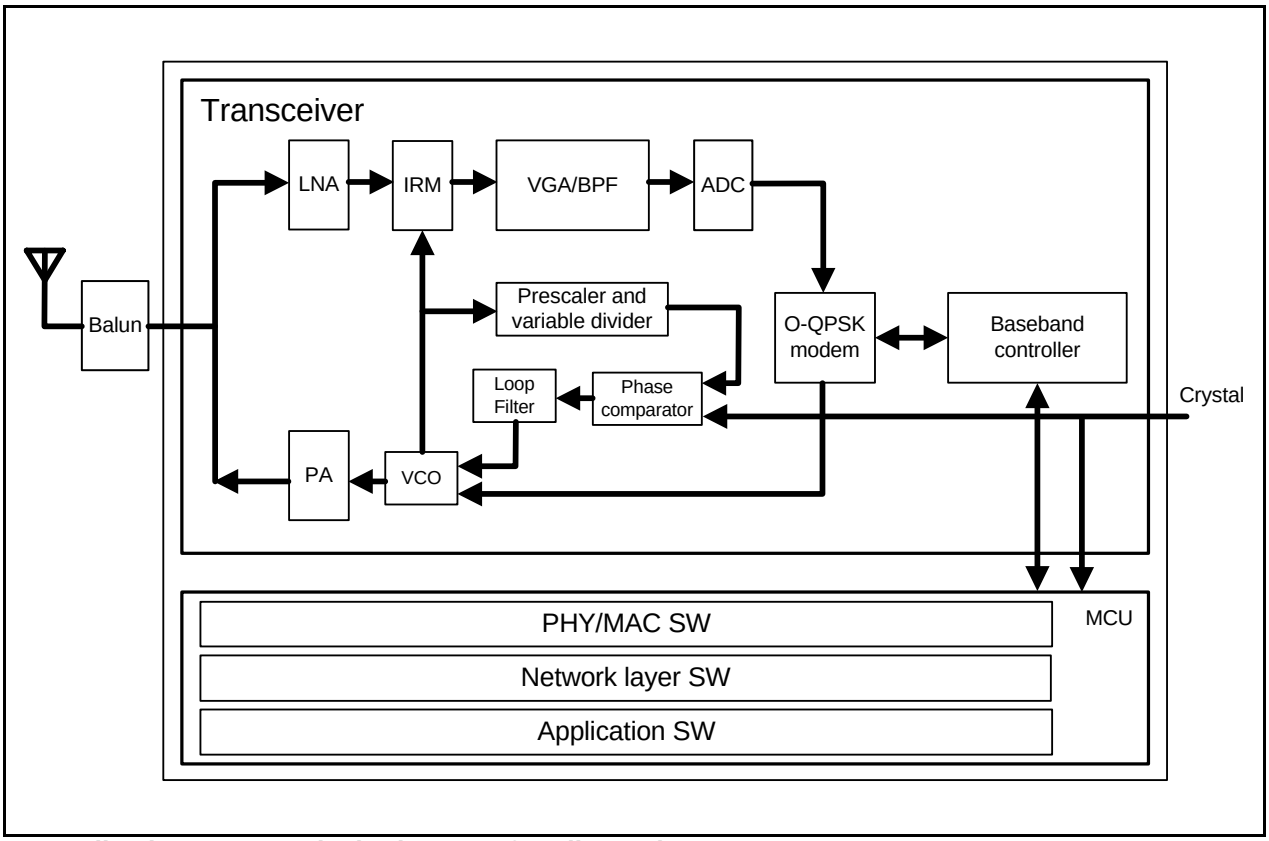
- Pins 26 and 27 are differential I/O pins for the 2.4 GHz band. Connect these pins using the shortest possible wiring. The side of this wiring must be guarded with the GND wiring of pins 25 and 28. Also, drill many via holes at equal spaces.
- Be sure to connect pins 28 and 29 (pins VSSRF1 and VSSRF2) to the GND to ensure RF isolation between pins 27 and 30.
- For the LC of the BALUN block, use contact C side (C38) close to pin 26 (RFIOP) to avoid RFIO to VCO interference via the GND.
- L1 and C9 are used as notch filters for suppressing second harmonics for transmission output. Adjust them to reduce the 4.8 GHz band.
- Adjust the balance of the BALUN block to set S11 (S22) to -6 dB or lower in each receive mode and transmit mode. Also, finely adjust the phase block (LC/CL) to set the local leak (RFIN - 2 MHz) to about -58 to -60 dBm.

[Others]

- Pins 19 and 20 (IFRXTP/N) are TESTIO pins. It is recommended that monitor pads be prepared.

Appendix 6. Block Diagram of Radio Equipment

Appendix Figure 6.1 shows a Block Diagram of Radio Equipment.



Appendix Figure 6.1 Block Diagram of Radio Equipment

Index

REVISION HISTORY	R8C/3MQ Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.00	Aug 11, 2011	—	First Edition issued
2.00	Jun 29, 2012	2	Table 1.1 "Voltage detection" revised, Table 1.2 "2.2 V" → "2.15 V"
		3, 4	Tables 1.2 and 1.3 "2.2 V" → "2.15 V"
		5	Table 1.4 and Figure 1.1 revised
		6	Figure 1.2 revised
		14	Figure 3.1 revised
		30, 48, 155, 162, 442	5.1.3, 6.2.8, 13.2.1, 14.2.6, and 26.3.3 b4 and b5 revised, Note 2 and LVDAS bit description added
		35	5.4 description revised
		38	6.1 description, Table 6.1 "Detection voltage" revised
		39	Figure 6.1 revised
		40	Figure 6.2 revised
		44	6.2.4 description added
		71, 97, 349	7.4.10, 9.2.7, and 24.2.3 Note 1 added
		98	Figure 9.3 Note 1 revised
		147, 505	11.9.3 and 29.2.3 "2.2 V" → "2.15 V"
		182	15.3.6 description revised
		187, 509	"15.4.5" and "29.5.5" added
		190	17.2.1 Note 4 revised
		244	Table 19.7 "Count period" revised
		273, 513	19.9.4 and 29.8.4 description revised
		355	24.2.10 Notes 5 and 6 revised
		396	Figure 25.9 revised
		408	25.2.11 b6 and b7 "R/W" → "—"
		410	25.2.13 RCVTRG and CCATRG Bit description revised
		417	25.2.19 and 25.2.20 Bit description revised
		436	"25.4.4" added
		439	26.2 description revised
		440	Figure 26.1 revised
		443	Table 26.3 "CPU clock" revised
		462 to 464	Figures 26.10 to 26.12 title revised
		465	26.4.11.4 "When the FMR 22 bit is ... auto-erased in EW1 mode.", Figure 26.13 added
		479, 523	"26.7.2" and "29.13.2" added
		484	Table 28.2 "2.2 V" → "2.15 V"
		488	Table 28.5 revised
		495	Table 28.13 "2.2 V" → "2.15 V"
		499	Table 28.18 "2.2 V" → "2.15 V"
		500, 501	Timing requirements, Figures 28.11 to 28.13, titles "2.2 V" → "2.15 V"
		502	Table 28.23 revised
		524	29.14.1 description revised
		526 to 529	"31. Usage note for the development tool for R5F213MCQNNP" added
		533	Appendix Figure 3.1 revised
		534	"Appendix 4" added

REVISION HISTORY	R8C/3MQ Group User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
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		536	"Appendix 6" added

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