

# BF1217WR

N-channel dual gate MOSFET

Rev. 2 — 20 June 2011

Product data sheet

## 1. Product profile

---

### 1.1 General description

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1217WR is encapsulated in the SOT343R plastic package.

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

### 1.2 Features and benefits

- Excellent low frequency noise performance
- Superior cross modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio

### 1.3 Applications

- Gain controlled low noise amplifiers for VHF and UHF applications with 5 V supply voltage
  - ◆ digital and analog television tuners
  - ◆ professional communication equipment

### 1.4 Quick reference data

**Table 1. Quick reference data**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	DC	-	-	6	V
$I_D$	drain current	DC	-	-	30	mA
$P_{tot}$	total power dissipation	$T_{sp} \leq 107\text{ }^\circ\text{C}$	[1]	-	180	mW
$ y_{fs} $	forward transfer admittance	$f = 100\text{ MHz}; T_j = 25\text{ }^\circ\text{C}; I_D = 18\text{ mA}$	23	27	38	mS
$C_{iss(G1)}$	input capacitance at gate1	$f = 100\text{ MHz}$	[2]	-	2.5	pF
$C_{rss}$	reverse transfer capacitance	$f = 100\text{ MHz}$	[2]	-	20	fF
NF	noise figure	$f = 400\text{ MHz}; Y_S = Y_{S(opt)}$	-	1.0	-	dB
		$f = 800\text{ MHz}; Y_S = Y_{S(opt)}$	-	1.5	-	dB
Xmod	cross modulation	input level for $k = 1\%$ at 40 dB AGC; $f_w = 50\text{ MHz}; f_{unw} = 60\text{ MHz}$	[3]	105	107	-
$T_j$	junction temperature		-	-	150	$^\circ\text{C}$

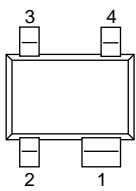
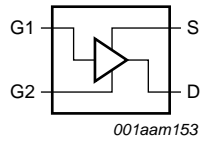
[1]  $T_{sp}$  is the temperature at the soldering point of the source lead.

[2] Calculated from S-parameters.

[3] Measured in [Figure 17](#) test circuit.

## 2. Pinning information

**Table 2. Discrete pinning**

Pin	Description	Simplified outline	Graphic symbol
1	source		
2	drain		
3	gate 2		
4	gate 1		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BF1217WR	-	plastic surface-mounted package; reverse pinning; 4 leads	SOT343R

## 4. Marking

**Table 4. Marking**

Type number	Marking	Description
BF1217WR	VA%	% = p : made in Hong Kong
		% = t : made in Malaysia
		% = w : made in China

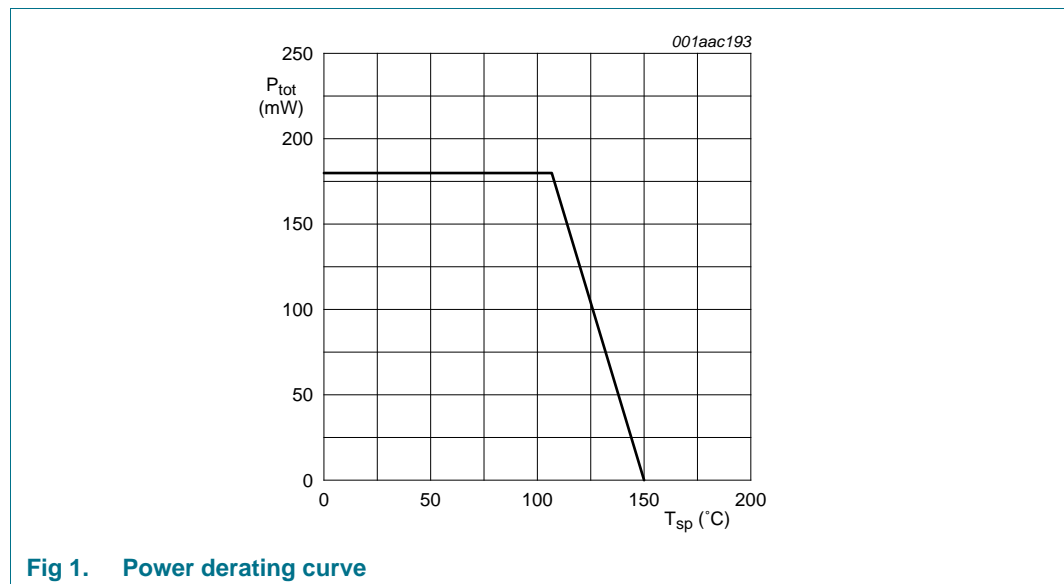
## 5. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>Per MOSFET</b>					
$V_{DS}$	drain-source voltage	DC	-	6	V
$I_D$	drain current	DC	-	30	mA
$I_{G1}$	gate1 current		-	±10	mA
$I_{G2}$	gate2 current		-	±10	mA
$P_{tot}$	total power dissipation	$T_{sp} \leq 107\text{ °C}$ [1]	-	180	mW
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	150	°C

[1]  $T_{sp}$  is the temperature at the soldering point of the source lead.



**Fig 1. Power derating curve**

## 6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		240	K/W

## 7. Static characteristics

Table 7. Static characteristics

$T_j = 25\text{ }^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per MOSFET; unless otherwise specified</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0\text{ V}$ ; $I_D = 10\text{ }\mu\text{A}$	6	-	-	V
$V_{(BR)G1-SS}$	gate1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0\text{ V}$ ; $I_{G1-S} = 10\text{ mA}$	6	-	10	V
$V_{(BR)G2-SS}$	gate2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0\text{ V}$ ; $I_{G2-S} = 10\text{ mA}$	6	-	10	V
$V_{F(S-G1)}$	forward source-gate1 voltage	$V_{G2-S} = V_{DS} = 0\text{ V}$ ; $I_{S-G1} = 10\text{ mA}$	0.5	-	1.5	V
$V_{F(S-G2)}$	forward source-gate2 voltage	$V_{G1-S} = V_{DS} = 0\text{ V}$ ; $I_{S-G2} = 10\text{ mA}$	0.5	-	1.5	V
$V_{G1-S(th)}$	gate1-source threshold voltage	$V_{DS} = 5\text{ V}$ ; $V_{G2-S} = 4\text{ V}$ ; $I_D = 100\text{ }\mu\text{A}$	0.3	-	1.0	V
$V_{G2-S(th)}$	gate2-source threshold voltage	$V_{DS} = 5\text{ V}$ ; $V_{G1-S} = 5\text{ V}$ ; $I_D = 100\text{ }\mu\text{A}$	0.4	-	1.0	V
$I_{DS}$	drain-source current	$V_{G2-S} = 4\text{ V}$ ; $V_{DS} = 5\text{ V}$ ; $R_{G1} = 82\text{ k}\Omega$	[1]	-	24	mA
$I_{G1-S}$	gate1 cut-off current	$V_{G2-S} = 0\text{ V}$ ; $V_{DS} = 0\text{ V}$ ; $V_{G1-S} = 5\text{ V}$	-	-	50	nA
$I_{G2-S}$	gate2 cut-off current	$V_{G2-S} = 4\text{ V}$ ; $V_{DS} = 0\text{ V}$ ; $V_{G1-S} = 0\text{ V}$	-	-	20	nA

[1]  $R_{G1}$  connects gate1 to  $V_{GG} = 5\text{ V}$ . See [Figure 17](#).

## 8. Dynamic characteristics

**Table 8. Dynamic characteristics**

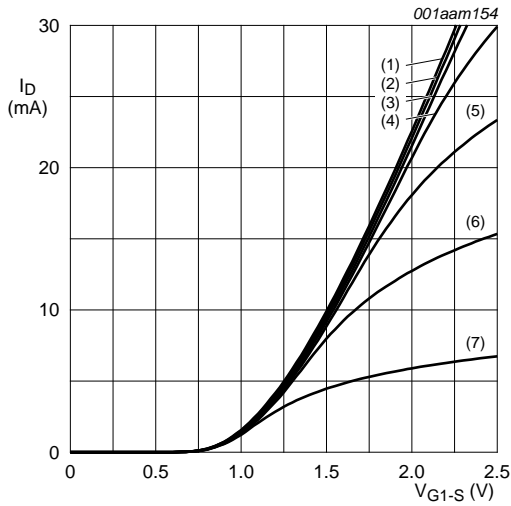
Common source;  $T_{amb} = 25\text{ °C}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $V_{DS} = 5\text{ V}$ ;  $I_D = 18\text{ mA}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$ y_{fs} $	forward transfer admittance	$f = 100\text{ MHz}$ ; $T_j = 25\text{ °C}$	23	27	38	mS
$C_{iss(G1)}$	input capacitance at gate1	$f = 100\text{ MHz}$	[1]	-	2.5	pF
$C_{iss(G2)}$	input capacitance at gate2	$f = 100\text{ MHz}$	[1]	-	1.0	pF
$C_{oss}$	output capacitance	$f = 100\text{ MHz}$	[1]	-	0.8	pF
$C_{rss}$	reverse transfer capacitance	$f = 100\text{ MHz}$	[1]	-	20	fF
$G_{tr}$	transducer power gain	$B_S = B_{S(opt)}$ ; $B_L = B_{L(opt)}$	[1]			
		$f = 200\text{ MHz}$ ; $G_S = 2\text{ mS}$ ; $G_L = 0.5\text{ mS}$	-	34	-	dB
		$f = 400\text{ MHz}$ ; $G_S = 2\text{ mS}$ ; $G_L = 1\text{ mS}$	-	30	-	dB
		$f = 800\text{ MHz}$ ; $G_S = 3.3\text{ mS}$ ; $G_L = 1\text{ mS}$	-	26	-	dB
NF	noise figure	$f = 400\text{ MHz}$ ; $Y_S = Y_{S(opt)}$	-	1.0	-	dB
		$f = 800\text{ MHz}$ ; $Y_S = Y_{S(opt)}$	-	1.5	-	dB
Xmod	cross modulation	input level for $k = 1\%$ ; $f_w = 50\text{ MHz}$ ; $f_{unw} = 60\text{ MHz}$	[2]			
		at 0 dB AGC	90	104	-	dB $\mu$ V
		at 10 dB AGC	-	100	-	dB $\mu$ V
		at 20 dB AGC	-	104	-	dB $\mu$ V
		at 40 dB AGC	105	107	-	dB $\mu$ V

[1] Calculated from S-parameters.

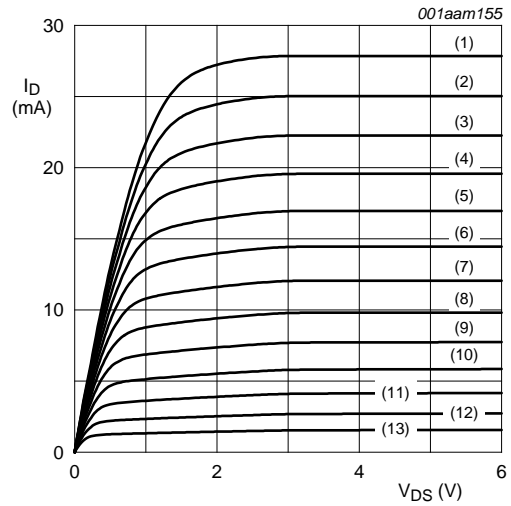
[2] Measured in [Figure 17](#) test circuit.

**8.1 Graphs**



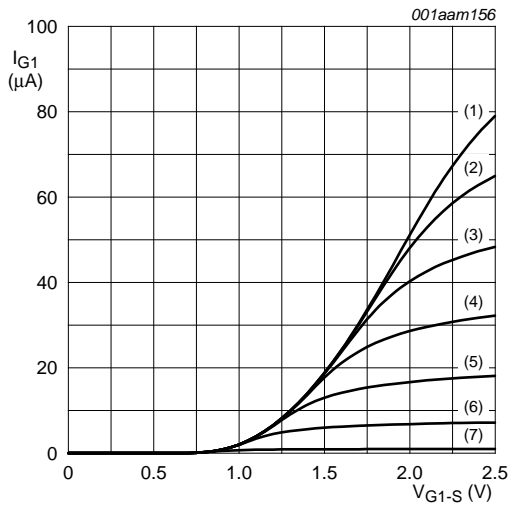
- (1)  $V_{G2-S} = 4.0\text{ V}$
  - (2)  $V_{G2-S} = 3.5\text{ V}$
  - (3)  $V_{G2-S} = 3.0\text{ V}$
  - (4)  $V_{G2-S} = 2.5\text{ V}$
  - (5)  $V_{G2-S} = 2.0\text{ V}$
  - (6)  $V_{G2-S} = 1.5\text{ V}$
  - (7)  $V_{G2-S} = 1.0\text{ V}$
- $V_{DS} = 5\text{ V}; T_j = 25\text{ }^\circ\text{C}.$

**Fig 2. Transfer characteristics; typical values**



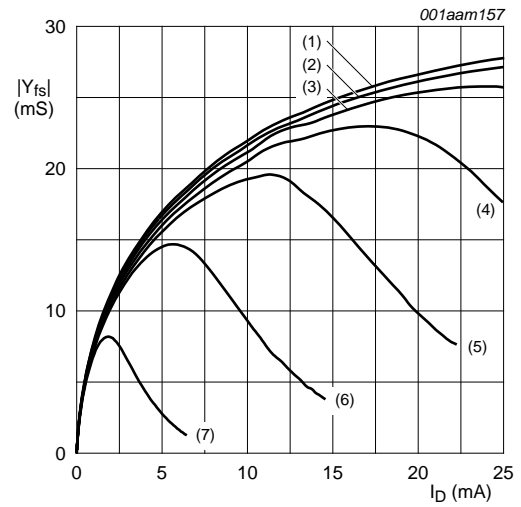
- (1)  $V_{G1-S} = 2.2\text{ V}$
  - (2)  $V_{G1-S} = 2.1\text{ V}$
  - (3)  $V_{G1-S} = 2.0\text{ V}$
  - (4)  $V_{G1-S} = 1.9\text{ V}$
  - (5)  $V_{G1-S} = 1.8\text{ V}$
  - (6)  $V_{G1-S} = 1.7\text{ V}$
  - (7)  $V_{G1-S} = 1.6\text{ V}$
  - (8)  $V_{G1-S} = 1.5\text{ V}$
  - (9)  $V_{G1-S} = 1.4\text{ V}$
  - (10)  $V_{G1-S} = 1.3\text{ V}$
  - (11)  $V_{G1-S} = 1.2\text{ V}$
  - (12)  $V_{G1-S} = 1.1\text{ V}$
  - (13)  $V_{G1-S} = 1.0\text{ V}$
- $V_{G2-S} = 4\text{ V}; T_j = 25\text{ }^\circ\text{C}.$

**Fig 3. Output characteristics; typical values**



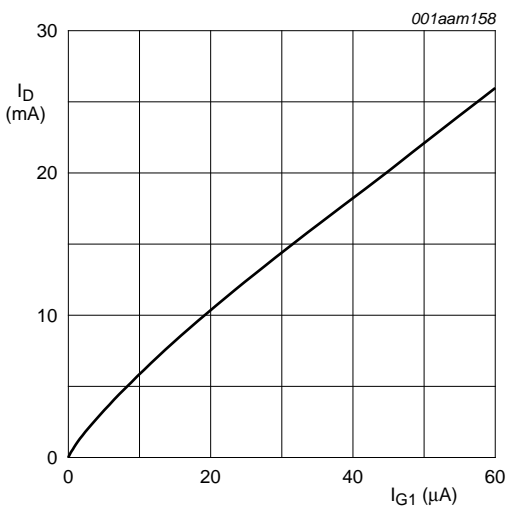
- (1)  $V_{G2-S} = 4.0\text{ V}$
  - (2)  $V_{G2-S} = 3.5\text{ V}$
  - (3)  $V_{G2-S} = 3.0\text{ V}$
  - (4)  $V_{G2-S} = 2.5\text{ V}$
  - (5)  $V_{G2-S} = 2.0\text{ V}$
  - (6)  $V_{G2-S} = 1.5\text{ V}$
  - (7)  $V_{G2-S} = 1.0\text{ V}$
- $V_{DS} = 5\text{ V}; T_j = 25\text{ }^\circ\text{C}.$

**Fig 4. Gate1 current as a function of gate1 voltage; typical values**



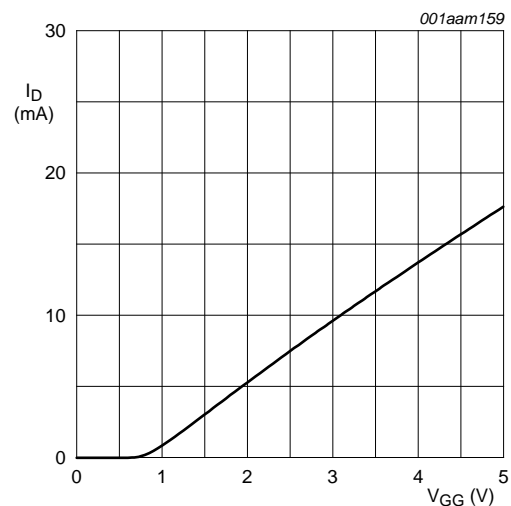
- (1)  $V_{G2-S} = 4.0\text{ V}$
  - (2)  $V_{G2-S} = 3.5\text{ V}$
  - (3)  $V_{G2-S} = 3.0\text{ V}$
  - (4)  $V_{G2-S} = 2.5\text{ V}$
  - (5)  $V_{G2-S} = 2.0\text{ V}$
  - (6)  $V_{G2-S} = 1.5\text{ V}$
  - (7)  $V_{G2-S} = 1.0\text{ V}$
- $V_{DS} = 5\text{ V}; T_j = 25\text{ }^\circ\text{C}.$

**Fig 5. Forward transfer admittance as a function of drain current; typical values**



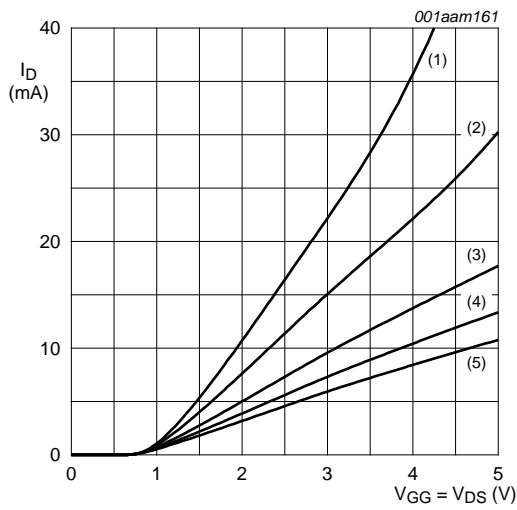
$V_{DS} = 5\text{ V}; V_{G2-S} = 4\text{ V}; T_j = 25\text{ }^\circ\text{C}.$

**Fig 6. Drain current as a function of gate1 current; typical values**



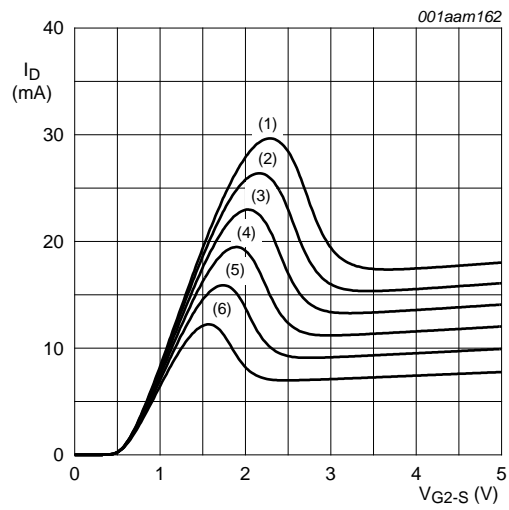
$V_{DS} = 5\text{ V}; V_{G2-S} = 4\text{ V}; R_{G1} = 82\text{ k}\Omega; T_j = 25\text{ }^\circ\text{C}.$

**Fig 7. Drain current as a function of gate1 supply voltage ( $V_{GG}$ ); typical values**



- (1)  $R_{G1} = 20 \text{ k}\Omega$
  - (2)  $R_{G1} = 40 \text{ k}\Omega$
  - (3)  $R_{G1} = 80 \text{ k}\Omega$
  - (4)  $R_{G1} = 120 \text{ k}\Omega$
  - (5)  $R_{G1} = 160 \text{ k}\Omega$
- $V_{G2-S} = 4 \text{ V}; T_j = 25 \text{ }^\circ\text{C}.$

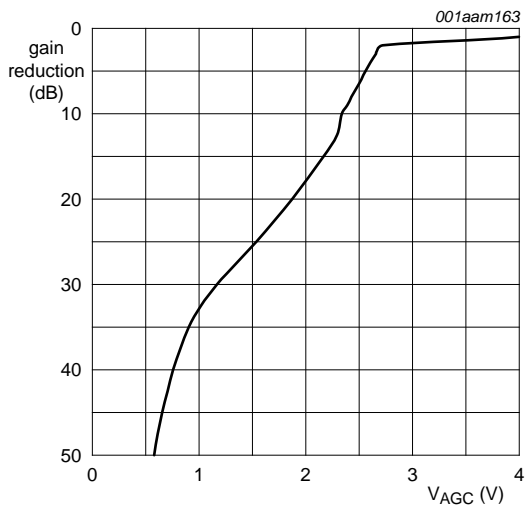
**Fig 8. Drain current as a function of  $V_{DS}$  and  $V_{GG}$ ; typical values**



- (1)  $V_{GG} = 5.0 \text{ V}$
  - (2)  $V_{GG} = 4.5 \text{ V}$
  - (3)  $V_{GG} = 4.0 \text{ V}$
  - (4)  $V_{GG} = 3.5 \text{ V}$
  - (5)  $V_{GG} = 3.0 \text{ V}$
  - (6)  $V_{GG} = 2.5 \text{ V}$
- $T_j = 25 \text{ }^\circ\text{C}; R_{G1} = 82 \text{ k}\Omega$  (connected to  $V_{GG}$ ).

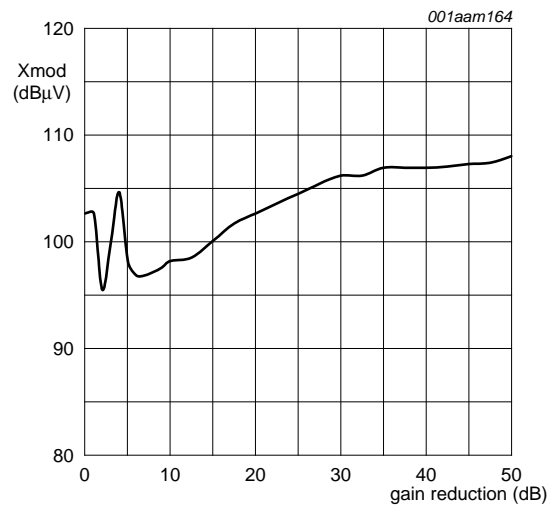
**Fig 9. Drain current as a function of gate2 voltage; typical values**





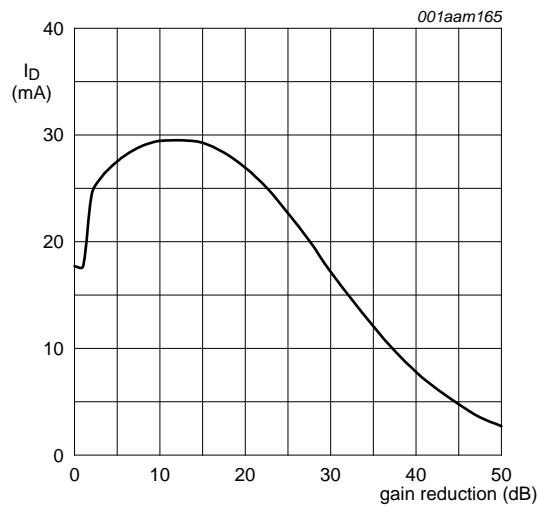
$V_{DS} = 5\text{ V}$ ;  $V_{GG} = 5\text{ V}$ ;  $I_{D(nom)} = 19\text{ mA}$ ;  $R_{G1} = 82\text{ k}\Omega$ ;  $f = 50\text{ MHz}$ ;  $T_j = 25\text{ }^\circ\text{C}$ ; see [Figure 17](#).

**Fig 10. Typical gain reduction as a function of the AGC voltage; typical values**



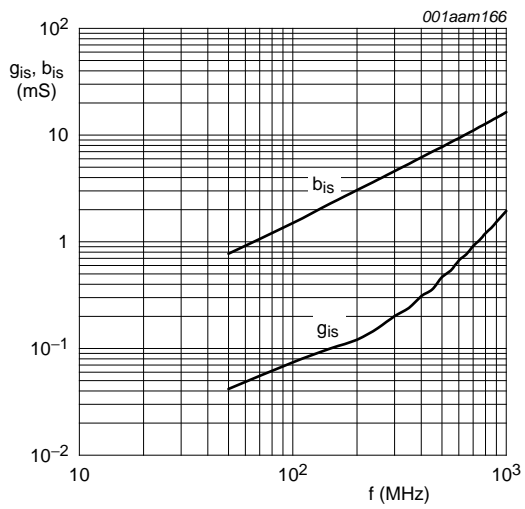
$V_{DS} = 5\text{ V}$ ;  $V_{GG} = 5\text{ V}$ ;  $V_{G2-S(nom)} = 4\text{ V}$ ;  $R_{G1} = 82\text{ k}\Omega$ ;  $f_w = 50\text{ MHz}$ ;  $f_{unw} = 60\text{ MHz}$ ;  $I_{D(nom)} = 19\text{ mA}$ ;  $T_j = 25\text{ }^\circ\text{C}$ ; see [Figure 17](#).

**Fig 11. Unwanted voltage for 1% cross modulation as a function of gain reduction; typical values**



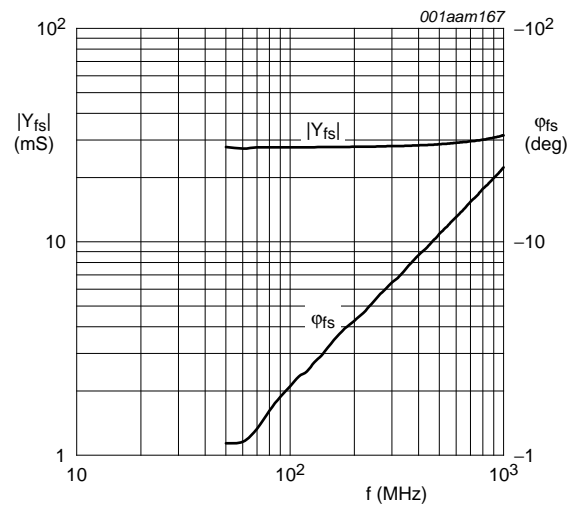
$V_{DS} = 5\text{ V}$ ;  $V_{GG} = 5\text{ V}$ ;  $V_{G2-S(nom)} = 4\text{ V}$ ;  $R_{G1} = 82\text{ k}\Omega$ ;  $f_w = 50\text{ MHz}$ ;  $I_{D(nom)} = 19\text{ mA}$ ;  $T_j = 25\text{ }^\circ\text{C}$ ; see [Figure 17](#).

**Fig 12. Typical drain current as a function of gain reduction; typical values**



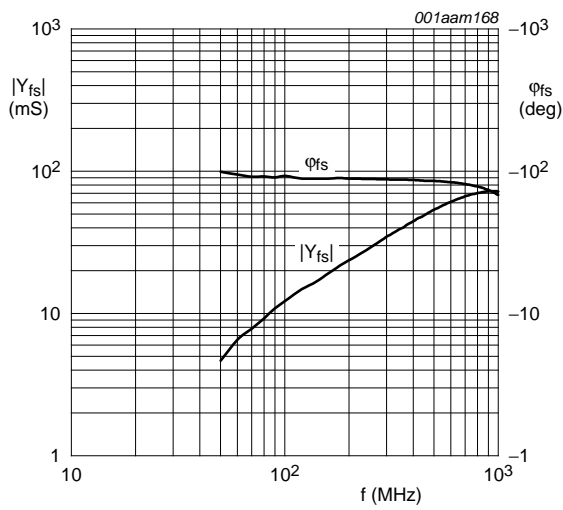
$V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 19\text{ mA}$ .

**Fig 13. Input admittance as a function of frequency; typical values**



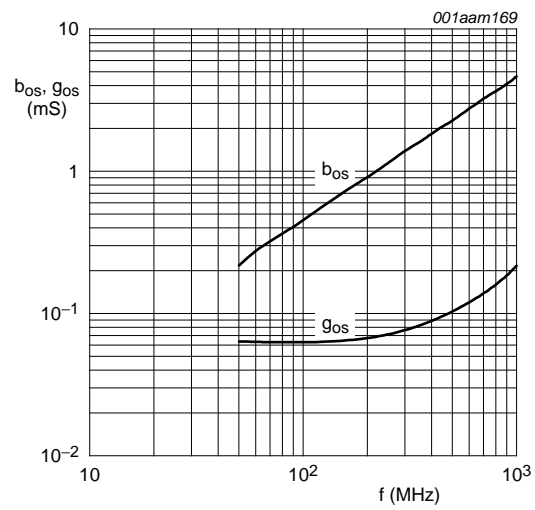
$V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 19\text{ mA}$ .

**Fig 14. Forward transfer admittance and phase as a function of frequency; typical values**



$V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 19\text{ mA}$ .

**Fig 15. Reverse transfer admittance and phase as a function of frequency; typical values**



$V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 19\text{ mA}$ .

**Fig 16. Output admittance as a function of frequency; typical values**

## 8.2 Scattering parameters

**Table 9. Scattering parameters**

$V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 19\text{ mA}$ ;  $T_{amb} = 25\text{ °C}$ ;  $Z_0 = 50\text{ }\Omega$ ; typical values.

f (MHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)
40	0.9960	-3.50	2.77	177.20	0.00034	82.80	0.9945	-1.00
50	0.9957	-4.46	2.76	176.02	0.00046	82.50	0.9944	-1.28
100	0.9935	-8.66	2.74	172.19	0.00121	81.86	0.9938	-2.69
200	0.9880	-17.55	2.73	164.42	0.00231	80.28	0.9927	-5.39
300	0.9805	-26.17	2.69	156.64	0.00331	75.66	0.9909	-8.17
400	0.9712	-34.58	2.64	149.07	0.00414	71.21	0.9896	-10.79
500	0.9589	-42.78	2.58	141.74	0.00482	67.42	0.9872	-13.30
600	0.9451	-50.61	2.52	134.58	0.00526	64.33	0.9850	-16.08
700	0.9309	-58.23	2.45	127.49	0.00549	61.90	0.9836	-18.74
800	0.9166	-65.68	2.37	120.79	0.00551	60.77	0.9818	-21.05
900	0.9034	-72.70	2.29	114.37	0.00536	60.73	0.9796	-23.59
1000	0.8894	-79.30	2.22	107.90	0.00505	62.45	0.9781	-26.44

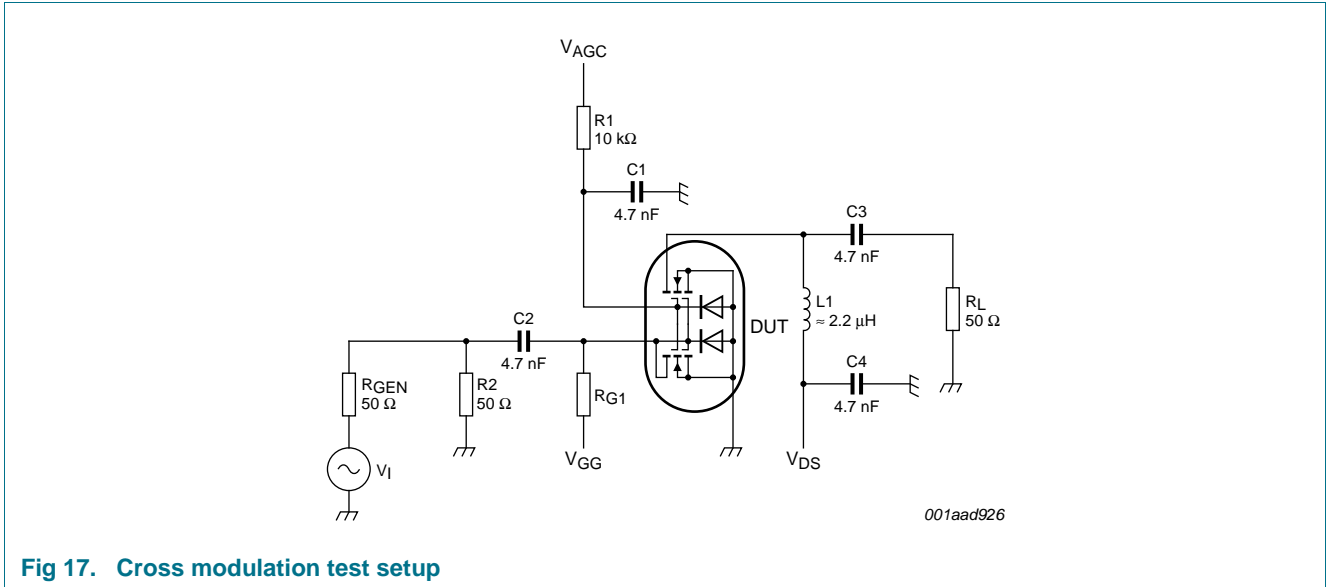
## 8.3 Noise data

**Table 10. Noise data**

$V_{DS} = 5\text{ V}$ ;  $V_{G2-S} = 4\text{ V}$ ;  $I_D = 19\text{ mA}$ ;  $T_{amb} = 25\text{ °C}$ ; typical values.

f (MHz)	NF <sub>min</sub> (dB)	$\Gamma_{opt}$		r <sub>n</sub> (ratio)
		(ratio)	(deg)	
400	1.0	0.798	29.5	0.907
800	1.5	0.703	57.7	0.749

**9. Test information**



**Fig 17. Cross modulation test setup**

**10. Package outline**

Plastic surface-mounted package; reverse pinning; 4 leads

SOT343R

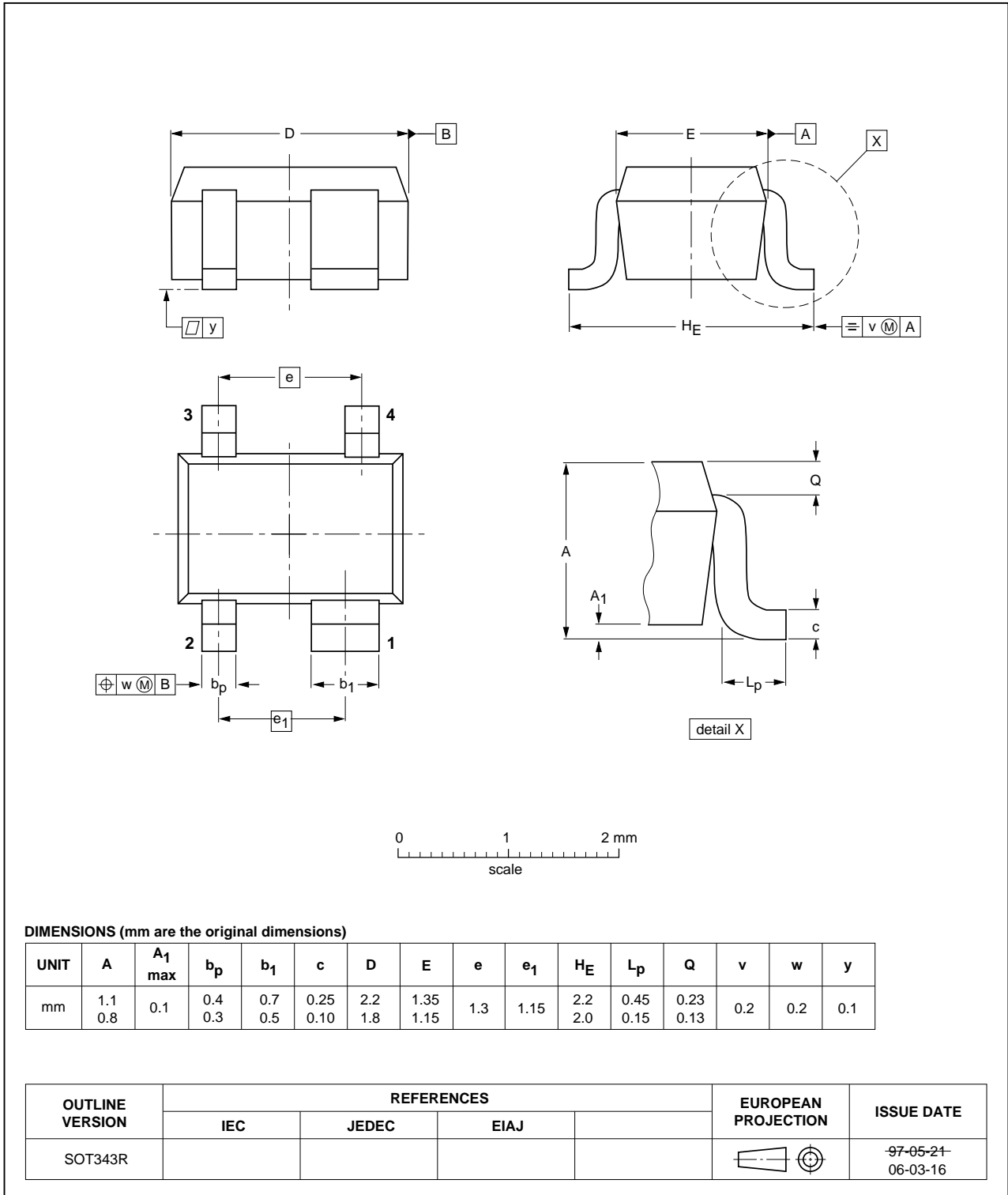


Fig 18. Package outline SOT343

## 11. Abbreviations

Table 11. Abbreviations

Acronym	Description
AGC	Automatic Gain Control
DC	Direct Current
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
UHF	Ultra High Frequency
VHF	Very High Frequency

## 12. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BF1217WR v.2	20110620	Product data sheet	-	BF1217WR v.1
Modifications:	• Package outline corrected.			
BF1217WR v.1	20100803	Product data sheet	-	-

## 13. Legal information

### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 13.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 13.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any

liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Quick reference data** — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

## 13.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 14. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)



## 15. Contents

<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features and benefits . . . . .	1
1.3	Applications . . . . .	1
1.4	Quick reference data . . . . .	2
<b>2</b>	<b>Pinning information</b> . . . . .	<b>2</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
<b>4</b>	<b>Marking</b> . . . . .	<b>3</b>
<b>5</b>	<b>Limiting values</b> . . . . .	<b>3</b>
<b>6</b>	<b>Thermal characteristics</b> . . . . .	<b>4</b>
<b>7</b>	<b>Static characteristics</b> . . . . .	<b>4</b>
<b>8</b>	<b>Dynamic characteristics</b> . . . . .	<b>5</b>
8.1	Graphs . . . . .	6
8.2	Scattering parameters . . . . .	11
8.3	Noise data . . . . .	11
<b>9</b>	<b>Test information</b> . . . . .	<b>12</b>
<b>10</b>	<b>Package outline</b> . . . . .	<b>13</b>
<b>11</b>	<b>Abbreviations</b> . . . . .	<b>14</b>
<b>12</b>	<b>Revision history</b> . . . . .	<b>14</b>
<b>13</b>	<b>Legal information</b> . . . . .	<b>15</b>
13.1	Data sheet status . . . . .	15
13.2	Definitions . . . . .	15
13.3	Disclaimers . . . . .	15
13.4	Trademarks . . . . .	16
<b>14</b>	<b>Contact information</b> . . . . .	<b>16</b>
<b>15</b>	<b>Contents</b> . . . . .	<b>17</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 20 June 2011

Document identifier: BF1217WR