SAM E70/S70/V70/V71 Family

SAM E70/S70/V70/V71 Family Silicon Errata and Data Sheet Clarification

SAM E70/S70/V70/V71 Family

The SAM E70/S70/V70/V71 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001527A), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following tables. The silicon issues are summarized in Silicon Issue Summary.

The errata described in this document will be addressed in future revisions of the SAM E70/S70/V70/V71 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in Data Sheet Clarifications, following the discussion of silicon issues.

The Device and Revision ID values for the various SAM E70/S70/V70/V71 family silicon revisions are shown in the following tables.

Table 1. SAM V71 Silicon Device Identification

Part Number	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHPID_CIDR[31:0]	CHIPID_EXID[31:0]	A	B
SAMV71Q19	0xA12D_0A0x	0x00000002	0x0	0x1
SAMV71Q20	0xA122_0C0x	0x00000002		
SAMV71Q21	0xA122_0E0x	0x00000002		
SAMV71N19	0xA12D_0A0x	0x00000001		
SAMV71N20	0xA122_0C0x	0x00000001		
SAMV71N21	0xA122_0E0x	0x00000001		
SAMV71J19	0xA12D_0A0x	0x00000000		
SAMV71J20	0xA122_0C0x	0x00000000		
SAMV71J21	0xA122_0E0x	0x00000000		

Table 2. SAM V70 Silicon Device Identification

Part Number	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHPID_CIDR[31:0]	CHIPID_EXID[31:0]	A	B
SAMV70Q19	0xA13D_0A0x	0x00000002	0x0	0x1
SAMV70Q20	0xA132_0C0x	0x00000002		
SAMV70N19	0xA13D_0A0x	0x00000001		
SAMV70N20	0xA132_0C0x	0x00000001		
SAMV70J19	0xA13D_0A0x	0x00000000		
SAMV70J20	0xA132_0C0x	0x00000000		

Table 3. SAM S70 Silicon Device Identification

Part Number	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHPID_CIDR[31:0]	CHIPID_EXID[31:0]	A	B
SAMS70Q19	0xA11D_0A0x	0x00000002	0x0	N/A
SAMS70Q20	0xA112_0C0x	0x00000002		
SAMS70Q21	0xA112_0E0x	0x00000002		
SAMS70N19	0xA11D_0A0x	0x00000001		
SAMS70N20	0xA112_0C0x	0x00000001		
SAMS70N21	0xA112_0E0x	0x00000001		
SAMS70J19	0xA11D_0A0x	0x00000000		
SAMS70J20	0xA112_0C0x	0x00000000		
SAMS70J21	0xA112_0E0x	0x00000000		

Table 4. SAM E70 Silicon Device Identification

Part Number	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHPID_CIDR[31:0]	CHIPID_EXID[31:0]	A	B
SAME70Q19	0xA10D_0A0x	0x00000002	0x0	N/A
SAME70Q20	0xA102_0C0x	0x00000002		
SAME70Q21	0xA102_0E0x	0x00000002		
SAME70N19	0xA10D_0A0x	0x00000001		
SAME70N20	0xA102_0C0x	0x00000001		
SAME70N21	0xA102_0E0x	0x00000001		

Part Number	Device Identification		Revision (CHIPID_CIDR.VERSION[4:0])	
	CHPID_CIDR[31:0]	CHIPID_EXID[31:0]	A	B
SAME70J19	0xA10D_0A0x	0x00000000		
SAME70J20	0xA102_0C0x	0x00000000		
SAME70J21	0xA102_0E0x	0x00000000		

Note:

1. Refer to the “Chip Identifier (CHIPID)” section in the current Device Data Sheet (DS60001527A) for detailed information on Chip Identification and Revision IDs for your specific device.

1. Silicon Issue Summary

Table 1-1. Silicon Issue Summary

Module	Item and Feature	Summary	Affected Silicon Revisions	
			A	B
AFEC	Write Protection	The AFEC_CSELR register is not write-protected.	X	X
AFEC	Performance	The AFEC is sensitive to noise. Too much noise may lead to reduced AFEC performance, especially INL, DNL and SNR.	X	X
AFEC	AOFF bit	Changing the AOFF bit in the AFEC_COCR register during conversions is not safe.	X	X
ARM Cortex-M7	ARM® Cortex®-M7	All issues related to the ARM r0p1 (for MRLA) and r1p1 (and MRLB) cores are described on the ARM site.	X	X
Boundary Scan Mode	Internal Regulator	The internal regulator is OFF in Boundary Scan mode.	X	
Device	AHB Peripheral (AHBP) Port Frequency Ratio	Peripheral accesses done through the AHBP with a Core/Bus ratio of 1/3 and 1/4 may lead to unpredictable results.	X	X
Device	AHB Slave (AHBS) Port Latency Access	DMA accesses done through the AHBS to the TCM with a Core/Bus ratio of 1/2, 1/3, and 1/4 may lead to latency due to one Wait state added to the access from the bus to AHBS.	X	
XDMAC	TCM Accesses	If TCM accesses are generated through the AHBS port of the core, only 32-bit accesses are supported.	X	X
XDMAC	Byte and Half-Word Accesses	If XDMAC is used to transfer 8-bit or 16-bit data in Fixed Source Address mode or Fixed Destination Address mode, source and destination addresses are incremented by 8-bit or 16-bit.	X	X
XDMAC	Request Overflow Error	When a DMA memory-to-memory transfer is performed, if the hardware request line selected by the field PERID bit in the XDMAC_CCx register toggles when the copy is enabled, the ROIS bit in the XDMAC_CISx register is set incorrectly.	X	X

Module	Item and Feature	Summary	Affected Silicon Revisions	
			A	B
FFPI	Flash Programming	The FFPI programs only 1 MB of Flash memory.	X	
GMAC	Priority Queues	On Revision A silicon, only three priority queues are available.	X	
I2SC	Module Availability	The Inter-IC Sound Controller (I2SC) is not available.	X	
I2SC	Corrupted First Sent Data	Immediately after the I2SC module is reset, the first data sent by the controller on the I2SDO line is corrupted.		X
MCAN	Non-ISO Operation	The default frame format on Revision A silicon does not match the default format specified in the current device data sheet.	X	
MCAN	MCAN_CCCR Register	In Revision A silicon, the MCAN CC Control register content does not match the content of the current device data sheet.	X	
MCAN	Transmitter Delay Compensation Value (TDCV) Bits	In Revision A silicon, the Transmitter Delay Compensation Value (TDCV) bit field does not match the content in the current device data sheet.	X	
MCAN	MCAN_PSR Register	In Revision A silicon, the content of the MCAN Protocol Status register differs from the content in the current device data sheet.	X	
MCAN	MCAN_IR Register	In Revision A silicon, the content of the MCAN Interrupt register differs from the content in the current device data sheet.	X	
MCAN	MCAN_IE Register	On Revision A silicon, the content in the MCAN Interrupt Enable register does not match the content in the current device data sheet.	X	
MCAN	MCAN_ILS Register	On Revision A silicon, the content in the MCAN Interrupt Line Support Register does not match the content in the current device data sheet.	X	
MCAN	MCAN Data Bit Timing and Prescaler Register	On Revision A silicon, the MCAN Data Bit Timing and Prescaler register (MCAN_DBTP) is named MCAN Fast	X	

Module	Item and Feature	Summary	Affected Silicon Revisions	
			A	B
		Bit Timing and Prescaler register (MCAN_FBTP).		
MCAN	MCAN Nominal Bit Timing and Prescaler Register	On Revision A silicon, the MCAN Nominal Bit Timing and Prescaler register (MCAN_NBTP) is named MCAN Bit Timing and Prescaler register (MCAN_BTP).	X	
MCAN	MCAN Transmitter Delay Compensation Register	In Revision A silicon, the MCAN Transmitter Delay Compensation Register (MCAN_TDCR) does not exist.	X	
MCAN	Timestamping Function	On Revision A silicon, TC Counter 0 is not connected to PCK6 and PCK7; therefore, the timestamping functionality does not exist.	X	
PIO	PIO Line Configuration for AFEC and DACC Analog Inputs	To enable the analog inputs, AFE_ADx or DACx, the pull-up resistors on the I/O lines must be disabled in the PIO user interface prior to writing registers AFEC_CHER or DACC_CHER.	X	X
PMC	Wait Mode Exit Fail from Flash	The delay to exit from Wait mode is too short to respect the Flash wake-up time from Stand-by mode and Deep Power-down mode. This delay may lead to bad opcode fetching.	X	X
PMC	PMC_OCR Register Calibration Reporting	When reading the PMC_OCR register with the SEL8 and SEL12 bits cleared, the CAL8 and CAL12 bits are not updated with the manufacturing calibration bits of the Main RC Oscillator. However, the Main RC Oscillator is loaded with this manufacturing calibration data.	X	X
QSPI	Module Hangs with Long DLYCS	The QSPI module hangs if a command is written to any QSPI register during the delay defined in the DLYCS bit. There is no status bit to flag the end of the delay.	X	X
RTC	RTC_CALR Reset Value	On Revision A silicon, the reset value of the RTC_CALR register is 0x01E11220.	X	

Module	Item and Feature	Summary	Affected Silicon Revisions	
			A	B
SDRAMC	SDRAM Controller Scrambling Use Limitation	The scrambling/unscrambling feature of the SDRAM Controller (SDRAMC) has a use limitation.	X	X
SDRAMC	USB and SDRAM Concurrent Access Issue	USB module functionality is adversely affected with concurrent SDRAM access.	X	X
SMC	SMC_WPSR Register Write Protection	When the write protection feature is enabled and a write attempt into a protected register is performed, the Write Protection Violation Source (WPVSRC) bit field in the SMC_WPSR register does not report the right violation source.		X
SSC	Inverted Left/Right Channels	When the SSC is in Slave mode, the TF signal is derived from the codec and not controlled by the SSC.	X	
SSC	Unexpected TD Output Delay	An unexpected delay on TD output may occur when the SSC is configured under certain conditions.	X	X
SUPC	Write-Protection	The SUPC_WUIR register is not write-protected.	X	X
TWIHS	I2C Hold Timing Incompatibility	The TWIHS module is not compatible with I^2C hold timing.	X	X
TWIHS	Clear Command	A bus reset using the CLEAR bit of the TWIHS Control register does not work correctly during a bus busy state.	X	X
USART	Flow Control with DMA	The RTS signal is not connected to the DMA. Therefore, when DMA is used, Flow Control is not supported.	X	X
USART	Bad Frame Detection	If a bad frame is received (i.e., incorrect baud rate) with the last data bit being sampled at 1, frame error detection does not occur.	X	X
USBHS	USBHS Host Does Not Function in Low-Speed Mode	The USB Host does not function in Low-Speed mode.	X	

Module	Item and Feature	Summary	Affected Silicon Revisions	
			A	B
USBHS	64-pin LQFP Package	The USBHS module does not function in 64-pin LQFP package devices.	X	X
USBHS	NO DMA for Endpoint 7	The DMA feature is not available for Pipe/Endpoint 7.	X	X

2. Analog Front-End Controller (AFEC)

2.1 Write Protection

The AFEC_CSELR register is not write-protected.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

2.2 Performance

The AFEC is sensitive to noise. Too much noise may lead to reduced AFEC performance, especially INL, DNL and SNR. The following situations generate noise:

- Using a 64-pin QFP package option (it does not have the VREFN pin)
- Device activity (that is, clock tree)
- External components (that is, missing on-board supply decoupling capacitors)

Workaround

Adapt the environment to the expected level of performances.

Affected Silicon Revisions

A	B						
X	X						

2.3 AOFF bit

Changing the AOFF bit in the AFEC_COCR register during conversions is not safe.

The recommended value of the AOFF bit is 512 (the default value is zero). Different values are possible for each channel. The AOFF bit is read and updated during the AFE start-up sequence and at the end of each conversion. If during AFE idle time (no conversion is on-going) the user updates the AOFF bit for the next channel to be converted, the next conversion will be incorrect.

Workaround

The value of the AOFF bit can be updated only if the AFEC module is restarted, or if two conversions are run; the second one will have the correct AOFF bit setting.

Affected Silicon Revisions

A	B						
X	X						

3. ARM Cortex-M7

3.1 ARM® Cortex®-M7

All issues related to the ARM r0p1 (for MRLA) and r1p1 (and MRLB) cores are described on the ARM website.

Workaround

Refer to the following ARM documentation:

- For ARM Cortex-M7 r0p1 core (MRLA device): https://silver.arm.com/download/download.tm?pv=2004343
- For ARM Cortex-M7 r1p1 core (MRLB device): https://silver.arm.com/download/download.tm?pv=3257391&p=1929427
- ARM Embedded Trace Macrocell CoreSight ETM–M7 (TM975) Software Developers Errata Notice: https://silver.arm.com/download/download.tm?pv=1998309

Affected Silicon Revisions

A	B						
X	X						

4. Boundary Scan Mode

4.1 Internal Regulator

The internal regulator is OFF in Boundary Scan mode.

Workaround

The user must provide external VDDCORE (1.2V) to perform Boundary Scan mode.

Affected Silicon Revisions

A	B						
X							

5. Device

5.1 AHB Peripheral (AHBP) Port Frequency Ratio

Peripheral accesses done through the AHBP with a Core/Bus ratio of 1/3 and 1/4 may lead to unpredictable results.

Workaround

The user must use a Core/Bus frequency ratio of 1 or 1/2.

Affected Silicon Revisions

A	B						
X	X						

5.2 AHB Slave (AHBS) Port Latency Access

DMA accesses done through the AHBS to the TCM with a Core/Bus ratio of 1/2, 1/3, and 1/4 may lead to latency due to one Wait state added to the access from the bus to AHBS.

Workaround

The user must use only the Core/Bus frequency ratio of 1 to guarantee the length of the access.

Affected Silicon Revisions

A	B						
X							

6. Extended DMA Controller (XDMAC)

6.1 TCM Accesses

If TCM accesses are generated through the AHBS port of the core, only 32-bit accesses are supported. Accesses that are not 32-bit aligned may overwrite bytes at the beginning and at the end of 32-bit words.

Workaround

The user application must use 32-bit aligned buffers and buffers with a size of a multiple of 4 bytes when transferring data to or from the TCM through the AHBS port of the core.

Affected Silicon Revisions

A	B						
X	X						

6.2 Byte and Half-Word Accesses

If XDMAC is used to transfer 8-bit or 16-bit data in Fixed Source Address mode or Fixed Destination Address mode, source and destination addresses are incremented by 8-bit or 16-bit.

Workaround

The user can resolve this issue by setting the source addressing mode to use microblock and data striding with microblock stride set to 0 and data stride set to -1.

Affected Silicon Revisions

A	B						
X	X						

6.3 Request Overflow Error

When a DMA memory-to-memory transfer is performed, if the hardware request line selected by the field PERID bit in the XDMAC_CCx register toggles when the copy is enabled, the ROIS bit in the XDMAC_CISx register is set incorrectly. The memory transfer proceeds normally and the data area is correctly transferred.

Workaround

Configure the PERID bit to an unused peripheral ID.

Affected Silicon Revisions

A	B						
X	X						

7. Fast Flash Programming Interface (FFPI)

7.1 Flash Programming

The FFPI programs only 1 MB of Flash memory.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

8. Ethernet MAC (GMAC)

8.1 Priority Queues

On Revision A silicon, only three priority queues are available with the following sizes:

Queue Number	Queue Size
2 (highest priority)	4 KB
1	2 KB
0 (lowest priority)	2 KB

Workaround

None.

Affected Silicon Revisions

A	B						
X							

9. Inter-IC Sound Controller (I2SC)

9.1 Module Availability

The Inter-IC Sound Controller (I2SC) is not available.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

9.2 Corrupted First Sent Data

Immediately after the I2SC module is reset, the first data sent by the controller on the I2SDO line is corrupted. Any data that follows is not affected.

Workaround

None.

Affected Silicon Revisions

A	B						
	X						

10. Controller Area Network (MCAN)

10.1 Non-ISO Operation

The default frame format on Revision A silicon does not match the default format specified in the current device data sheet.

Workaround

To retain Revision A behavior, set the MCAN_CCCR.NISO bit to '1'.

Affected Silicon Revisions

A	B						
X							

10.2 MCAN_CCCR Register

In Revision A silicon, the MCAN CC Control register content does not match the content of the current device data sheet.

- NISO bit is missing
- EFBI bit is named FDBS
- PXHD bit is named FDO
- BRSE bit and FDOE bit are named CME[1:0]
- CMR[1:0] bits are present

Workaround

None.

Affected Silicon Revisions

A	B						
X							

10.3 Transmitter Delay Compensation Value (TDCV) Bits

In Revision A silicon, the Transmitter Delay Compensation Value (TDCV) bit field does not match the content in the current device data sheet.

In Revision A silicon, the TDCV bits are located in the MCAN_TEST register.

In the current device data sheet, the TDCV bits are located in the MCAN_PSR register.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

10.4 MCAN_PSR Register

In Revision A silicon, the content of the MCAN Protocol Status register differs from the content in the current device data sheet.

- PXE bit is not available
- RFDF bit is named REDL
- DLEC[2:0] bits are named FLEC[2:0]

Workaround
None.

Affected Silicon Revisions

A	B						
X							

10.5 MCAN_IR Register

In Revision A silicon, the content of the MCAN Interrupt register differs from the content in the current device data sheet.

- STE and FOE bits are present
- ARA bit is replaced by the ACKE bit
- PED bit is replaced by the BE bit
- PEA bit is replaced by the CRCE bit

Workaround
None.

Affected Silicon Revisions

A	B						
X							

10.6 MCAN_IE Register

On Revision A silicon, the content in the MCAN Interrupt Enable register does not match the content in the current device data sheet.

- STEE and FOEE bits are present
- ARAE bit is replaced by the ACKEE bit

- PEDE bit is replaced by the BEE bit
- PEAE bit is replaced by the CRCEE bit

Workaround
None.

Affected Silicon Revisions

A	B						
X							

10.7 MCAN_ILS Register

On Revision A silicon, the content in the MCAN Interrupt Line Support Register does not match the content in the current device data sheet.

- STEL and FOEL bits are present
- ARAL bit is replaced by the ACKEL bit
- PEDL bit is replaced by the BEL bit
- PEAL bit is replaced by the CRCEL bit

Workaround
None.

Affected Silicon Revisions

A	B						
X							

10.8 MCAN Data Bit Timing and Prescaler Register

On Revision A silicon, the MCAN Data Bit Timing and Prescaler register (MCAN_DBTP) is named MCAN Fast Bit Timing and Prescaler register (MCAN_FBTP).

Workaround
When using Revision A silicon, ensure that the name MCAN_FBTP is used.

Affected Silicon Revisions

A	B						
X							

10.9 MCAN Nominal Bit Timing and Prescaler Register

On Revision A silicon, the MCAN Nominal Bit Timing and Prescaler register (MCAN_NBTP) is named MCAN Bit Timing and Prescaler register (MCAN_BTP).

Workaround
When using Revision A silicon, ensure that the name MCAN_BTP is used.

Affected Silicon Revisions

A	B						
X							

10.10 MCAN Transmitter Delay Compensation Register

In Revision A silicon, the MCAN Transmitter Delay Compensation Register (MCAN_TDCR) does not exist.

Workaround
The transmit delay compensation offset is configured in the TDCO field of the MCAN_FBTP register.

Affected Silicon Revisions

A	B						
X							

10.11 Timestamping Function

On Revision A silicon, TC Counter 0 is not connected to PCK6 and PCK7; therefore, the timestamping functionality does not exist.

Workaround
None.

Affected Silicon Revisions

A	B						
X							

11. Parallel Input/Output (PIO)

11.1 PIO Line Configuration for AFEC and DACC Analog Inputs

To enable the analog inputs, AFE_ADx or DACx, the pull-up resistors on the I/O lines must be disabled in the PIO user interface prior to writing registers AFEC_CHER or DACC_CHER.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

12. Power Management Controller (PMC)

12.1 Wait Mode Exit Fail from Flash

The delay to exit from Wait mode is too short to respect the Flash wake-up time from Stand-by mode and Deep Power-down mode. This delay may lead to bad opcode fetching.

Workaround 1

If Flash in Stand-by mode (FLPM = 0) or in Deep Power-down mode (FLPM = 1) is used, run the wake-up routine from SRAM. This option provides a slight improvement in power consumption.

Workaround 2

If Flash in Stand-by mode (FLPM = 0) or in Deep Power-down mode (FLPM = 1) is used, run the wake-up routine from SRAM. This option provides a slight improvement in power consumption.

Affected Silicon Revisions

A	B						
X	X						

12.2 PMC_OCR Register Calibration Reporting

When reading the PMC_OCR register with the SEL8 and SEL12 bits cleared, the CAL8 and CAL12 bits are not updated with the manufacturing calibration bits of the Main RC Oscillator. However, the Main RC Oscillator is loaded with this manufacturing calibration data.

Workaround

To recover the manufacturing calibration bits of the Main RC oscillator, use the following steps:

1. Execute the ‘Get CALIB Bit’ command by writing the FCMD bit in the EEFC_FCR register with the GCALB command.
2. Read the EEFC_FRR register. The 8 MHz RC calibration bits are EEFC_FRR bits [17-11] and the the 12 MHz RC calibration bits are EEFC_FRR bits [25-19].

Affected Silicon Revisions

A	B						
X	X						

13. Quad Serial Peripheral Interface (QSPI)

13.1 Module Hangs with Long DLYCS

The QSPI module hangs if a command is written to any QSPI register during the delay defined in the DLYCS bit. There is no status bit to flag the end of the delay.

Workaround

The DLYCS bit defines a minimum period over which the Chip Select is deasserted, which is required by some memories. This delay is generally less than 60 ns and comprises internal execution time, arbitration, and latencies. Therefore, the DLYCS bit must be configured to be slightly higher than the value specified for the slave device. The software must wait for at least this same period of time before a command can be written to the QSPI module.

Affected Silicon Revisions

A	B						
X	X						

14. Real-Time Clock (RTC)

14.1 RTC_CALR Reset Value

On Revision A silicon, the reset value of the RTC_CALR register is 0x01E11220.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

15. SDRAM Controller (SDRAMC)

15.1 SDRAM Controller Scrambling Use Limitation

The scrambling/unscrambling feature of the SDRAM Controller (SDRAMC) has a use limitation.

Workaround

The read of a scrambled area must be performed with the same type of access done during the write of this area. As an example, it is recommended to write using 32-bit words and read 32-bit words.

Affected Silicon Revisions

A	B						
X	X						

15.2 USB and SDRAM Concurrent Access Issue

USB module functionality is adversely affected with concurrent SDRAM access.

Workaround

Ensure that no concurrent module operations when using both SDRAM and USB.

Affected Silicon Revisions

A	B						
X	X						

16. Static Memory Controller (SMC)

16.1 SMC_WPSR Register Write Protection

When the write protection feature is enabled and a write attempt into a protected register is performed, the Write Protection Violation Source (WPVSRC) bit field in the SMC_WPSR register does not report the right violation source. As a consequence, the value in the WPVSRC bit field is incorrect. This issue does not affect the write protection feature itself, which is fully functional.

Workaround

None.

Affected Silicon Revisions

A	B						
	X						

17. Serial Synchronous Controller (SSC)

17.1 Inverted Left/Right Channels

When the SSC is in Slave mode, the TF signal is derived from the codec and not controlled by the SSC. The SSC transmits the data when detecting the falling edge on the TF signal after the SSC transmission is enabled. In some cases of overflow, a left/right channel inversion may occur. When this occurs, the SSC must be reinitialized.

Workaround

Using the SSC in Master mode will ensure that TF is controlled by the SSC and no error occurs. If the SSC must be used in TF Slave mode, the SSC must be started by writing TXEN and RXEN synchronously with the TXSYN flag rising in the SSC_SR.

Affected Silicon Revisions

A	B						
X							

17.2 Unexpected TD Output Delay

An unexpected delay on TD output may occur when the SSC is configured with the following conditions:

- The START bit in the RCMR register = Start on falling edge/Start on Rising edge/Start on any edge
- The FSOS bit in the RFMR register = None (input)
- The START bit in the TCMR register = Receive Start

Under these conditions, an unexpected delay of two or three system clock cycles is added to the TD output.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

18. Supply Controller (SUPC)

18.1 Write-Protection

The SUPC_WUIR register is not write-protected.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

19. TWI High-Speed (TWIHS)

19.1 I²C Hold Timing Incompatibility

The TWIHS module is not compatible with I²C hold timing. The divider to program the hold time is too short to achieve the expected hold time at high frequency. The achieved time is 227 ns maximum at 150 MHz, instead of the required 300 ns.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

19.2 Clear Command

A bus reset using the CLEAR bit of the TWIHS Control register does not work correctly during a bus busy state.

Workaround

Reconfigure the TWCK line in GPIO output and generate nine clock pulses through software to unlock the I²C device.
Once this is done, the TWCK line can be reconfigured as a peripheral line.

Affected Silicon Revisions

A	B						
X	X						

20. Universal Synchronous Asynchronous Receiver Transmitter (USART)

20.1 Flow Control with DMA

The RTS signal is not connected to the DMA. Therefore, when DMA is used, Flow Control is not supported.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

20.2 Bad Frame Detection

If a bad frame is received (i.e., incorrect baud rate) with the last data bit being sampled at 1, frame error detection does not occur.

Workaround

There is no general workaround. When performing baud rate detection with receive part, the transmit frame must be sent with a parity bit set to '0'.

Affected Silicon Revisions

A	B						
X	X						

21. USB High-Speed (USBHS)

21.1 USBHS Host Does Not Function in Low-Speed Mode

The USB Host does not function in Low-Speed mode.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

21.2 64-pin LQFP Package

The USBHS module does not function in 64-pin LQFP package devices.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

21.3 NO DMA for Endpoint 7

The DMA feature is not available for Pipe/Endpoint 7.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

22. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001527A):

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

No clarifications to report at this time.

23. Appendix A: Revision History

Rev A Document (11/2017)
Initial release of this document.

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