GDDR5X SGRAM

MT58K256M321JA-100/-110/-120:A

16 Meg x 32 I/O x 16 banks, 32 Meg x 16 I/O x 16 banks

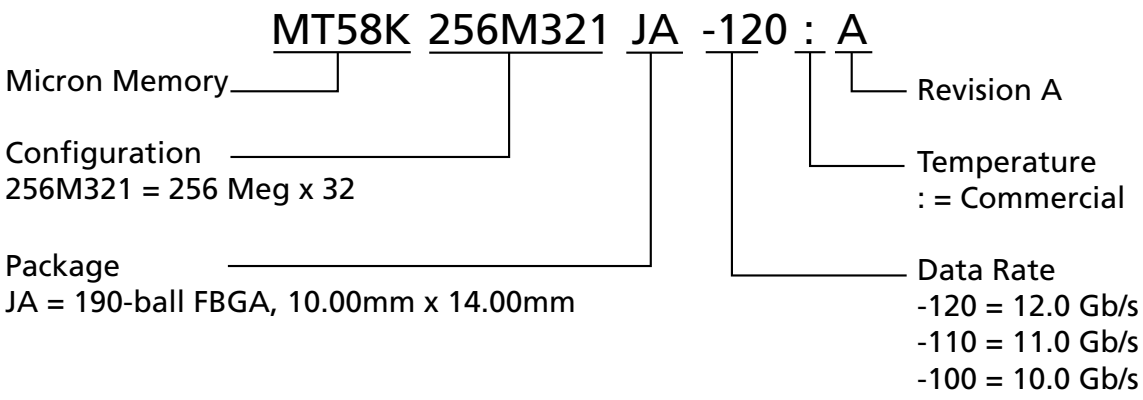
Features

- $V_{DD} = V_{DDQ}$ = 1.35V ±3%
- V_{PP} = 1.8V -3%/+6%
- Data rate: 12.0 Gb/s, 11.0 Gb/s, 10.0 Gb/s
- Single ended interface for command, address and data
- Differential clock input CK_t/CK_c for ADD/CMD
- Two differential clock inputs WCK_t/WCK_c, each associated with two data bytes (DQ, DBI_n, EDC)
- Single data rate (SDR) commands (CK)
- Double data rate (DDR) addresses (CK)
- QDR and DDR operating modes:
  - QDR mode: Quad data rate (QDR) data (WCK); 16n prefetch architecture with 512bit per array read or write access; burst length 16
  - DDR mode: Double data rate (DDR) data (WCK); 8n prefetch architecture with 256bit per array read or write access; burst length 8
- 16 internal banks
- 4 bank groups for ^{t}CCDL = 3 ^{t}CK and 4 ^{t}CK
- Programmable READ latency: 9 to 20
- Programmable WRITE latency: 5 to 7
- Write data mask function via address bus (single/double/quad byte mask)
- Data bus inversion (DBI) and address bus inversion (ABI)
- Input/output PLL
- Address training: Address input monitoring via DQ/DBI_n/EDC pins
- WCK2CK clock training with phase information via EDC pins
- Data read and write training via read FIFO (depth = 6)
- Read FIFO pattern preload by LDFF command
- Write data load to read FIFO via WRTR command
- Consecutive read of read FIFO via RDTR command
- Read/write EDC on/off mode
- Programmable EDC hold pattern for CDR
- Read/write data transmission integrity secured by cyclic redundancy check (CRC-8)
- Programmable CRC READ latency = 2 to 3
- Programmable CRC WRITE latency = 9 to 14
- Low power modes
- RDQS mode on EDC pins
- On-chip temperature sensor with read-out
- Auto precharge option for each burst access
- Auto refresh mode with per-bank refresh option
- Temperature sensor controlled self refresh rate
- Digital ^{t}RAS lockout
- On-die termination (ODT) for all high-speed inputs
- Pseudo open drain (POD-135) compatible outputs
- ODT and output driver strength auto-calibration with external resistor ZQ pin (120 Ω)
- Programmable termination and driver strength offsets
- Internal V_{REF} for data inputs
- Selectable external or internal V_{REF} for ADD/CMD inputs
- Data input receiver characteristics programmable per byte
- Vendor ID for device identification
- Mirror function with MF pin
- IEEE 1149.1 compliant boundary scan
- 190 ball BGA package
- Lead-free (RoHS-compliant) and halogen-free packaging
- T_C = 0°C to +95°C

Options[1]	Marking
• Organization	
– 256 Meg x 32 (words x bits)	256M321
• FBGA package	
– 190-ball (10mm x 14mm)	JA
• Timing – maximum data rate	
– 12.0 Gb/s	-120
– 11.0 Gb/s	-110
– 10.0 Gb/s	-100
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ +95°C)	None
• Revision	A

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Figure 1: Part Numbering



FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's web site: http://www.micron.com.

Operating Frequency Ranges

Figure 2: Data Rates in QDR, DDR, and RDQS Modes

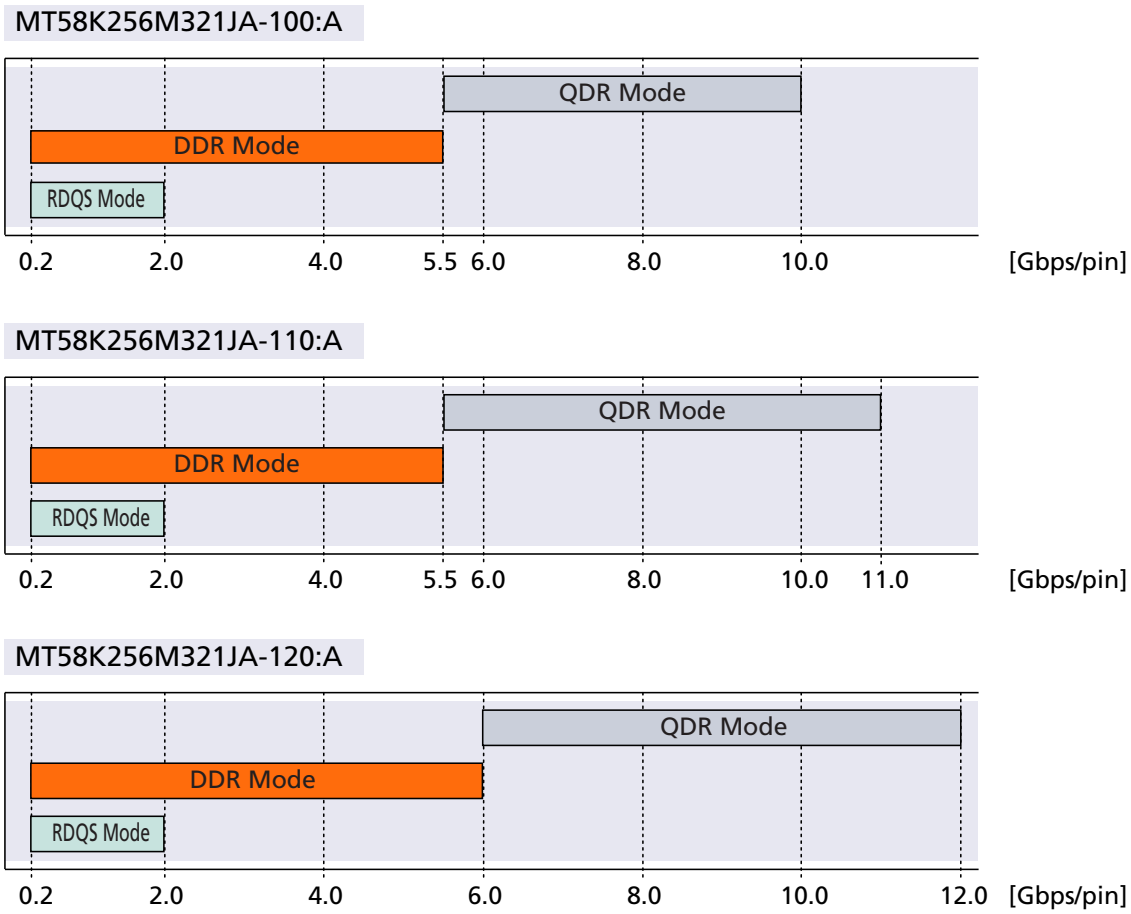


Table 1: Operating Frequency Ranges

Operating Mode	Symbol	-100		-110		-120		Unit
		Min	Max	Min	Max	Min	Max	
QDR mode	^{f}CK	687	1250	687	1375	750	1500	MHz
DDR mode		50	1375	50	1375	50	1500	
RDQS mode		50	500	50	500	50	500	

Note: The operating range and AC timings of a faster speed bin are a superset of all slower speed bins. Therefore it is safe to use a faster bin device as a drop-in replacement of a slower bin device when operated within the frequency range of the slower bin device.

Ball Assignments and Descriptions

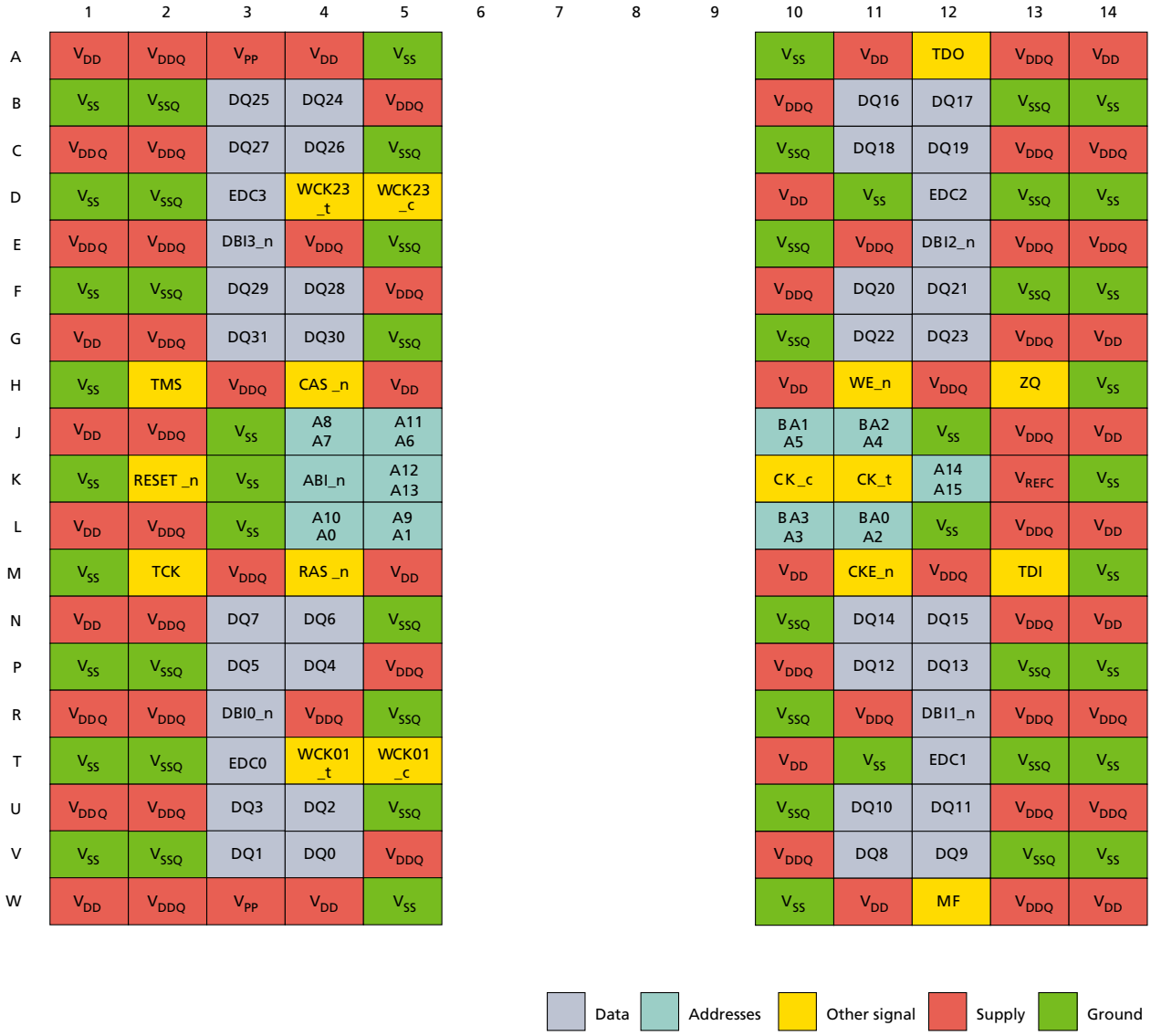
Figure 3: 190-Ball FBGA – MF = 0 (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	V_{DD}	V_{DDQ}	V_{PP}	V_{DD}	V_{SS}					V_{SS}	V_{DD}	TDO	V_{DDQ}	V_{DD}
B	V_{SS}	V_{SSQ}	DQ1	DQ0	V_{DDQ}					V_{DDQ}	DQ8	DQ9	V_{SSQ}	V_{SS}
C	V_{DDQ}	V_{DDQ}	DQ3	DQ2	V_{SSQ}					V_{SSQ}	DQ10	DQ11	V_{DDQ}	V_{DDQ}
D	V_{SS}	V_{SSQ}	EDC0	WCK01_t	WCK01_c					V_{DD}	V_{SS}	EDC1	V_{SSQ}	V_{SS}
E	V_{DDQ}	V_{DDQ}	DBI0_n	V_{DDQ}	V_{SSQ}					V_{SSQ}	V_{DDQ}	DBI1_n	V_{DDQ}	V_{DDQ}
F	V_{SS}	V_{SSQ}	DQ5	DQ4	V_{DDQ}					V_{DDQ}	DQ12	DQ13	V_{SSQ}	V_{SS}
G	V_{DD}	V_{DDQ}	DQ7	DQ6	V_{SSQ}					V_{SSQ}	DQ14	DQ15	V_{DDQ}	V_{DD}
H	V_{SS}	TMS	V_{DDQ}	RAS_n	V_{DD}					V_{DD}	CKE_n	V_{DDQ}	ZQ	V_{SS}
J	V_{DD}	V_{DDQ}	V_{SS}	A10 A0	A9 A1					BA3 A3	BA0 A2	V_{SS}	V_{DDQ}	V_{DD}
K	V_{SS}	RESET_n	V_{SS}	ABI_n	A12 A13					CK_c	CK_t	A14 A15	V_{REFC}	V_{SS}
L	V_{DD}	V_{DDQ}	V_{SS}	A8 A7	A11 A6					BA1 A5	BA2 A4	V_{SS}	V_{DDQ}	V_{DD}
M	V_{SS}	TCK	V_{DDQ}	CAS_n	V_{DD}					V_{DD}	WE_n	V_{DDQ}	TDI	V_{SS}
N	V_{DD}	V_{DDQ}	DQ31	DQ30	V_{SSQ}					V_{SSQ}	DQ22	DQ23	V_{DDQ}	V_{DD}
P	V_{SS}	V_{SSQ}	DQ29	DQ28	V_{DDQ}					V_{DDQ}	DQ20	DQ21	V_{SSQ}	V_{SS}
R	V_{DDQ}	V_{DDQ}	DBI3_n	V_{DDQ}	V_{SSQ}					V_{SSQ}	V_{DDQ}	DBI2_n	V_{DDQ}	V_{DDQ}
T	V_{SS}	V_{SSQ}	EDC3	WCK23_t	WCK23_c					V_{DD}	V_{SS}	EDC2	V_{SSQ}	V_{SS}
U	V_{DDQ}	V_{DDQ}	DQ27	DQ26	V_{SSQ}					V_{SSQ}	DQ18	DQ19	V_{DDQ}	V_{DDQ}
V	V_{SS}	V_{SSQ}	DQ25	DQ24	V_{DDQ}					V_{DDQ}	DQ16	DQ17	V_{SSQ}	V_{SS}
W	V_{DD}	V_{DDQ}	V_{PP}	V_{DD}	V_{SS}					V_{SS}	V_{DD}	MF	V_{DDQ}	V_{DD}

Data Addresses Other signal Supply Ground

Note: 1. Bytes 1 and 3 are disabled when the device is configured to x16 mode, non-mirrored (MF = 0).

Figure 4: 190-Ball FBGA – MF = 1 (Top View)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	V_{DD}	V_{DDQ}	V_{PP}	V_{DD}	V_{SS}					V_{SS}	V_{DD}	TDO	V_{DDQ}	V_{DD}
B	V_{SS}	V_{SSQ}	DQ25	DQ24	V_{DDQ}					V_{DDQ}	DQ16	DQ17	V_{SSQ}	V_{SS}
C	V_{DDQ}	V_{DDQ}	DQ27	DQ26	V_{SSQ}					V_{SSQ}	DQ18	DQ19	V_{DDQ}	V_{DDQ}
D	V_{SS}	V_{SSQ}	EDC3	WCK23_t	WCK23_c					V_{DD}	V_{SS}	EDC2	V_{SSQ}	V_{SS}
E	V_{DDQ}	V_{DDQ}	DBI3_n	V_{DDQ}	V_{SSQ}					V_{SSQ}	V_{DDQ}	DBI2_n	V_{DDQ}	V_{DDQ}
F	V_{SS}	V_{SSQ}	DQ29	DQ28	V_{DDQ}					V_{DDQ}	DQ20	DQ21	V_{SSQ}	V_{SS}
G	V_{DD}	V_{DDQ}	DQ31	DQ30	V_{SSQ}					V_{SSQ}	DQ22	DQ23	V_{DDQ}	V_{DD}
H	V_{SS}	TMS	V_{DDQ}	CAS_n	V_{DD}					V_{DD}	WE_n	V_{DDQ}	ZQ	V_{SS}
J	V_{DD}	V_{DDQ}	V_{SS}	A8 A7	A11 A6					BA1 A5	BA2 A4	V_{SS}	V_{DDQ}	V_{DD}
K	V_{SS}	RESET_n	V_{SS}	ABI_n	A12 A13					CK_c	CK_t	A14 A15	V_{REFC}	V_{SS}
L	V_{DD}	V_{DDQ}	V_{SS}	A10 A0	A9 A1					BA3 A3	BA0 A2	V_{SS}	V_{DDQ}	V_{DD}
M	V_{SS}	TCK	V_{DDQ}	RAS_n	V_{DD}					V_{DD}	CKE_n	V_{DDQ}	TDI	V_{SS}
N	V_{DD}	V_{DDQ}	DQ7	DQ6	V_{SSQ}					V_{SSQ}	DQ14	DQ15	V_{DDQ}	V_{DD}
P	V_{SS}	V_{SSQ}	DQ5	DQ4	V_{DDQ}					V_{DDQ}	DQ12	DQ13	V_{SSQ}	V_{SS}
R	V_{DDQ}	V_{DDQ}	DBI0_n	V_{DDQ}	V_{SSQ}					V_{SSQ}	V_{DDQ}	DBI1_n	V_{DDQ}	V_{DDQ}
T	V_{SS}	V_{SSQ}	EDC0	WCK01_t	WCK01_c					V_{DD}	V_{SS}	EDC1	V_{SSQ}	V_{SS}
U	V_{DDQ}	V_{DDQ}	DQ3	DQ2	V_{SSQ}					V_{SSQ}	DQ10	DQ11	V_{DDQ}	V_{DDQ}
V	V_{SS}	V_{SSQ}	DQ1	DQ0	V_{DDQ}					V_{DDQ}	DQ8	DQ9	V_{SSQ}	V_{SS}
W	V_{DD}	V_{DDQ}	V_{PP}	V_{DD}	V_{SS}					V_{SS}	V_{DD}	MF	V_{DDQ}	V_{DD}

Data Addresses Other signal Supply Ground

Note: 1. Bytes 0 and 2 are disabled when the device is configured to x16 mode, mirrored (MF = 1).

Table 2: 190-Ball FBGA Ball Descriptions

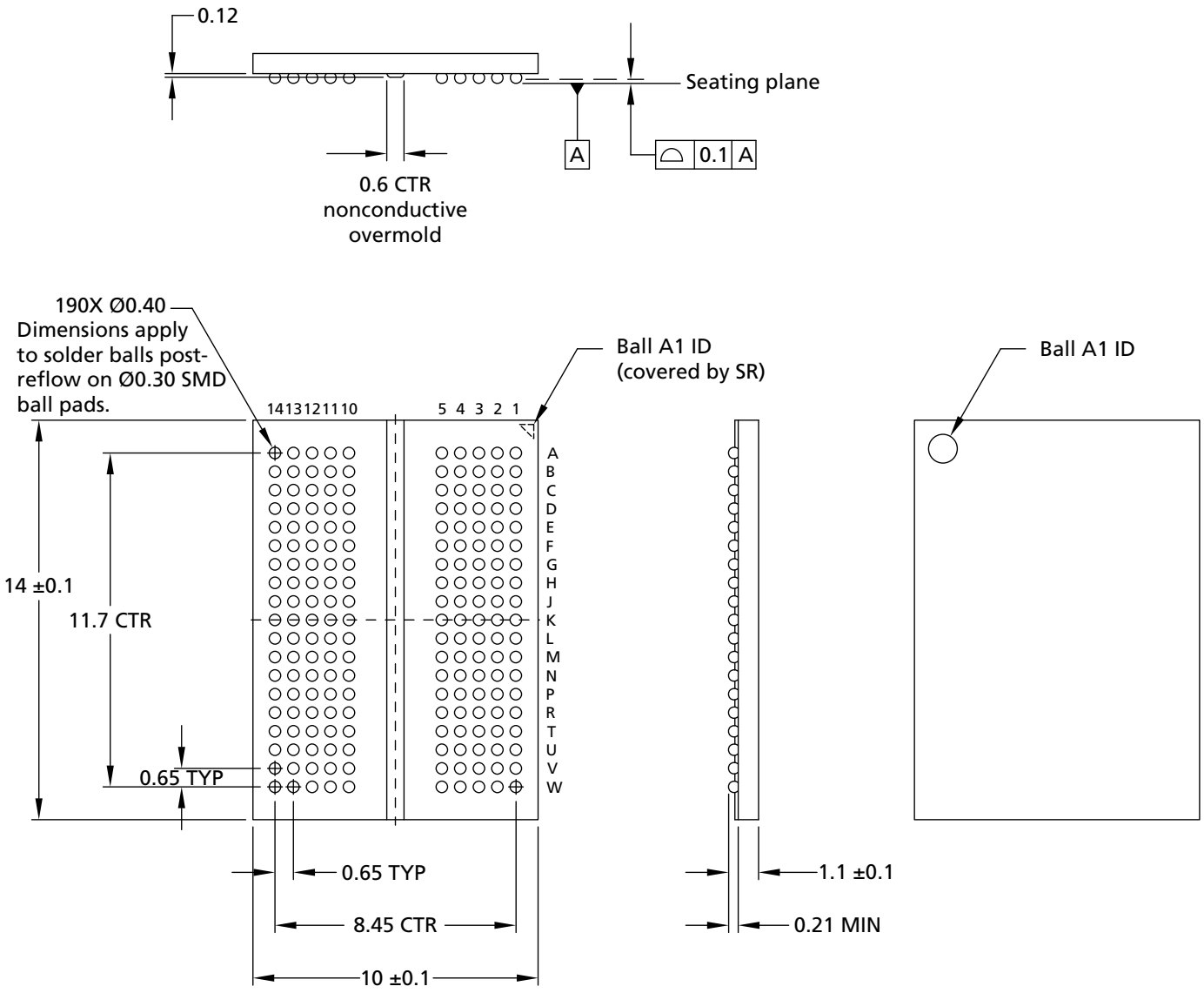
Symbol	Type	Description
A[15:0]	Input	**Address inputs:** A[13:0] (A14) provide the row address for ACTIVATE commands. A[5:0] provide the lower column address (CAL), and A7, A9, and A[15:12] the upper column address (CAU) in QDR operating mode; A[6:0] provide the lower column address (CAL), and A[7:6], A9, and A[15:12] the upper column address (CAU) in DDR operating mode. A8 defines the AUTO PRECHARGE function for READ/WRITE commands, to select one location out of the memory array in the respective bank. A8 sampled during a PRECHARGE command determines whether the precharge applies to one bank (A8 LOW, bank selected by BA[3:0]) or all banks (A8 HIGH). The address inputs also provide the op-code during a MODE REGISTER SET command and the data bits during a LDFF command. A[12:8] and A14 are sampled with the rising edge of CK_t and A[7:0], A13, and A15 are sampled with the rising edge of CK_c. CAL is associated with DQ[15:0] and CAU is associated with DQ[31:16].
ABI_n	Input	**Address bus inversion**
BA[3:0]	Input	**Bank address inputs:** BA[3:0] define to which bank an ACTIVATE, READ, WRITE, PRECHARGE, or PER-BANK REFRESH command is being applied. BA[3:0] also determine which mode register is accessed with an MODE REGISTER SET command. BA[3:0] are sampled with the rising edge of CK_t.
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. Command inputs are latched on the rising edge of CK_t. Address inputs are latched on the rising edge of CK_t and the rising edge of CK_c. All latencies are referenced to CK_t.
WCK01_t, WCK01_c/ WCK23_t, WCK23_c	Input	**Write Clocks:** WCK_t and WCK_c are differential clocks used for write data capture and read data output. WCK01_t/WCK01_c is associated with DQ[15:0], DBI0_n, DBI1_n, EDC0, and EDC1. WCK23_t/WCK23_c is associated with DQ[31:16], DBI2_n, DBI3_n, EDC2, and EDC3.
CKE_n	Input	**Clock enable:** CKE_n LOW activates and CKE_n HIGH deactivates the internal clock, device input buffers, and output drivers. Taking CKE_n HIGH provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or ACTIVE POWER-DOWN (LOW ACTIVE in any bank). CKE_n must be maintained LOW throughout read and write accesses.
MF	Input	**Mirror function:** Must be tied to power or ground.
RAS_n, CAS_n, WE_n	Input	**Command inputs:** RAS_n, CAS_n, and WE_n define the command being entered.
RESET_n	Input	**Reset:** RESET_n LOW asynchronously initiates a full chip reset. With RESET_n LOW all ODTs are disabled. A full chip reset may be performed at any time by pulling RESET_n LOW.
DQ[31:0]	I/O	**Data input/output:** Bidirectional 32-bit data bus.
DBI[3:0]_n	I/O	**Data bus inversion:** DBI0_n is associated with DQ[7:0], DBI1_n is associated with DQ[15:8], DBI2_n is associated with DQ[23:16], DBI3_n is associated with DQ[31:24].
EDC[3:0]	Output	**Error detection code:** The calculated CRC data is transmitted on these pins. In addition these pins drive a hold pattern when idle and can be used as an RDQS function. EDC0 is associated with DQ[7:0], EDC1 is associated with DQ[15:8], EDC2 is associated with DQ[23:16], EDC3 is associated with DQ[31:24].
V_{DD}	Supply	**Power supply**
V_{DDQ}	Supply	**DQ power supply:** I/O power supply
V_{REFC}	Supply	**Reference voltage for address and command pins**

Table 2: 190-Ball FBGA Ball Descriptions (Continued)

Symbol	Type	Description
V_{PP}	Supply	**Pump Voltage**
V_{SS}	Supply	**Ground**
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Supply	**External reference ball for impedance calibration**
TDI	Input	**JTAG test data input**
TDO	Output	**JTAG test data output**
TMS	Input	**JTAG test mode select**
TCK	Input	**JTAG test clock**

Package Dimensions

Figure 5: 190-Ball FBGA (JA)



Notes:
1. Package dimension specification is compliant to MO-246 Rev. G, variation T14.0x10.0-HK-190G.
2. All dimensions are in millimeters.
3. Solder ball material: SAC-Q (92.5% Sn, 4% Ag, 3% Bi, 0.5% Cu).

Functional Description

Functional Overview

The GDDR5X SGRAM is a high speed dynamic random-access memory designed for applications requiring high bandwidth. It is internally configured as 16-bank memory and contains 8,589,934,592 bits.

The device's high-speed interface is optimized for point-to-point connections to a host controller. On-die termination (ODT) is provided for all high-speed interface signals to eliminate the need for termination resistors in the system.

Two operating modes are supported which mainly differ in the internal prefetch and DQ/DBI_n pin to WCK clock frequency ratio. The operating mode is set by a mode register bit:

- In quad data rate (QDR) mode the interface transfers four 32-bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 16n-prefetch a single write or read access consists of a 512-bit wide, two CK clock cycle data transfer at the internal memory core and sixteen corresponding 32-bit wide one-quarter WCK clock cycle data transfers to the I/O pins.
- In double data rate (DDR) mode the interface transfers two 32-bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 8n-prefetch a single write or read access consists of a 256-bit wide, two CK clock cycle data transfer at the internal memory core and eight corresponding 32-bit wide one-half WCK clock cycle data transfers to the I/O pins.

Read and write accesses are burst oriented; an access starts at a selected location and consists of a total of sixteen data words in QDR mode and eight data words in DDR mode. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command and the next rising CK_c edge are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command and the next rising CK_c edge are used to select the bank and the column location for the burst access.

Mirror Function Enable

A mirror function (MF) mode is provided to change the physical location of the data, command and address pins assisting in PCB signal routing. The MF pin should be tied directly to V_{SSQ} or V_{DDQ} depending on the desired ballout.

It is pointed out that this mirror function mode swaps the location of the data bytes (Byte 0 .. Byte 3). The controller must strictly adhere to this data byte order because this byte order is assumed in the internal assignment of the write data mask received with WDM and WSM commands.

Table 3: ADD/CMD Signals Affected by Mirror Function Mode (MF)

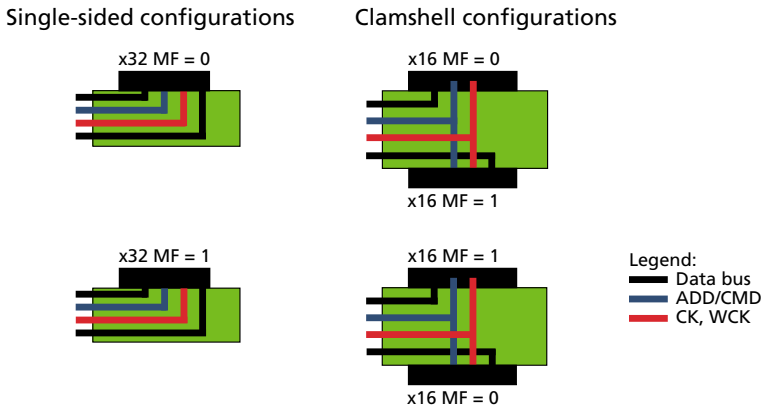
Ball	Signal		Ball	Signal		Ball	Signal	
	MF = 0	MF = 1		MF = 0	MF = 1		MF = 0	MF = 1
H-4	RAS_n	CAS_n	J-10	BA3 A3	BA1 A5	L-10	BA1 A5	BA3 A3
H-11	CKE_n	WE_n	J-11	BA0 A2	BA2 A4	L-11	BA2 A4	BA0 A2
J-4	A10 A0	A8 A7	L-4	A8 A7	A10 A0	M-4	CAS_n	RAS_n
J-5	A9 A1	A11 A6	L-5	A11 A6	A9 A1	M-11	WE_n	CKE_n

Clamshell Mode

A GDDR5X SGRAM based memory system is typically divided into several channels each being 32-bit wide. A channel can be comprised of a single GDDR5X SGRAM operated in x32 mode, or two GDDR5X SGRAMs each operated in x16 (clamshell) mode, and typically assembled on opposite sides of the PCB. Clamshell mode is an elegant method to double the channel's memory density.

In x32 mode all high-speed data pins (DQ, DBI_n, EDC) and WCK clocks shall be routed point-to-point (P2P). In x16 mode, all high-speed data pins (DQ, DBI_n, EDC) and WCK clocks are recommended to be routed P2P. WCK is allowed to be routed point-to-two-point (P22P) for x16 mode but may limit achievable frequencies. The ADD/CMD and CK clock shall be routed P2P when the device is operated in x32 mode, and P22P when the devices are operated in x16 mode as shown in Figure 6. Note that in x16 mode one device must be configured to MF = 0 (non-mirrored) and the other device to MF = 1 (mirrored). In x32 mode the device can be configured to MF = 0 or MF = 1 depending on PCB routing preferences.

Figure 6: Example PCB Layout Topologies



GDDR5X SGRAMs are configured to either x32 mode or x16 mode at power-up with RESET_n going HIGH. The mode is selected on the pin at location D-12 which is EDC1 when configured to MF = 0 and EDC2 when configured to MF = 1. For x16 mode this pin is tied to V_{SSQ}; the pin is part of the two bytes that are disabled in this mode and therefore not needed for EDC functionality. For x32 mode this pin is active and terminated to V_{DDQ} in the system or by the controller. The disabled pins in x16 mode are all in a High-Z state, non-terminating.

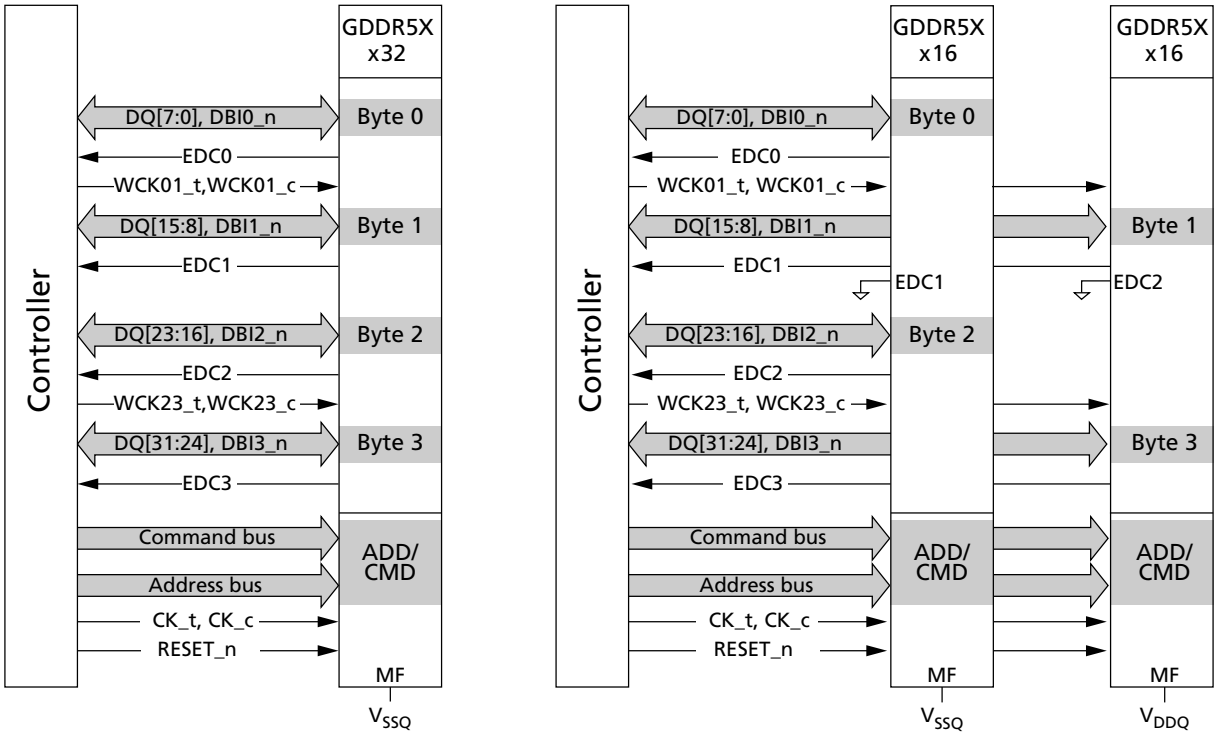
The ADD/CMD and CK pin ODT are enabled with a value as determined by the level of the CKE_n pin at RESET_n going HIGH.

Table 4: MF, x32/x16 Mode and Default ADD/CMD/CK ODT

Mode	MF	EDC1 (MF = 0) or EDC2 (MF = 1)	Default ADD/CMD/CK ODT
x16 non-mirrored	V_{SSQ}	V_{SSQ}	ZQ = 120Ω
x32 non-mirrored	V_{SSQ}	V_{DDQ} (terminated by the system or controller)	ZQ/2 = 60Ω
x16 mirrored	V_{DDQ}	V_{SSQ}	ZQ = 120Ω
x32 mirrored	V_{DDQ}	V_{DDQ} (terminated by the system or controller)	ZQ/2 = 60Ω

Usually the configuration is fixed in the system. Once the configuration has been set, it cannot be changed during normal operation. A comparison of x32 mode and x16 mode systems is shown in Figure 7.

Figure 7: System View for x32 Mode vs. x16 Mode



Clocking

The device operates from a differential clock CK_t and CK_c. Commands are registered at every rising edge of CK_t. Addresses are registered at every rising edge of CK_t and every rising edge of CK_c.

The data interface uses two differential forwarded clocks WCK_t and WCK_c, each associated with two data bytes. WCK_t and WCK_c are continuously running and operate at twice the frequency of the command/address clock (CK_t/CK_c). A PLL is associated

with each WCK pair. The use of the PLL is mandatory in QDR mode and not supported in DDR mode.

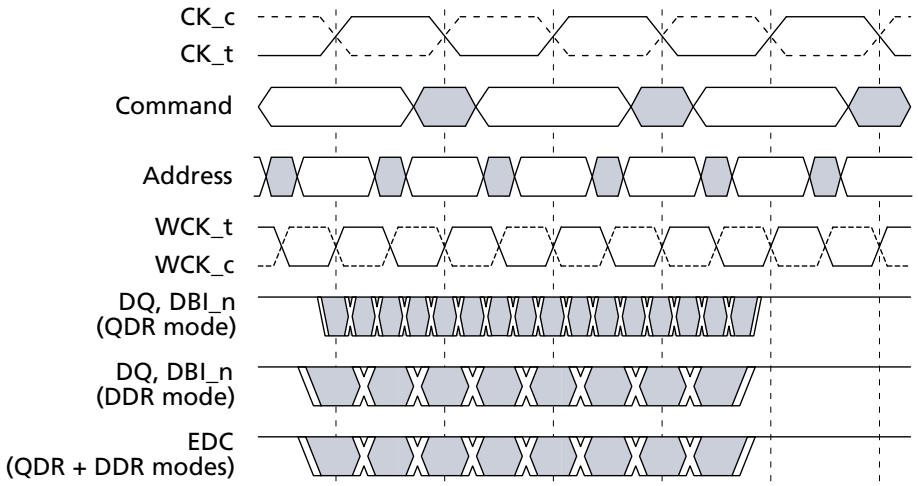
- QDR mode uses a quad data rate data interface and a 16n-prefetch architecture for DQ/DBI_n, and a double data rate data interface and 8n-prefetch architecture for EDC. The PLL generates four equally spaced clock edges per WCK clock cycle. QDR means that four DQ/DBI_n data words per WCK cycle are registered at these internally generated clock edges. DDR means that two EDC data words per WCK cycle are registered at every second of these internally generated clock edges.
- DDR mode uses a double data rate data interface and an 8n-prefetch architecture for DQ/DBI_n/EDC. DDR means that the data is registered at every rising edge of WCK_t and rising edge of WCK_c.

The table below and Figure 8 illustrate the clock and interface signal relationship for both QDR and DDR operating modes.

Table 5: Example Clock and Interface Signal Frequency Relationship

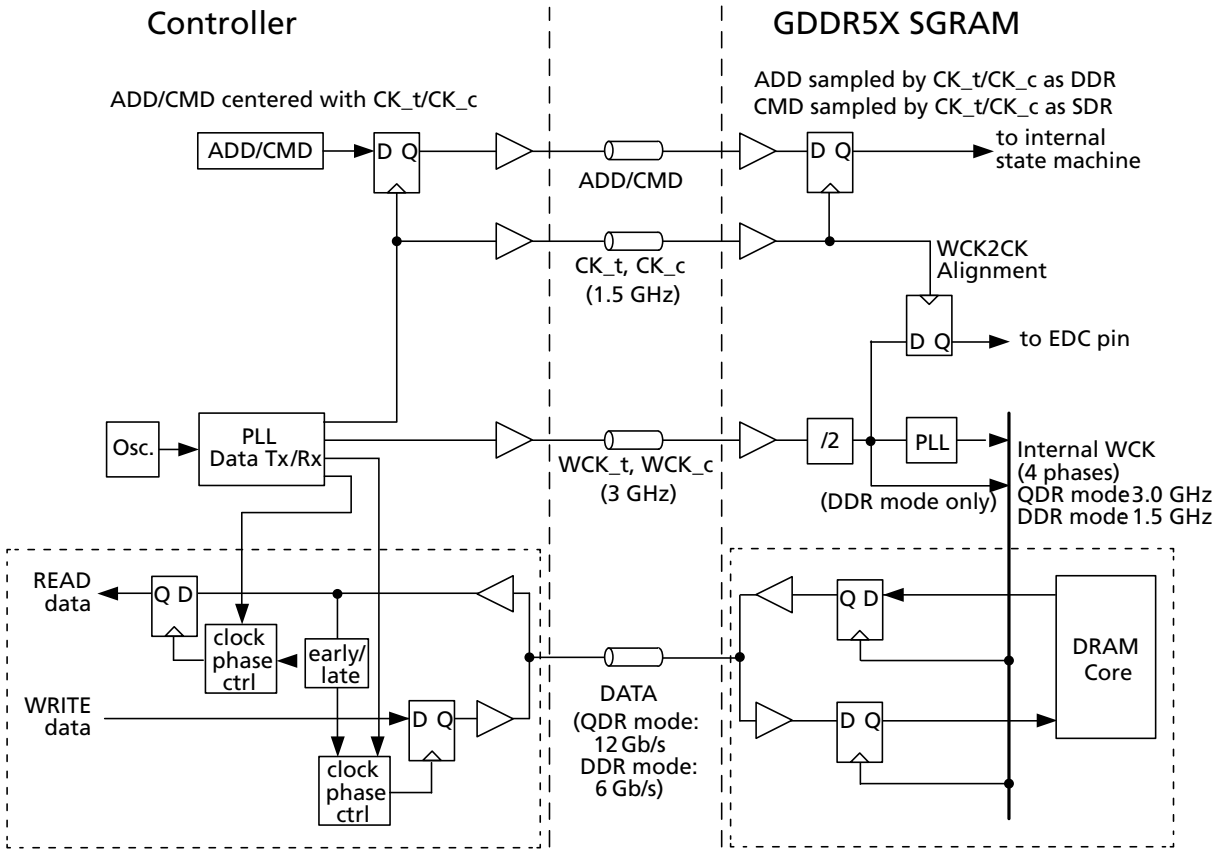
Pin	QDR Mode	DDR Mode	Unit
CK_t, CK_c	1.5	1.5	GHz
Command	1.5	1.5	Gbps/pin
Address	3	3	Gbps/pin
WCK_t, WCK_c	3	3	GHz
DQ, DBI_n	12	6	Gbps/pin
EDC	6	6	Gbps/pin

Figure 8: Clocking and Interface Relationship



Note: 1. Above shows the relationship between the data rate of the buses and the clocks, and is not a timing diagram.

Figure 9: Block Diagram of an Example Clock System



Addressing

GDDR5X SGRAMs use a double data rate address scheme to reduce pins required on the device as shown in Table 6. The addresses should be provided in two parts; the first half is latched on the rising edge of CK_t along with the command pins such as RAS_n, CAS_n, and WE_n; the second half is latched on the next rising edge of CK_c.

The use of DDR addressing allows all address values to be latched in at the same rate as the SDR commands. All addresses related to command access have been positioned for latching on the initial rising edge for faster decoding.

Table 6: Address Pairs

Clock Edge	Address Inputs									
Rising CK_t	BA3	BA2	BA1	BA0	A14	A12	A11	A10	A9	A8
Rising CK_c	A3	A4	A5	A2	A15	A13	A6	A0	A1	A7

Table 7: Addressing

Parameter		256 Meg x 32	512 Meg x 16
Row address		A0 to A13	A0 to A14
Column address DQ[15:0]	QDR mode	A0 to A5	
	DDR mode	A0 to A6	
Column address DQ[31:16]	QDR mode	A7, A9, A12 to A15	
	DDR mode	A7, A9, A12 to A15, A6	
Bank address		BA0 to BA3	
Auto precharge		A8	
Page size		4K	2K
Refresh		16K/32ms	
Refresh period		1.9µs	

Note: 1. The burst order is fixed for reads and writes, and no column address bits are assigned to distinguish between the UIs of a burst. A memory controller may internally assign such column address bits, but these column address bits are not transmitted on the column address bus.

Two column addresses with a common bank address are provided with each READ and WRITE command, allowing two pseudo-independent memory accesses with 32 bytes access granularity in QDR operating mode and 16 bytes access granularity in DDR operating mode:

- The lower column address (CAL) is associated with DQ[15:0] and received on addresses A[5:0].
- The upper column address (CAU) is associated with DQ[31:16] and received on addresses A[15:12, 9, 7].

The addressing is transparent between QDR and DDR operating modes: data can be written in QDR operating mode with a single BL = 16 WRITE burst, and read in DDR operating mode with two BL = 8 READ bursts, and vice versa. Column address A6 is evaluated in DDR operating mode only; it can be considered the LSB and selects between the data corresponding to the first half of a BL = 16 burst (UI 0..7) with A6 being set LOW, and the data corresponding to the second half of a BL = 16 burst (UI 8..15) with A6 being set HIGH.

Figure below illustrates the addressing in QDR and DDR operating modes assuming the same column addresses CAL and CAU for lower and upper data bytes. This is equivalent to accesses using a single column address, however, it is required to provide both CAL and CAU along with the READ or WRITE command.

Figure 10: Column Accesses with Identical Lower and Upper Column Addresses

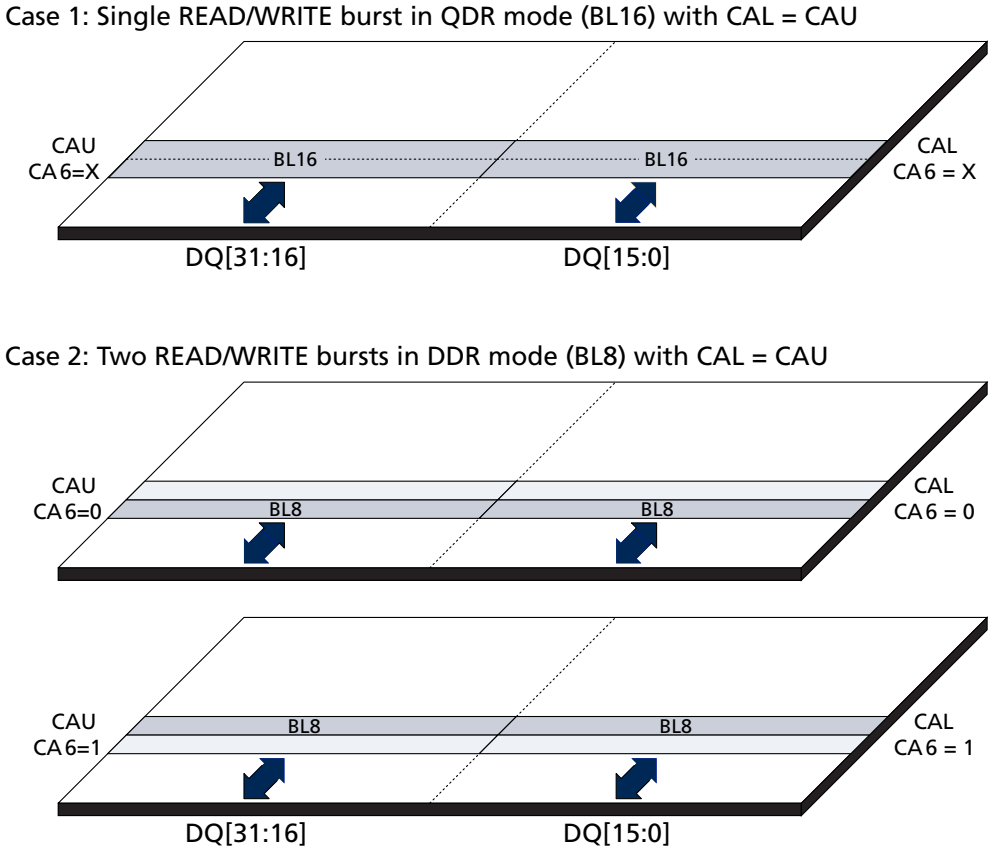
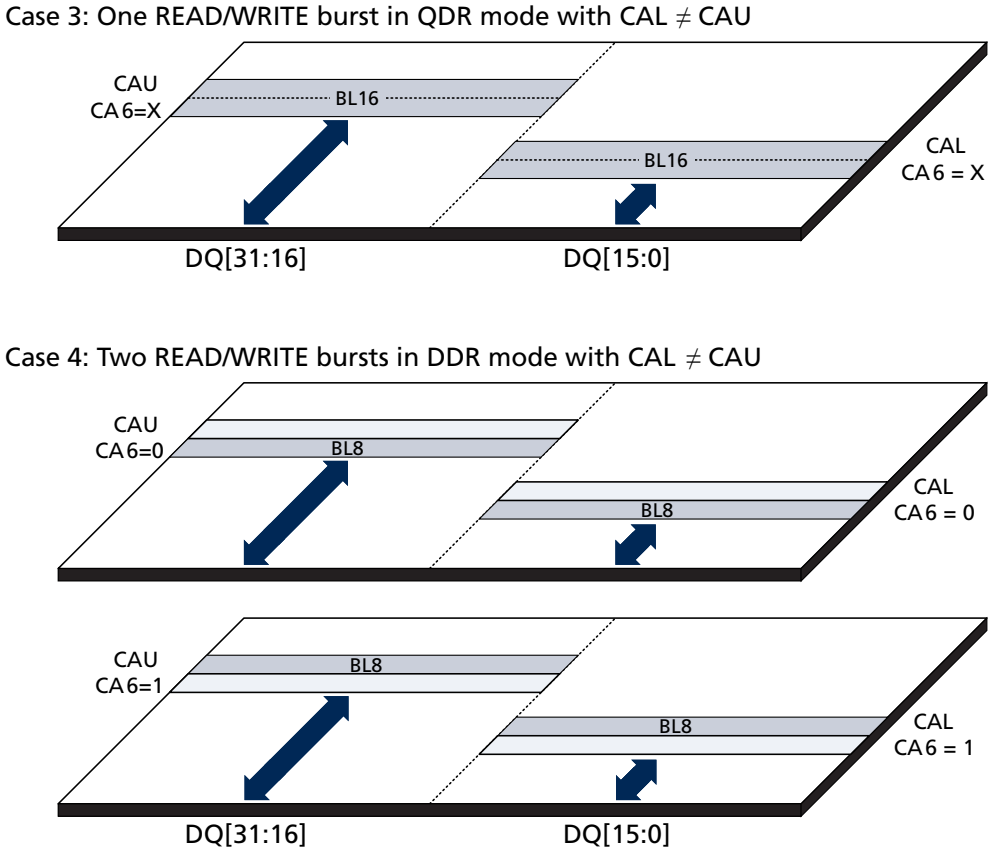


Figure below illustrates the addressing in QDR and DDR operating modes assuming different column address for lower and upper bytes. This corresponds to two pseudo-independent memory accesses with 32 bytes access granularity in QDR operating mode and 16 bytes in DDR operating mode. It is pointed out that both accesses share the bank address, and therefore access the same open row in that bank.

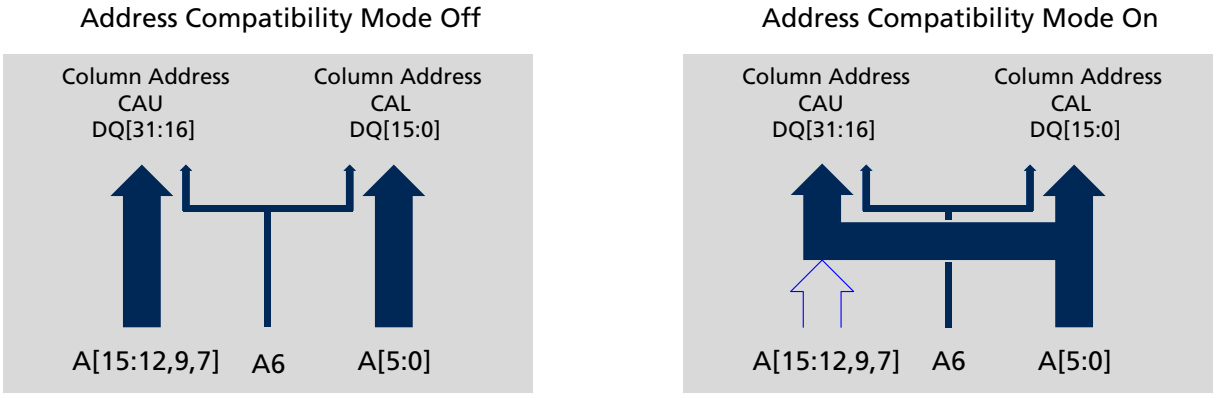
Figure 11: Column Accesses with Different Lower and Upper Column Addresses



Address Compatibility Mode

GDDR5 SGRAMs receive the column address on the lower address pins only; this column address is used for all data bytes. The address compatibility mode adopts this functionality for GDDR5X SGRAMs: if enabled by bit A8 in MR8, the device will use the column address received on A[5:0] as CAL and CAU. Address inputs A[15:12, 9, 7] are ignored in this mode. The memory accesses will be identical to those shown in Figure 10 for both BL = 16 and BL = 8 cases.

Figure 12: Address Compatibility Mode



Operating Conditions

Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 8: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–0.3	2.0	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.3	2.0	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.3	2.3	V	1 , 2
V_{IN}/V_{OUT}	Voltage on any pins relative to V_{SS}	–0.3	2.0	V	
T_{STG}	Storage temperature	–55	125	°C	

Notes:
1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times the device is power-up.
2. V_{PP} must be equal or greater than V_{DD} and V_{DDQ} at all times the device is power-up.

DC and AC Operating Conditions

GDDR5X SGRAMs are designed for 1.35V typical operating voltages. The interface follows the POD135 standard (JESD8-21A). All AC and DC values are measured at the ball.

Table 9: DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{DD}	Device supply voltage	1.3095	1.35	1.3905	V	1
V_{DDQ}	Output supply voltage	1.3095	1.35	1.3905	V	1
V_{PP}	Pump voltage	1.746	1.8	1.908	V	2
V_{REFD}	Reference voltage: DQ and DBI_n pins	0.69 × V_{DDQ}	–	0.71 × V_{DDQ}	V	3, 4
V_{REFD2}		0.49 × V_{DDQ}	–	0.51 × V_{DDQ}	V	3, 4, 5
V_{REFC}	Reference voltage: ADD/CMD pins	0.69 × V_{DDQ}	–	0.71 × V_{DDQ}	V	6
V_{REFC2}		0.49 × V_{DDQ}	–	0.51 × V_{DDQ}	V	6
V_{IHA}(DC)	DC input logic HIGH voltage with V_{REFC}: ADD/CMD pins	V_{REFC} + 0.135	–	–	V	7, 9
V_{ILA}(DC)	DC input logic LOW voltage with V_{REFC}: ADD/CMD pins	–	–	V_{REFC} - 0.135	V	7, 9
V_{IHA2}(DC)	DC input logic HIGH voltage with V_{REFC2}: ADD/CMD pins	V_{REFC2} + 0.27	–	–	V	9
V_{ILA2}(DC)	DC input logic LOW voltage with V_{REFC2}: ADD/CMD pins	–	–	V_{REFC2} - 0.27	V	9
V_{IHD}(DC)	DC input logic HIGH voltage with V_{REFD}: DQ and DBI_n pins	V_{REFD} + 0.09	–	–	V	8, 9
V_{ILD}(DC)	DC input logic LOW voltage with V_{REFD}: DQ and DBI_n pins	–	–	V_{REFD} - 0.09	V	8, 9
V_{IHD2}(DC)	DC input logic HIGH voltage with V_{REFD2}: DQ and DBI_n pins	V_{REFD2} + 0.27	–	–	V	9
V_{ILD2}(DC)	DC input logic LOW voltage with V_{REFD2}: DQ and DBI_n pins	–	–	V_{REFD2} - 0.27	V	9
V_{IHR}	RESET_n, MF and boundary scan input logic HIGH voltage; EDC1/2 input logic HIGH voltage for ×32/×16 mode select	0.8 × V_{DDQ}	–	–	V	9
V_{ILR}	RESET_n, MF and boundary scan input logic LOW voltage; EDC1/2 input logic LOW voltage for ×32/×16 mode select	–	–	0.2 × V_{DDQ}	V	9
I_L	Input leakage current (any input 0V ≤ V_{IN} ≤ V_{DDQ}; all other pins not under test = 0V)	–5	–	5	µA	10
I_{OZ}	Output leakage current (outputs are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	–5	–	5	µA	11
V_{OL}(DC)	Output logic LOW voltage	–	–	0.56	V	

Notes:
1. GDDR5X SGRAM devices are designed to tolerate PCB designs with separate V_{DDQ} and V_{DD} power regulators.
2. DC bandwidth is limited to 20 MHz.

3. AC noise in the system is estimated at 50mV peak-to-peak for the purpose of DRAM design.
4. The reference voltage source and control for DQ and DBI_n pins are determined by half V_{REFD}, V_{REF} C2D and V_{REFD} level mode register bits.
5. Programmable V_{REFD} levels are not supported with V_{REFD2}.
6. The reference voltage source (external or internal) is determined at power-up; the reference voltage level is determined by half V_{REFC} mode register bit.
7. ADD/CMD input slew rate must be greater than or equal to 2.7 V/ns. The slew rate is measured between V_{REFC} crossing and V_{IHA}(AC) or V_{ILA}(AC), or between V_{REFC2} crossing and V_{IHA2}(AC) or V_{ILA2}(AC).
8. DQ/DBI_n input slew rate must be greater than or equal to 2.7 V/ns. The slew rate is measured between V_{REFD} crossing and V_{IHD}(AC) or V_{ILD}(AC), or between V_{REFD2} crossing and V_{IHD2}(AC) or V_{ILD2}(AC).
9. V_{IHR} and V_{ILR} apply to boundary scan input pins TDI, TMS, and TCK. V_{IHR} and V_{ILR} also apply to ADD/CMD, CK_t/CK_c, DQ, DBI_n, and WCK_t/WCK_c input pins when boundary scan mode is active and input data are latched in the capture-DR TAP controller state.
10. I_L is measured with ODT off. Any input $0V \le V_{IN} \le V_{DDQ}$; all other pins not under test excluding TDI, TMS, and TCK = 0V.
11. I_{OZ} is measured with DQ disabled; $0V \le V_{OUT} \le V_{DDQ}$.

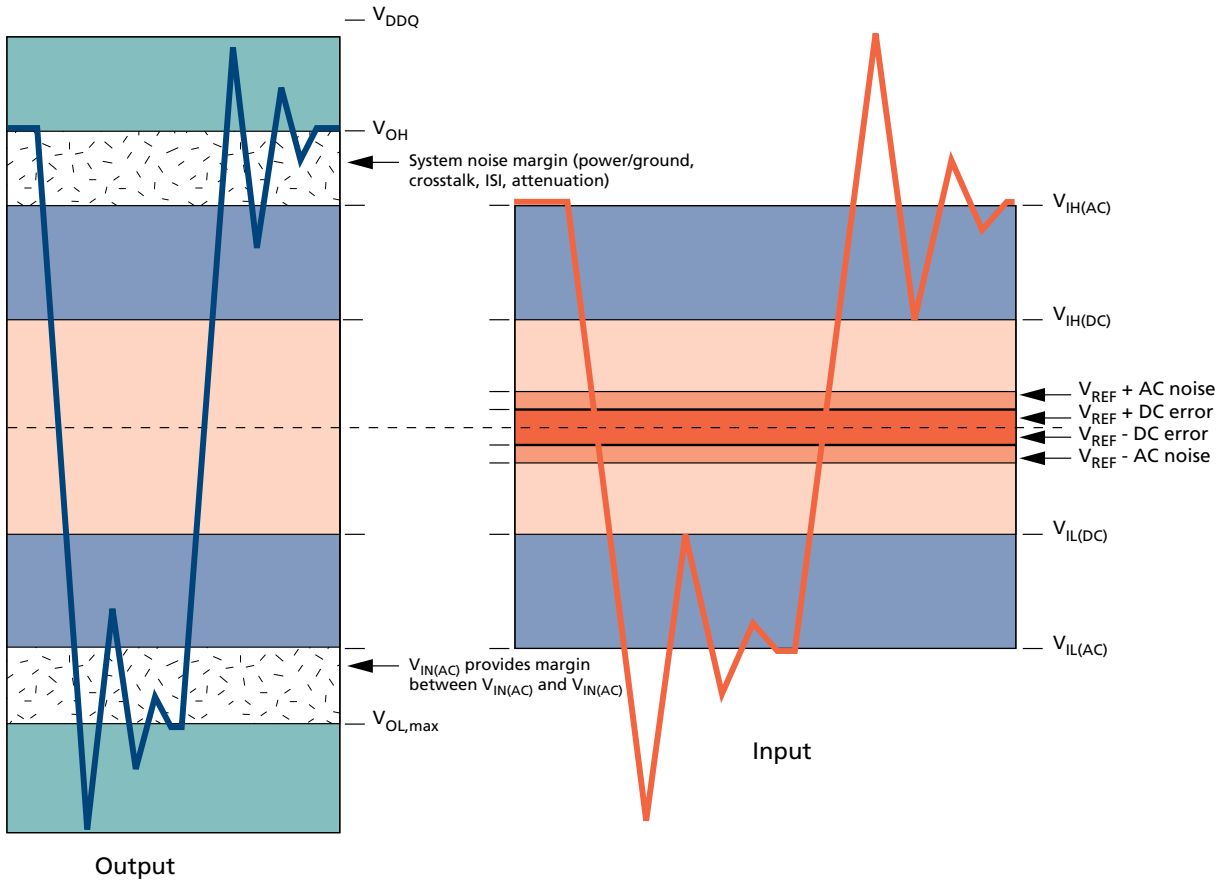
Table 10: AC Operating Conditions

Note 1 applies to the entire table

Symbol	Parameter	Min	Typ	Max	Unit
V_{IHA}(AC)	AC input logic HIGH voltage with V_{REFC}: ADD/CMD pins	V_{REFC} + 0.18	–	–	V
V_{ILA}(AC)	AC input logic LOW voltage with V_{REFC}: ADD/CMD pins	–	–	V_{REFC} - 0.18	V
V_{IHA2}(AC)	AC input logic HIGH voltage with V_{REFC2}: ADD/CMD pins	V_{REFC} + 0.36	–	–	V
V_{ILA2}(AC)	AC input logic LOW voltage with V_{REFC2}: ADD/CMD pins	–	–	V_{REFC} - 0.36	V
V_{IHD}(AC)	AC input logic HIGH voltage with V_{REFD}: DQ and DBI_n pins	V_{REFD} + 0.135	–	–	V
V_{ILD}(AC)	AC input logic LOW voltage with V_{REFD}: DQ and DBI_n pins	–	–	V_{REFD} - 0.135	V
V_{IHD2}(AC)	AC input logic HIGH voltage with V_{REFD2}: DQ and DBI_n pins	V_{REFD2} + 0.36	–	–	V
V_{ILD2}(AC)	AC input logic LOW voltage with V_{REFD2}: DQ and DBI_n pins	–	–	V_{REFD2} - 0.36	V

Note: 1. Use V_{IHR} and V_{ILR} when boundary scan mode is active and input data are latched in the capture-DR TAP controller state.

Figure 13: Voltage Waveform



Note: 1. V_{REF}, V_{IH}, and V_{IL} refer to whichever V_{REFxx} (V_{REFD}, V_{REFD2}, V_{REFC}, or V_{REFC2}) is being used.

Table 11: Clock Input Operating Conditions

Symbol	Parameter	Min	Max	Unit	Notes
V_{MP}(DC)	Clock input mid-point voltage: CK_t, CK_c	V_{REFC} - 0.10	V_{REFC} + 0.10	V	1, 6
V_{IDCK}(DC)	Clock input differential voltage: CK_t, CK_c	0.198	–	V	4, 6
V_{IDCK}(AC)	Clock input differential voltage: CK_t, CK_c	0.36	–	V	2, 4, 6
V_{IDWCK}(DC)	Clock input differential voltage: WCK_t, WCK_c	0.18	–	V	5, 7
V_{IDWCK}(AC)	Clock input differential voltage: WCK_t, WCK_c	0.27	–	V	2, 5, 7
V_{IN}	Single ended clock input voltage level: CK_t, CK_c, WCK_t, WCK_c	–0.30	V_{DDQ} + 0.30	V	12
CK_{slew}	Single ended slew rate: CK_t, CK_c	2.7	–	V/ns	9
WCK_{slew}	Single ended slew rate: WCK_t, WCK_c	2.7	–	V/ns	10
V_{IXCK}(AC)	Clock input crossing point voltage: CK_t, CK_c	V_{REFC} - 0.108	V_{REFC} + 0.108	V	2, 3, 6
V_{IXWCK}(AC)	Clock input crossing point voltage: WCK_t, WCK_c	V_{REFD} - 0.09	V_{REFD} + 0.09	V	2, 3, 7, 8

Notes:
1. This provides a minimum of 0.845V to a maximum of 1.045V and is nominally 70% of V_{DDQ}. DRAM timings relative to CK_t cannot be guaranteed if these limits are exceeded.
2. For AC operations, all DC clock requirements must be satisfied as well.
3. The value of V_{IXCK} and V_{IXWCK} is expected to equal 70% V_{DDQ} for the transmitting device and must track variations in the DC level of the same.
4. V_{IDCK} is the magnitude of the difference between the input level in CK_t and the input level on CK_c. The input reference level for signals other than CK_t and CK_c is V_{REFC}.
5. V_{IDWCK} is the magnitude of the difference between the input level in WCK_t and the input level on WCK_c. The input reference level for signals other than WCK_t and WCK_c is either V_{REFC}, V_{REFC2}, V_{REFD}, or V_{REFD2}.
6. The CK_t and CK_c input reference level (for timing referenced to CK_t and CK_c) is the point at which CK_t and CK_c cross. Refer to the applicable timings in the AC Timing tables.
7. The WCK_t and WCK_c input reference level (for timing referenced to WCK_t and WCK_c) is the point at which WCK_t and WCK_c cross. Refer to the applicable timings in the AC Timing tables.
8. V_{REFD} is either V_{REFD}, V_{REFD2}, or V_{REFC}.
9. The slew rate is measured between V_{REFC} crossing and V_{IXCK}(AC).
10. The slew rate is measured between V_{REFD} crossing and V_{IXWCK}(AC).
11. Ringback below V_{ID}(DC) is not allowed.
12. Use V_{IHR} and V_{ILR} when boundary scan mode is active and input data are latched in the capture-DR TAP controller state.

Figure 14: Clock Waveform