MC56F825XE_4M53V
Rev 0, 02/2014

MC56F825x/MC56F824x (4M53V) Chip Errata

The following errata items apply to devices of the mask set 4M53V.

23254: IIC interrupt flag (IIC_SR[IICIF]) is automatically cleared when DSC exits stop mode

Description: When address matching occurs while the IIC operates in slave receive mode, the IIC can wake the core from stop mode. However, the IICIF flag is then cleared automatically. As a result, the IIC address matching interrupt service routine cannot be entered.

Impact: If two or more peripherals are configured to wake the core from stop mode, it is difficult to determine whether an IIC module (or another module) wakes the core due to the automatic clearing of the IICIF flag.

Refer to the Description.

Workaround: Do not configure two IICs to wake the core from stop mode when address matching occurs; use only one IIC to wake the core from stop mode.

In case peripherals other than the IIC are also configured to wake the core from stop mode, use a software flag (such as SIM_SWC0) to indicate that the IIC wakes the core as follows:

1. Before executing a STOP instruction, set the software flag.
2. In the wakeup interrupt service routine for peripherals other than the IIC, clear the software flag.
3. After executing the STOP instruction, check the software flag.
4. If the software flag is still set, then the wakeup event was generated by the IIC, and the normal wakeup event handler for the IIC executes afterwards.

1. Program the IIC slave to use address matching.
2. Before entering stop mode, program the applicable IIC module's bit in the SIM_SD1 register to enable the module's clock to continue to operate in stop mode.
3. Enter stop mode.
4. On an address match event, an interrupt occurs and the IICIF flag remains set.

25283: RAM corruption at device reset

Description: On-chip RAM data can be corrupted if a hardware or COP reset is performed.

Impact: User data stored in on-chip RAM can be corrupted any time that a hardware or COP reset occurs.

Workaround: Store data in the flash memory used as EEPROM or in the SIM's general purpose software control registers (SIM_SCR0 – SIM_SCR3), which retain data after reset.

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Document Number: MC56F825XE_4M53V
Rev. 0
02/2014