PIC18F46J11

PIC18F46J11 Family
Silicon Errata and Data Sheet Clarification

The PIC18F46J11 family devices that you have received conform functionally to the current Device Data Sheet (DS39932**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F46J11 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F46J11 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	
		A2	A4
PIC18F24J11	0x26Ch	2h	4h
PIC18F25J11	0x26Dh		
PIC18F26J11	0x26Eh		
PIC18F44J11	0x26Fh		
PIC18F45J11	0x270h		
PIC18F46J11	0x271h		
PIC18LF24J11	0x272h		
PIC18LF25J11	0x273h		
PIC18LF26J11	0x274h		
PIC18LF44J11	0x275h		
PIC18LF45J11	0x276h		
PIC18LF46J11	0x277h		

Note 1: The Device IDs (DEVID and REVID) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format, "DEVID:REVID".

2: Refer to the *"PIC18F2XJXX/4XJXX Family Flash Microcontroller Programming Specification"* (DS39687) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				A2	A4
MSSP	I^2C™ Mode	1.	If a Stop condition occurs in the middle of an address or data reception, there will be issues with the SCL clock stream and RCEN bit.	X	X
MSSP	I^2C™ Slave Reception	2.	In I^2C™ slave reception, the module may have problems receiving correct data.	X	X
EUSART	Enable/ Disable	3.	If interrupts are enabled, disabling and re-enabling the module requires a 2 TCY delay.	X	X
A/D	FOSC/2 Clock	4.	FOSC/2 A/D Conversion mode may not meet linearity error limits.	X	X
PMP	PSP/PMP	5.	The data bus may not work correctly.	X	
Low Power Modes	Deep Sleep	6.	Wake-up events that occur during Deep Sleep entry may not generate an event.	X	X
DC Characteristics	Supply Voltage	7.	Minimum operating voltage (VDD) Parameter F devices is 2.25V.	X	
Special Features	T1DIG	8.	T1DIG Configuration bit is not implemented.	X	X
MSSP	Port 1	9.	When MSSP1 is in I^2C™ mode, the RB4 and RB5 pins may have extraneous pulses.	X	
A/D	Band Gap Reference	10.	At high VDD voltages, performing an A/D conversion on Channel 15 could have issues.	X	X
CTMU	Constant Current	11.	VDD voltages below the LVDSTAT threshold can cause the constant current source to turn off.	X	
A/D Converter	Sample Acquisition	12.	ANx pin may output pull-up pulse during acquisition.	X	X
Timer1/Timer3	Async Timer Interrupts	13.	Spurious timer interrupt flag generation is possible when writing to the timer in Async Timer mode.	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: Master Synchronous Serial Port

In Master I²C™ Receive mode, if a Stop condition occurs in the middle of an address or data reception, the SCL clock stream will continue endlessly and the RCEN bit of the SSPCON2 register will remain improperly set. When a Start condition occurs after the improper Stop condition, nine additional clocks will be generated, followed by the RCEN bit going low.

Work around

Use low-impedance pull-ups on the SDA line to reduce the possibility of noise glitches that may trigger an improper Stop event. Use a time-out event timer to detect the unexpected Stop condition, and subsequently, the stuck RCEN bit. Clear the stuck RCEN bit by clearing the SSPEN bit of SSPCON1.

Affected Silicon Revisions

A2	A4						
X	X						

2. Module: Master Synchronous Serial Port (MSSP)

When configured for I²C slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read after the SSPIF interrupt (PIR1<3>) has occurred, but before the first rising clock edge of the next byte being received.

Work around

The issue can be resolved in either of these ways:

- Prior to the I²C slave reception, enable the clock stretching feature. This is done by setting the SEN bit (SSPxCON2<0>).
- Each time the SSPxIF is set, read the SSPxBUF before the first rising clock edge of the next byte being received.

Affected Silicon Revisions

A2	A4						
X	X						

3. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (SPEN bit (RCSTAx<7>) = 0)
- The EUSART is re-enabled (RCSTAx<7> = 1)
- A two-cycle instruction is executed immediately after setting SPEN, CREN or TXEN = 1

Work around

Add a 2 TCY delay after any instruction that re-enables the EUSART module (sets SPEN, CREN or TXEN = 1).

See Example 1.

Affected Silicon Revisions

A2	A4						
X	X						

EXAMPLE 1: RE-ENABLING AN EUSART MODULE

```
;Initial conditions: SPEN = 0 (module disabled)
;To re-enable the module:
;Re-Initialize TXSTAx, BAUDCONx, SPBRGx, SPBRGHx registers (if needed)
;Re-Initialize RCSTAx register (if needed), but do not set SPEN = 1 yet

;Now enable the module, but add a 2-Tcy delay before executing any two-cycle
;instructions
bsf    RCSTA1, SPEN        ;or RCSTA2 if EUSART2
nop                        ;1 Tcy delay
nop                        ;1 Tcy delay (two total)

;CPU may now execute 2 cycle instructions
```

4. Module: 10-Bit Analog-to-Digital Converter (A/D)

When the A/D conversion clock select bits are set for FOSC/2 (ADCON1<2:0> = 000), the Integral Linearity Error (EIL), parameter (A03) and Differential Linearity Error (EDL), parameter (A04), may exceed data sheet specifications.

Work around

Select one of the alternate A/D clock sources shown in Table 3.

TABLE 3: ALTERNATE ADC SETTINGS

ADCON1<2:0> ADCS<2:0>	Clock Setting
110	FOSC/64
101	FOSC/16
100	FOSC/4
011	FRC
010	FOSC/32
001	FOSC/8

Affected Silicon Revisions

A2	A4						
X	X						

5. Module: Parallel Master Port (PMP)

When configured for Parallel Slave Port (PMMODEH<1:0> = 00 and PMPEN = 1), the data bus (PMD<7:0>) may not work correctly. Incorrect data could be captured in the PMDIN1L register.

When configured for Parallel *Master* Port (PMMODEH<1:0> = 1x and PMPEN = 1), clearing a PMEx bit to disable a PMP address line also disables the corresponding PMDx data bus line.

Work around

None.

Affected Silicon Revisions

A2	A4						
X							

6. Module: Low-Power Modes (Deep Sleep)

Entering Deep Sleep mode takes approximately 2 TCY, following the SLEEP instruction. Wake-up events that occur during this Deep Sleep entry period may not generate a wake-up event.

Work around

If using the RTCC alarm for Deep Sleep wake-up, code should only enter Deep Sleep mode when the RTCC Value Registers Read Synchronization bit (RTCCFG<4>) is clear.

This will prevent missing an RTCC alarm that could occur during the period after the SLEEP instruction, but before the Deep Sleep mode has been fully entered.

The A4 revision silicon allows insertion of a single instruction between setting the Deep Sleep Enable bit (DSEN, DSCONH<7>) and issuing the SLEEP instruction (see Example 2). The insertion of a NOP instruction before the SLEEP instruction eliminates the 2 TCY window where wake-up events could be missed.

Before using this work around, users should check their device's revision ID bits to verify that they have the A4 silicon. This can be done at run time by a table read from address, 3FFFFEh.

On A2 revision silicon devices, the instruction cannot be inserted between setting the DSEN bit and executing the SLEEP instruction, or the device will enter conventional Sleep mode, not Deep Sleep.

On A4 silicon devices, if the firmware immediately executes SLEEP after setting DSEN, the device will enter Deep Sleep mode without benefiting from this work around.

EXAMPLE 2: DEEP-SLEEP WAKE-UP WORK AROUND

```
EnterDeepSleep:
    bsf     DSCONH, DSEN        ; Enter Deep Sleep mode on SLEEP instruction
    nop                         ; Not compatible with A2 silicon
    sleep                       ; Enter Deep Sleep mode
    (…)                         ; Add code here to handle wake up events that may
                                ; have been asserted prior to Deep Sleep entry
    goto    EnterDeepSleep      ; re-attempt Deep Sleep entry if desired
```

Affected Silicon Revisions

A2	A4						
X	X						

7. Module: DC Characteristics (Supply Voltage)

The minimum operating voltage (V_{DD}) parameter (D001) for the F devices is 2.25V. For the LF devices (such as PIC18LF46J11), the minimum rated V_{DD} operating voltage is 2.0V.

Work around

None.

Affected Silicon Revisions

A2	A4						
X							

8. Module: Special Features (T1DIG)

The T1DIG Configuration bit (CONFIG2L<3>) function is not implemented. Effectively, T1DIG is '0' regardless of the value programmed into the bit.

Work around

None.

Affected Silicon Revisions

A2	A4						
X	X						

9. Module: Master Synchronous Serial Port (MSSP) – Port 1

When MSSP1 is used in I^2C mode, the correct data and clock signals are present on the RC3 and RC4 pins. The RB4 and RB5 pins, however, may have extraneous pulses that prevent them from being used normally.

Work around

The RC3 and RC4 pins retain the correct clock and data signals, so the device should be connected to the I^2C bus through these pins. If TRISB<5> remains cleared, RB5 can be used as a general purpose output pin under normal firmware control.

This issue applies only to MSSP1 when used in the I^2C mode.

No work around is necessary if MSSP1 is used in an SPI mode or if MSSP2 is used.

Affected Silicon Revisions

A2	A4						
X							

10. Module: 10-Bit Analog-to-Digital Converter (A/D) – Band Gap Reference

At high V_{DD} voltages (for example, > 2.5V), performing an A/D conversion on Channel 15 (the V_{BG} absolute reference) can temporarily disturb the reference voltage supplied to the HLVD module and comparator module (only when configured to use the V_{IRV}).

At lower V_{DD} voltages, the disturbance will be less or non-existent.

Work around

If precise HLVD or comparator V_{IRV} thresholds are required at high V_{DD} voltages, avoid performing A/D conversions on Channel 15 while simultaneously using the HLVD or comparator, V_{IRV}. If an A/D conversion is performed on Channel 15, a settling time of approximately 100 μs is needed before the reference voltage fully returns to the original value.

Affected Silicon Revisions

A2	A4						
X	X						

11. Module: Charge Time Measurement Unit (CTMU)

On the F devices, the CTMU current source will stop sourcing current if the applied VDD voltage falls below the LVDSTAT (WDTCON<6>) threshold (2.45V nominal). When VDD is above the LVDSTAT threshold, the CTMU will function normally.

This issue does not apply to the LF devices. The current source will continue functioning normally at all rated voltages for these devices.

Work around

None.

Affected Silicon Revisions

A2	A4						
X							

12. Module: Analog-to-Digital Converter (A/D)

At the beginning of sample acquisition, one or more small, pull-up pulses (approximately 25 ns long) may output to the currently selected ANx analog channel. These pulses can lead to a positive offset error when the analog signal voltage is near VSS and the external analog signal driver is unable to dissipate the added pull-up voltage before the A/D conversion occurs.

Work around

Do one or more of the following:

- Use the "0 TAD" A/D Acquisition Time setting to start the next sample acquisition period immediately following A/D conversion completion.

  This allows the external analog signal driver more time to dissipate the pull-up pulses that occur when the sample acquisition is started.
- Use a longer A/D Acquisition Time setting to provide time for the external analog signal driver to dissipate the pull-up pulse voltage.
- Use low-impedance, active analog signal drivers to reduce the time needed to dissipate the pull-up pulse voltage.
- Experiment with external filter capacitor values to avoid allowing the pull-up voltage offset to affect the final voltage that gets converted.

  Small filter capacitor values (or none at all) will allow time for the external analog signal driver to dissipate the pull-up voltage quickly. Alternately, large filter capacitor values will prevent the short pull-up pulses from increasing the final voltage enough to cause A/D conversion error.

Affected Silicon Revisions

A2	A4						
X	X						

13. Module: Timer1/Timer3

When the timer is operated in Asyncronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to TMRxH:TMRxL register. An unexpected interrupt flag may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible operate the timer module in Synchronous mode to avoid spurious timer interrupts.

Example 3 shows a method to suppress the spurious interrupt flag if it occurs upon writing to the timer.

EXAMPLE 3: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode

T1CONbits.TMR1ON = 0;        //Stop timer from incrementing
PIE1bits.TMR1IE = 0;         //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;        //Turn on timer

//Now wait at least two full T1CKI periods before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert.  If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).

while(TMR1L < 0x02);         //Wait for 2 timer increments more than the Updated Timer
                             //value (indicating more than 2 full T1CKI clock periods elapsed)
PIR1bits.TMR1IF = 0;         //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;         //Now re-enable interrupt vectoring for timer 1
```

A2	A4						
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39932**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Special Features of the CPU

On the 32K Flash devices (PIC18F45J11, PIC18F25J11), it is necessary to write WPFP5 (CONFIG4L<5>) with '0' to maintain proper operation of the write-protect feature.

On the 16K Flash devices (PIC18F44J11, PIC18F24J11), it is necessary to write WPFP5 and WPFP4 (CONFIG4L<5:4>) with '00' to maintain proper operation of the write-protect feature.

At the time of this writing, MPLAB® tools may incorrectly maintain the WPFP5/WPFP4 bits as '1'. To force MPLAB to write the Configuration bits with the corrected values, refer to Code Examples 1 and 2.

EXAMPLE 1: C18

```
// 32K Flash Devices (PIC18F45J11, PIC18F25J11):
#pragma romdata config_section = 0x7FFE
const rom unsigned char config4l = 0xC0;
#pragma code

// 16K Flash Devices (PIC18F44J11, PIC18F24J11):
#pragma romdata config_section = 0x3FFE
const rom unsigned char config4l = 0xC0;
#pragma code
```

EXAMPLE 2: MPASM™

```
; 32K Flash Devices (PIC18F45J11, PIC18F25J11)
    ORG 0x7FFE
config4l_and_4h db 0xC0, 0xF0

; 16K Flash Devices (PIC18F44J11, PIC18F24J11)
    ORG 0x3FFE
config4l_and_4h db 0xC0, 0xF0
```

The corrected data sheet definition for Register 26-7:

REGISTER 26-7: CONFIG4L: CONFIGURATION REGISTER 4 LOW (BYTE ADDRESS 300006h)

R/WO-1	R/WO-1	R/WO-1	R/WO-1	R/WO-1	R/WO-1	R/WO-1	R/WO-1
WPCFG	WPEND	WPFP5(2)	WPFP4(3)	WPFP3	WPFP2	WPFP1	WPFP0
bit 7							bit 0

Legend:			
R = Readable bit	WO = Write-Once bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 WPCFG: Write/Erase Protect Configuration Region Select bit
1 = Configuration Words page is not erase/write-protected, unless WPEND and WPFP<5:0> settings protect the Configuration Words page(1)
0 = Configuration Words page is erase/write-protected, regardless of WPEND and WPFP<5:0>(1)

bit 6 WPEND: Write/Erase Protect Region Select bit
1 = Flash pages WPFP<5:0> through Configuration Words page are erase/write-protected
0 = Flash pages 0 through WPFP<5:0> are erase/write-protected

bit 5-0 WPFP<5:0>: Write/Erase Protect Page Start/End Location bits
Used with WPEND bit to define which pages in Flash will be erase/write-protected.

Note 1: The "Configuration Words page" contains the FCWs and is the last page of implemented Flash memory on a given device. Each page consists of 1,024 bytes. For example, on a device with 64 Kbytes of Flash, the first page is 0 and the last page (Configuration Words page) is 63 (3Fh).

2: This bit must be written with '0' on the 32K and 16K Flash devices for proper write-protect operation.

3: This bit must be written with '0' on the 16K Flash devices for proper write-protect operation.

2. Module: Low-Power Modes

The last paragraph in **Section 4.6.3 "Deep Sleep Wake-up Sources"** should read as follows:

"The software can determine the wake event source by reading the DSWAKEH and DSWAKEL registers. When the application firmware is done using the DSWAKEH and DSWAKEL Status registers, **the firmware must manually clear the registers prior to entering Deep Sleep again, in order to ensure that the correct wake-up source is indicated upon resuming operation."**

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (2/2009)
First release of this document. Silicon issues 1-2 (MSSP), 3 (EUSART), 4 (ADC), 5 (PMP), 6 (Deep Sleep), 7 (Supply Voltage).

Rev B Document (3/2009)
Modified silicon issues 1 (MSSP) and 3 (EUSART), and added silicon issue 8 (Special Features – T1DIG).

Rev C Document (4/2009)
Added silicon issue 9 (Master Synchronous Serial Port (MSSP) – Port 1).

Rev D Document (6/2009)

Revised document to new format. Added silicon issues 10 (10-Bit A/D – Band Gap Reference) and 11 (CTMU).

Rev E Document (10/2009)

Replaced silicon issue 1 (I^2C Initialization) with 1 (MSSP). Added data sheet clarifications 1 (Comparator Voltage Reference Module), 2 (28-Pin QFN Pinout Diagram), 3 (RC4, RC5 Input/Output Pins), 4 (MSSP Pins), 5 (Watchdog Timer, Features Summary) and 6 (DC Characteristics).

Rev F Document (12/2009)

Revised silicon issue 6 (Low-Power Modes). Added data sheet clarification 7 (DC Characteristics – Power-Down Current).

Rev G Document (4/2010)

Revised silicon issue 5 (Parallel Master Port – PMP). Added silicon issue 12 (A/D Converter – A/D). Added data sheet clarification 6 (**Section 4.4 "Brown-out Reset (BOR)"**. Renumbered previous data sheet clarifications 6-7, now 7-8.

Rev H Document (11/2010)

Added data sheet clarification issue 9 (Electrical Characteristics).

Rev J Document (4/2011)

Removed all data sheet clarifications that have since been made to the data sheet. Added new data sheet clarification 1 (Special Features of the CPU).

Rev K Document (11/2013)

Added MPLAB X IDE; Added silicon issue 13 (Timer 1/ Timer 3); Other minor corrections;

Data Sheet Clarifications: Added data sheet clarification 2 (Low Power Modes).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

Printed on recycled paper.

ISBN: 9781620776148

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://www.microchip.com/support
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hangzhou
Tel: 86-571-2819-3187
Fax: 86-571-2819-3189

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880- 3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-366
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7830

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-3766400

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Pforzheim
Tel: 49-7231-424750

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

10/28/13